Trends in ultra fast silicon trackers

A. Rivetti - INFN Torino

Thanks to contribution by:

N. Cartiglia, L. Demaria, M. Mandurrino, E. Monteil, J. Olave, L. Pacher, L. Pancheri, M. Rolo

Future accelerators under study - energy frontier

Lepton colliders

- ILC
- CLIC
- FCC/e+e-
- CEPC

- Vertex/tracking detectors require:
  - ✓ Very good spatial resolution O(μm)
  - ✓ Very low material budget (0.15% X_0/layer)
  - ✓ Moderate time resolution
  - ✓ Moderate radiation hardness (1 Mrad TID, 10^{12} eq. neutrons)
- Vertex detector: silicon
- Main tracker: silicon or TPC

• **Very precise**

Hadron colliders

- HE-LHC
- FCC/pp
- SppC

- Vertex/tracking detectors require:
  - ✓ Very good spatial resolution O(μm)
  - ✓ low material budget
  - ✓ Very good time resolution
  - ✓ Extreme radiation hardness
- Vertex detector: silicon
- Main tracker: silicon

• **Very fast**

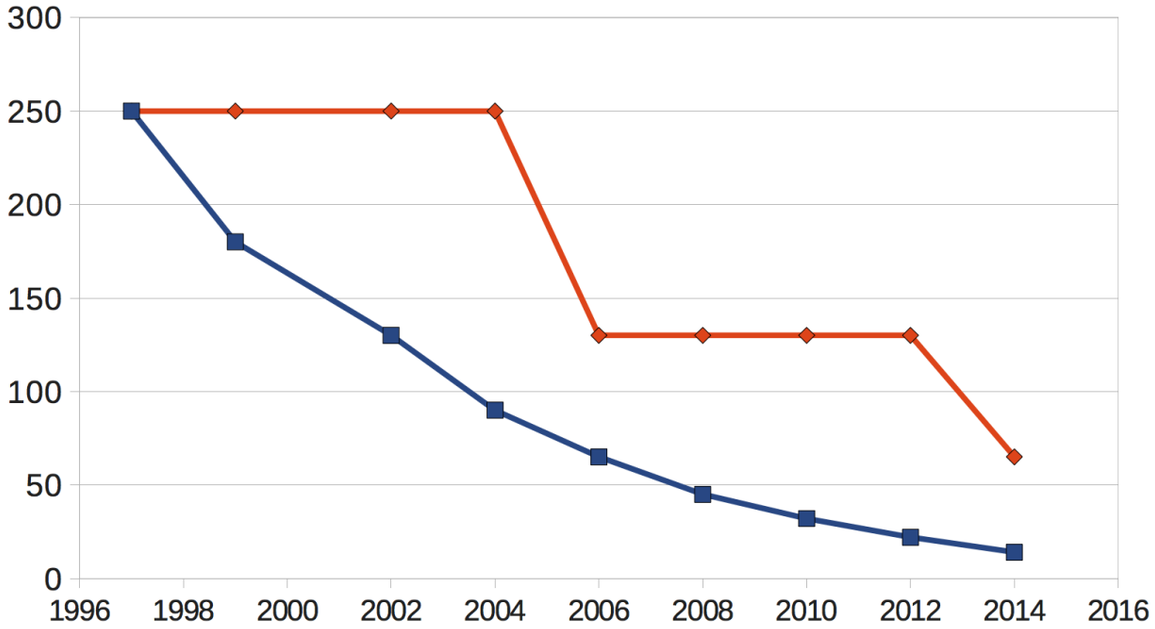
Facilities at the intensity frontier

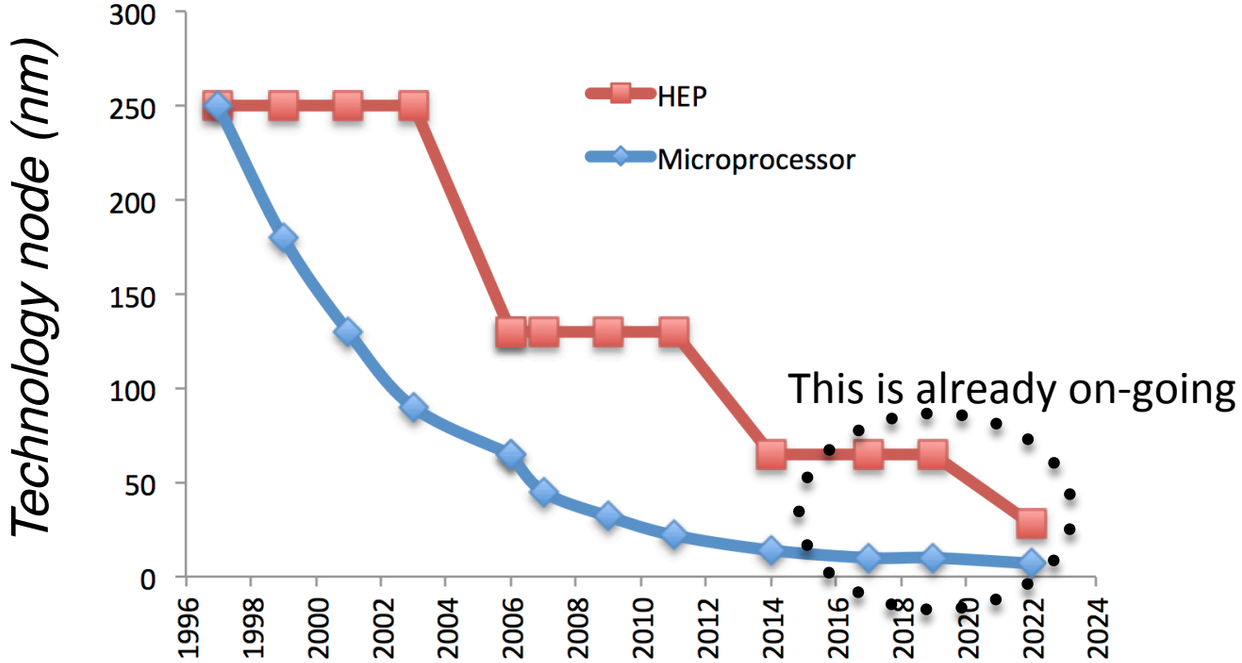
- FAIR at GSI-Germany
- NICA at JINR
- Electron-Ion collider
- ….

- Smaller and shorter term facilities can provide an ideal playground to test advanced detector concepts

Relevant trends in sensors/electronics

- Fast data transmission
- Better time resolution
- Smaller pixels, more functionality
- CMOS sensors with even larger Q/C and charge collected by drift: DMAPS
- Stitching
- 3D/high density interconnect





Fast data transmission

Y. Frans et al.

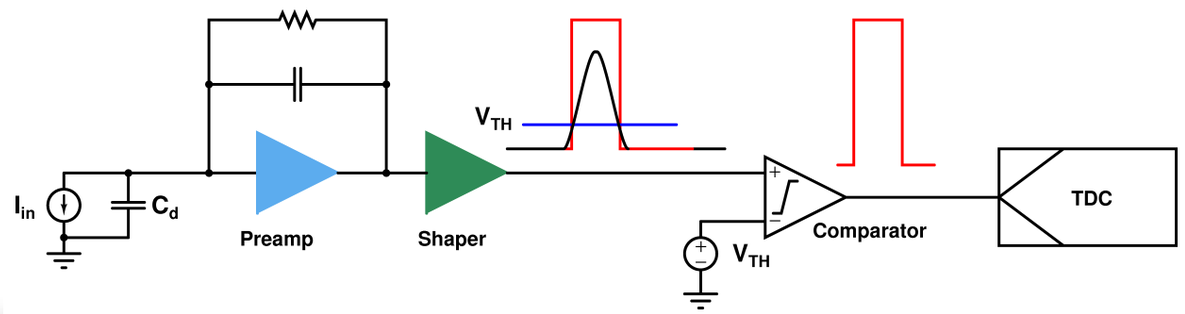
IEEE Journal of Solid-State Circuits (Volume: 51, Issue: 12, Dec. 2016)

	This work	[Chen CICC'14]	[Jiang ISSCC'14]
Technology	16nm FinFET	65nm CMOS	65nm CMOS
Data-rate	40-64 Gb/s	50-64.5 Gb/s	60Gb/s
FFE	3-tap	4-tap	None
Area (TX Only)	0.32mm2 (C4 array limited)	0.35mm2	2.1mm2
Power (TX) per channel	225mW @ 64Gb/s	199mW @64Gb/s	450mW @60Gb/s
Power (PLL+Clock Distribution) per channel	115mW @ 64Gb/s	N/A	
TX Amplitude (No EQ, diff-pp)	800mV	850mV	500mV
Wide-band TX Jitter (Clock Pattern)	RJ-rms=150fs PJ-pp=200fs DCD=30fs	Not reported	Not reported (narrow-band rms=461fs from 1kHz to 20MHz)
TX Jitter (PRBS)	PJ=600fs ISI=2.8ps	Not reported	Not reported

- Power O(200 mW) for 64 Gbit/s, about 1.6 Gevents
- Take 1 cm^2, 50 µm x 50 µm: 5 µW/pixel
- Power likely to be dominated by data transfer

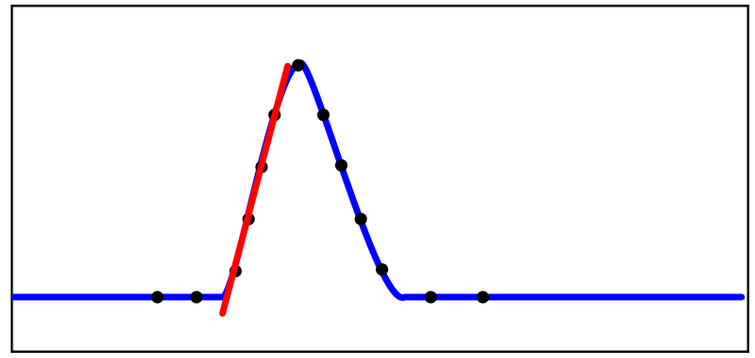
Better time resolution

Single sample timing



- Timing pulse provided by a discriminator
- Leading edge or zero crossing (CFD)
- Simple and compact electronics
- Suitable for highly pixellated detectors
- Can be used to measure also charge

Multiple sample timing



- Waveform sampling
- Many opportunities for DSP
- Data throughput is an issue
- Higher power/lower density

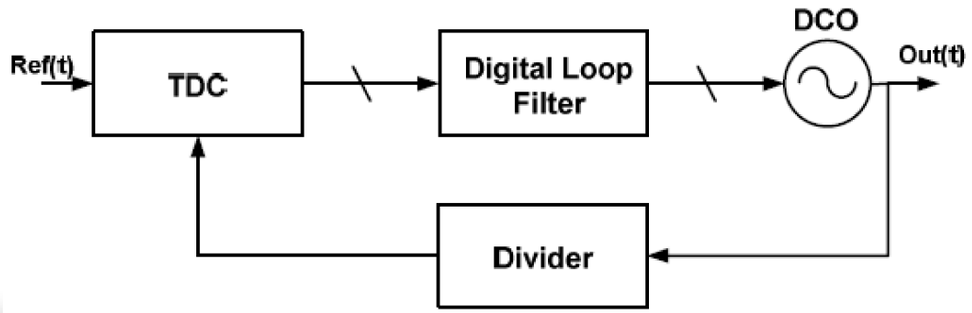
Time to digital converters

H. Wang, F. F. Dai A 14-Bit, 1-ps resolution, two-step ring and 2D Vernier TDC in 130nm CMOS technology
ESSCIRC 2017 - 43rd IEEE European Solid State Circuits Conference

TABLE I. TDCs PERFORMANCE COMPARISON

	VLSI 14 [7]	ISSCC 15 [8]	ISSCC 16 [9]	CICC 17 [2]	ISSCC 17 [1]	**This work**
Topology	Cyclic	Stochastic	SS-ADC	2D Vernier	SAR-ADC	**Ring+2D Vernier**
Process	28nm	14nm	65nm	45nm	14nm	**130nm**
NoB	12	10	6.1	8	7	**14**
ENoB (1)	9.74	8.28	5.76	7.58	3.68	**13.2**
Resolution	0.63ps	1.17ps	6ps	1.25ps	0.2ps	**1.0ps**
ER (2)	3.15ps	3.85ps	7.60ps	1.67ps	2ps (4)	**1.74ps**
Speed [MHz]	10	100	40	80	26	**10**
DNL [LSB]/[ps]	0.5/0.32	0.8/0.94	---/---	0.25/0.31	---/---	**0.41/0.41**
INL [LSB]/[ps]	3.8/2.39	2.3/2.7	0.27/1.6	0.34/0.4	9/1.8	**0.79/0.79**
Power [mW]	0.82	0.78	0.36	0.33	---	**2.4**
FoM (3)	0.02	0.01	0.13	0.02	---	**0.02**

1. ENoB = NoB – $\log_2$ (INL+1).
2. Effective Resolution (ER) = Resolution × $2^{(NOB - ENOB)}$.
3. FoM = Power / ($2^{NOB} \times F_S$) [pJ / conv-step].
4. calculated based on in-band phase noise. PN = $10\log(N^2(2\pi f_r)^2 t_{res}^2/12/f_r)$.

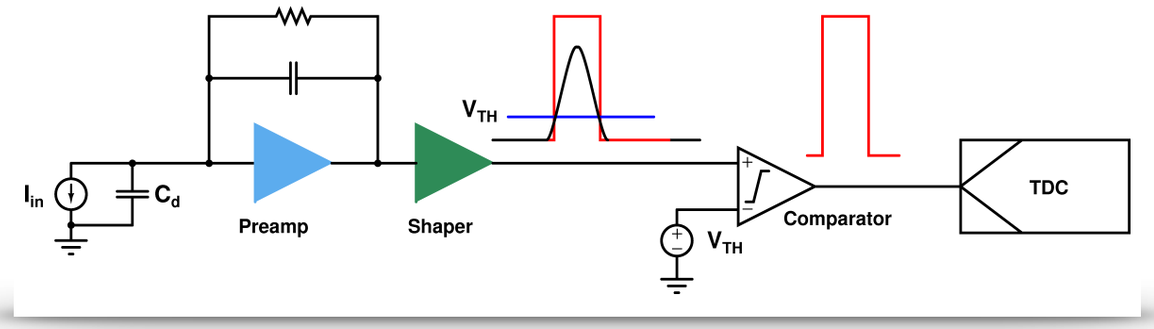


- TDCs now hitting the ps barrier
- Much progress thanks to ADPLL
- Many possible topologies

- TDCs not the limiting component in high resolution timing systems

Timing uncertainties

Timing jitter

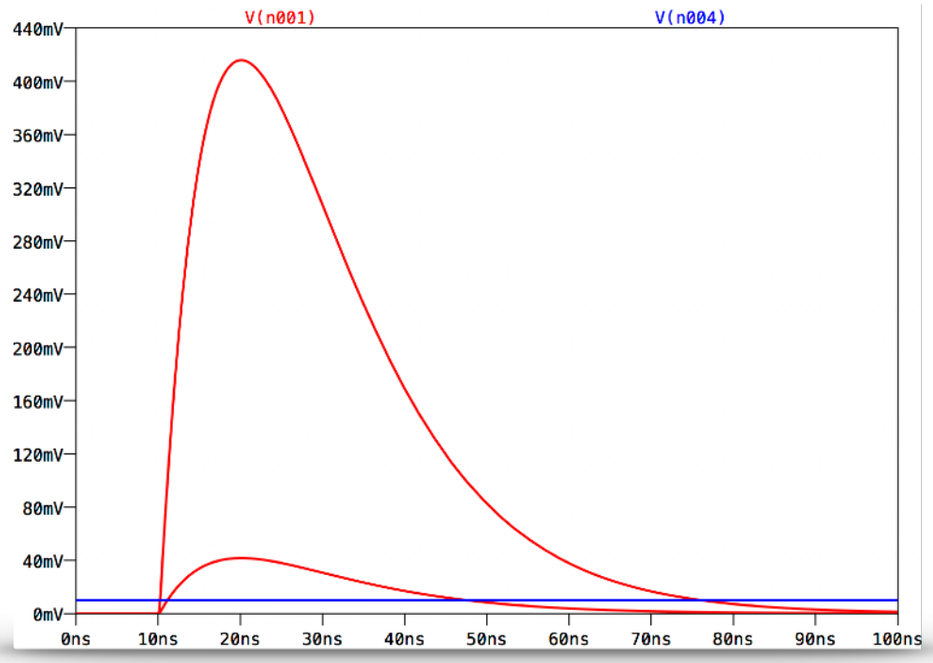


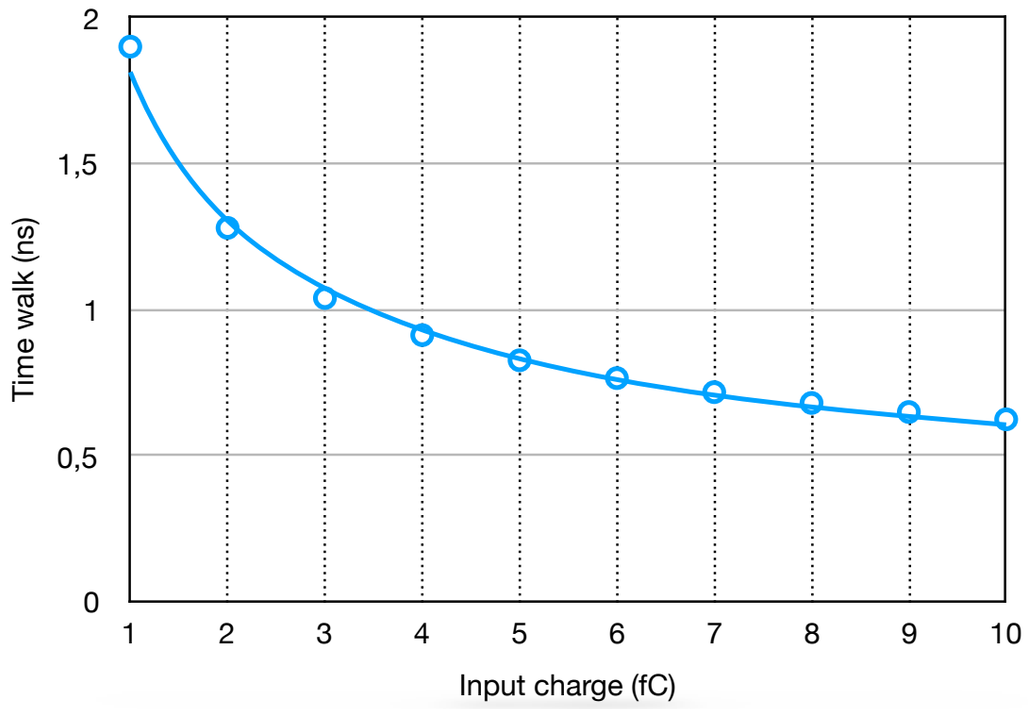
$$\sigma_t = \frac{\sigma_n}{\frac{dV}{dt}} \approx \frac{v_n}{\sqrt{2t_a}} \frac{C_d}{Q_{in}} \sqrt{t_a^2 + t_d^2} = \frac{v_n C_d}{Q_{in}} \sqrt{t_d}$$

Eg: g_m=30 µS, Cd=100 fF, Qin=1 fC, td=5 ns
σt= 117 ps

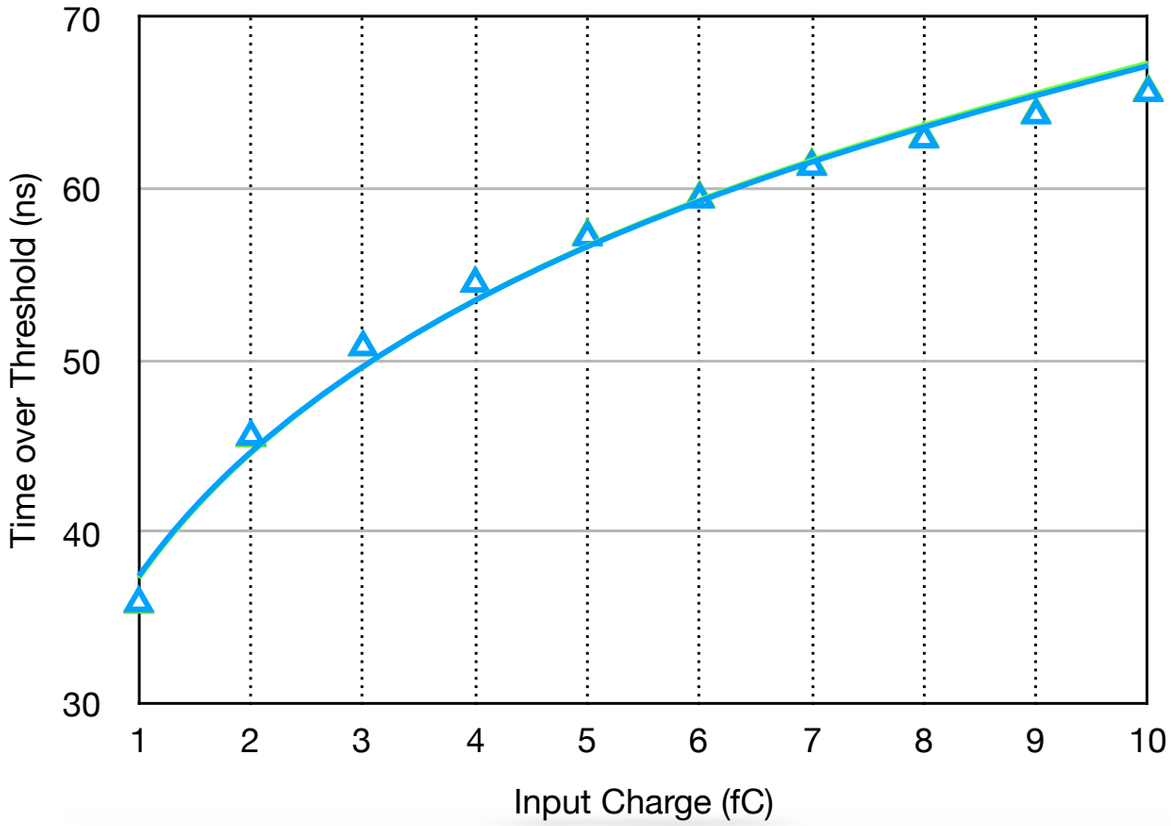
- Q/C very important also for good timing!

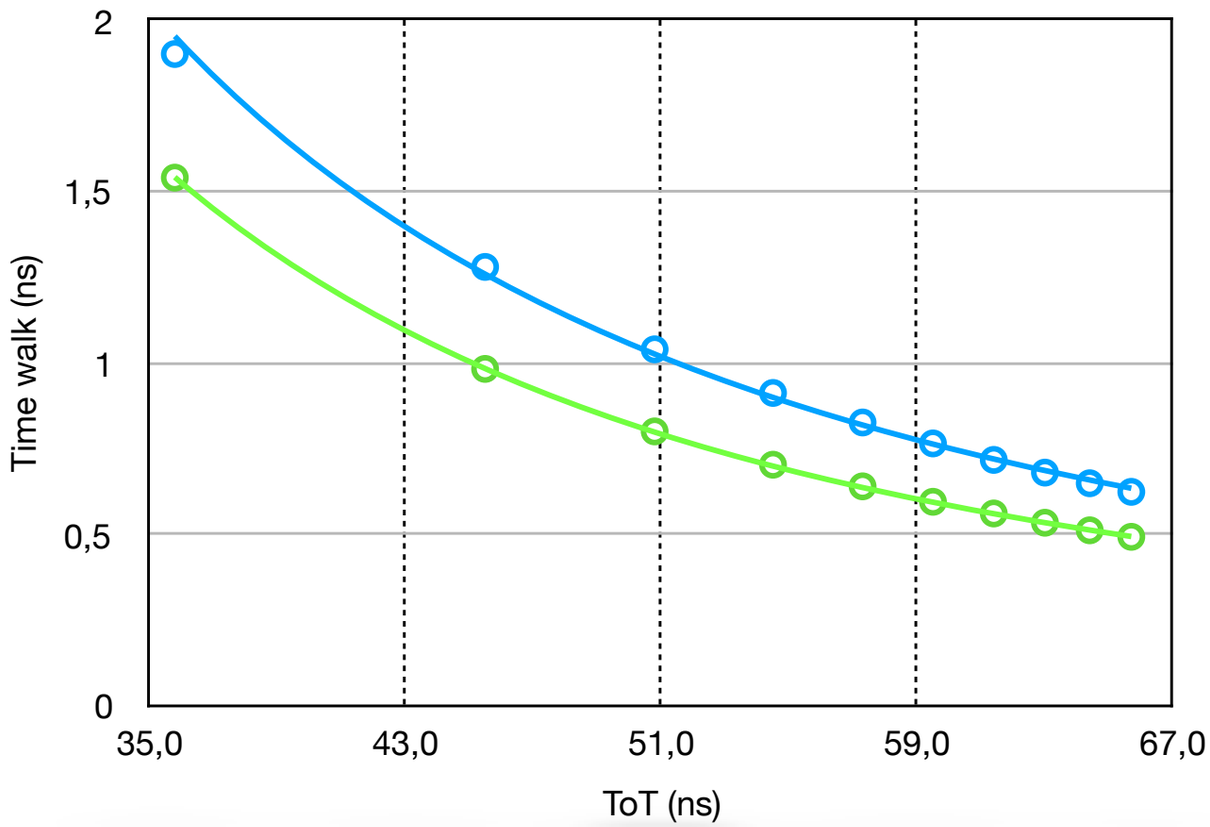
Time walk

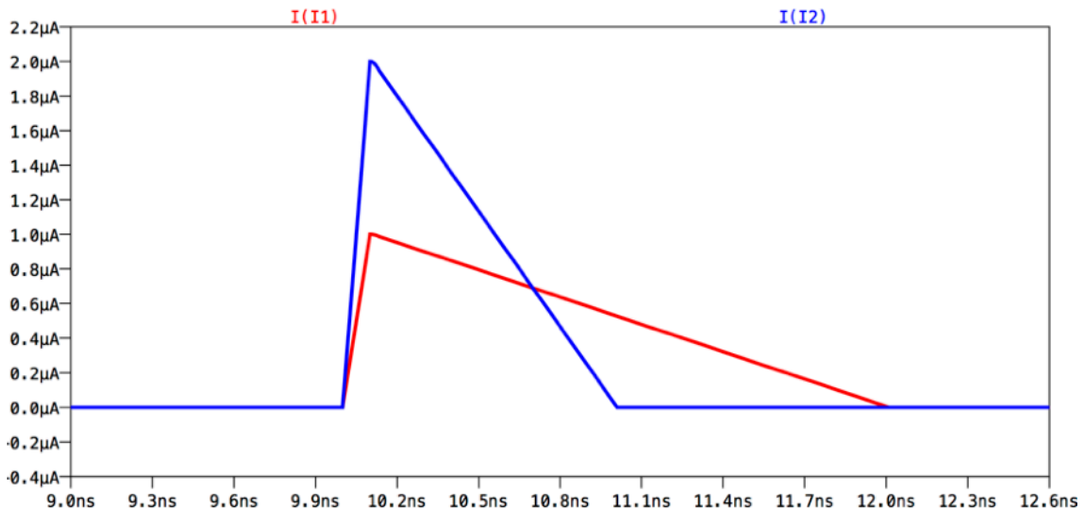




Shape related effects

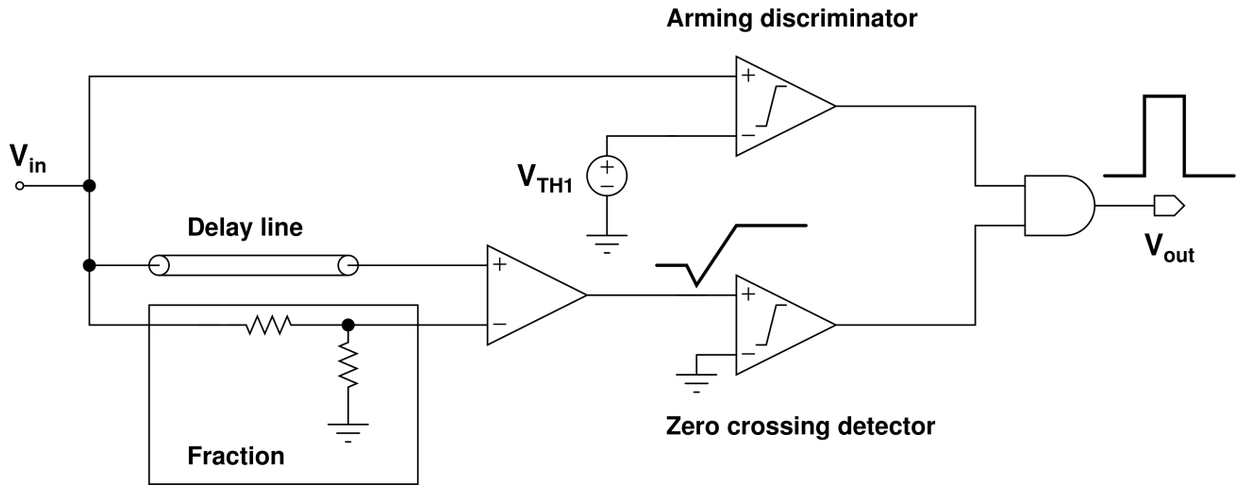






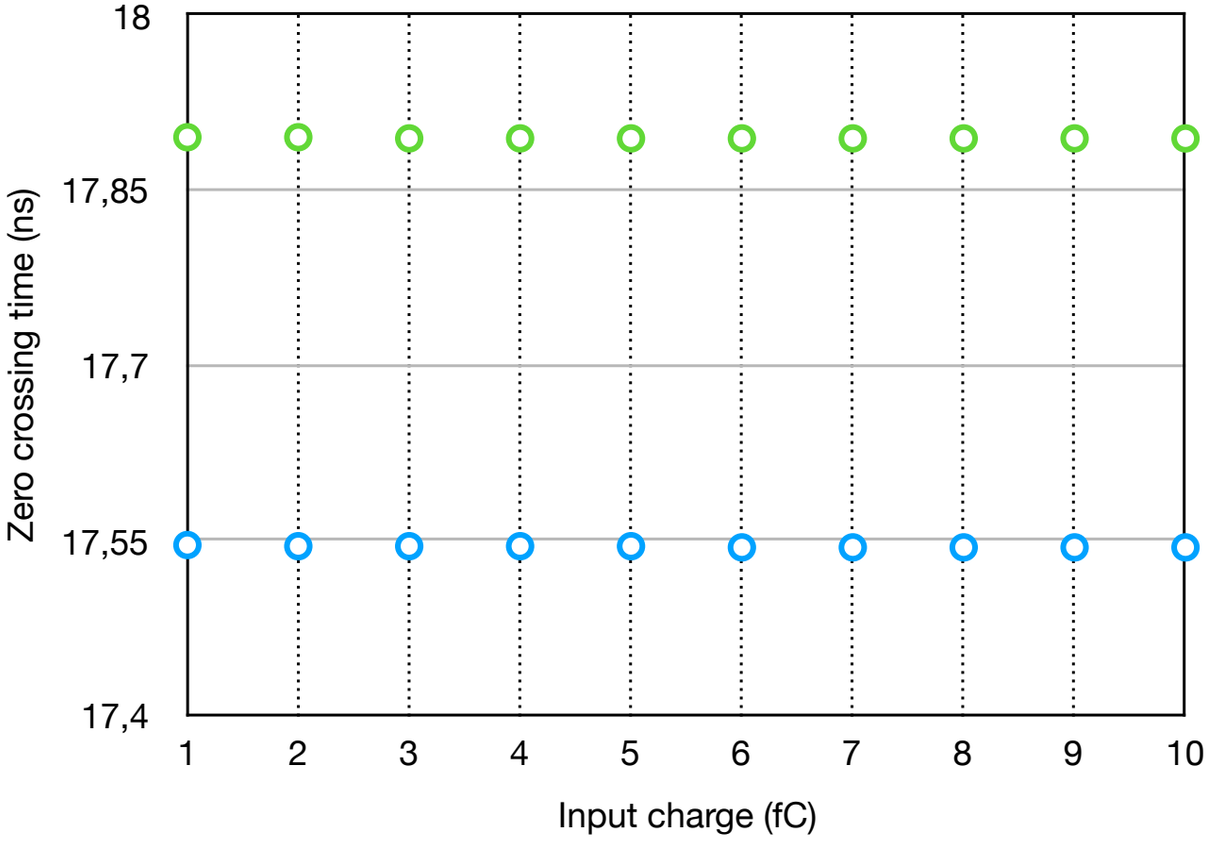
- Pulse shape variations affect timing
- Detector and front-end co-design to predict reasonably timing performance

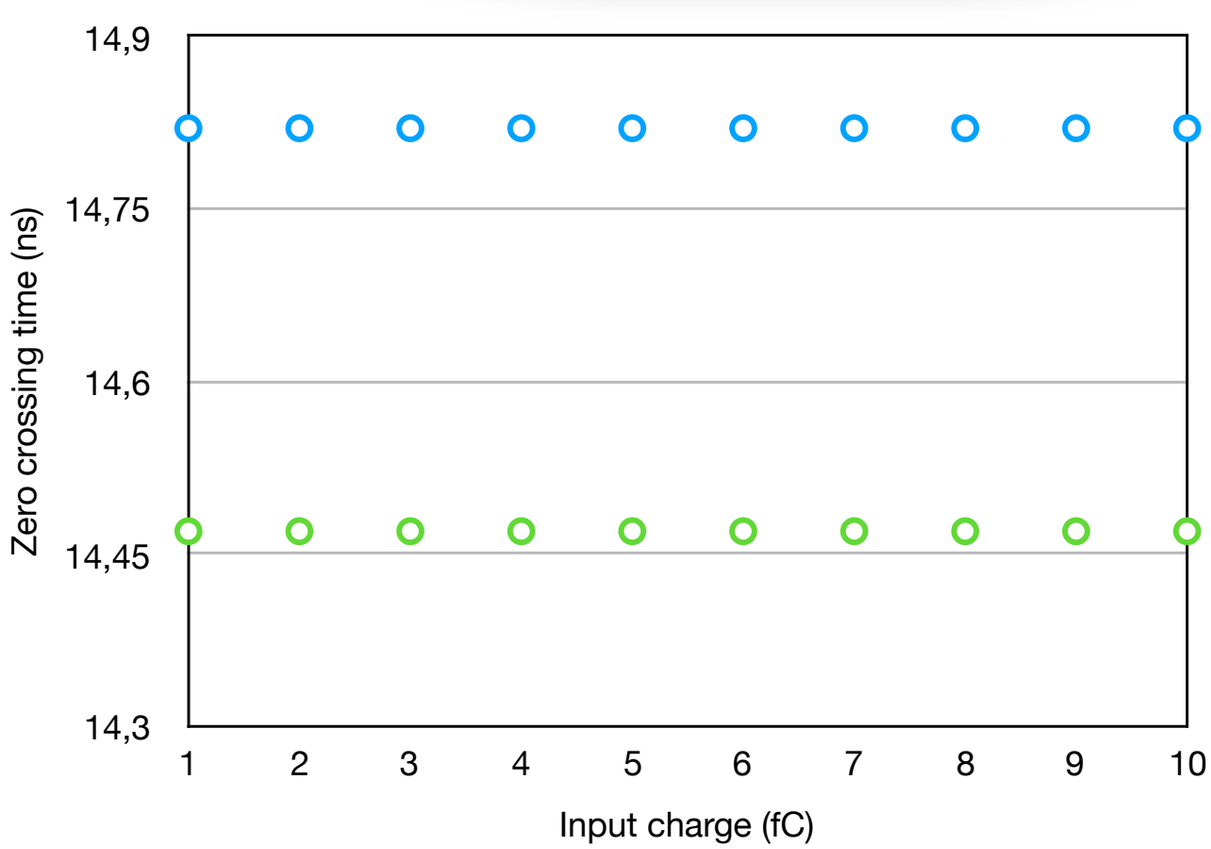
Constant fraction?



$$t_{zc} = \frac{t_d}{1-f}$$

$$t_{zc} = \frac{t_d e^{\frac{t_d}{\tau}}}{e^{\frac{t_d}{\tau}} - f}$$

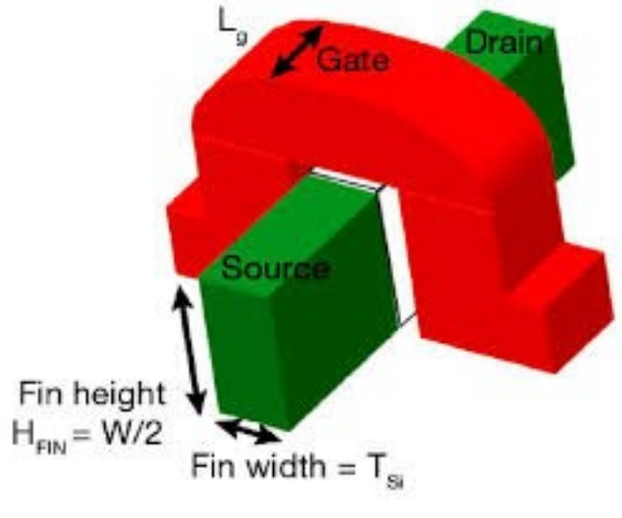


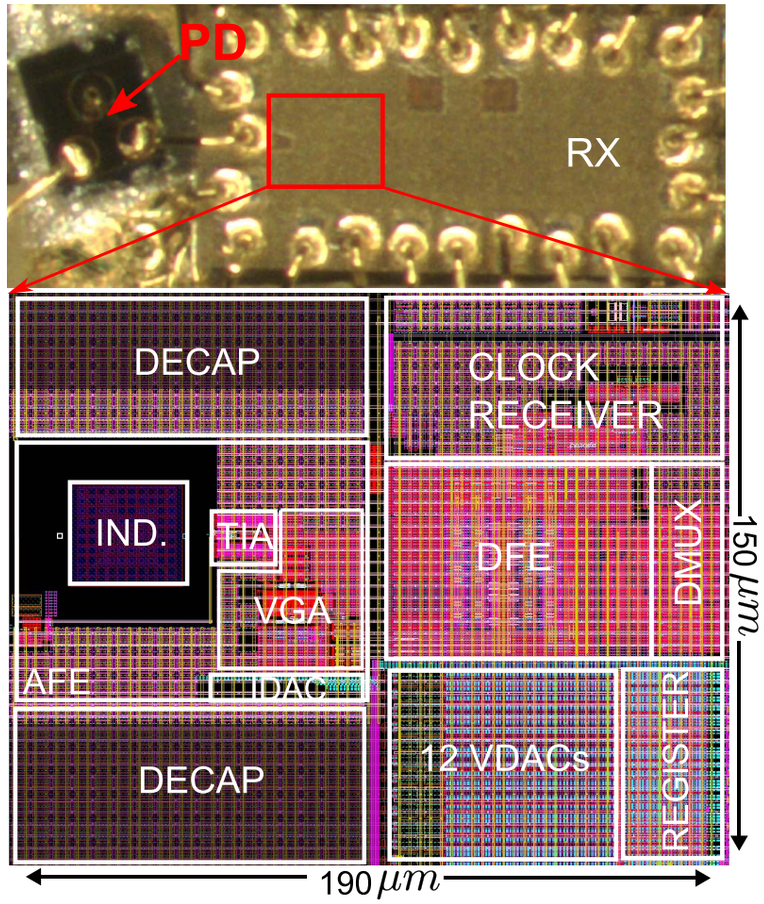


IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 52, NO. 12, DECEMBER 2017

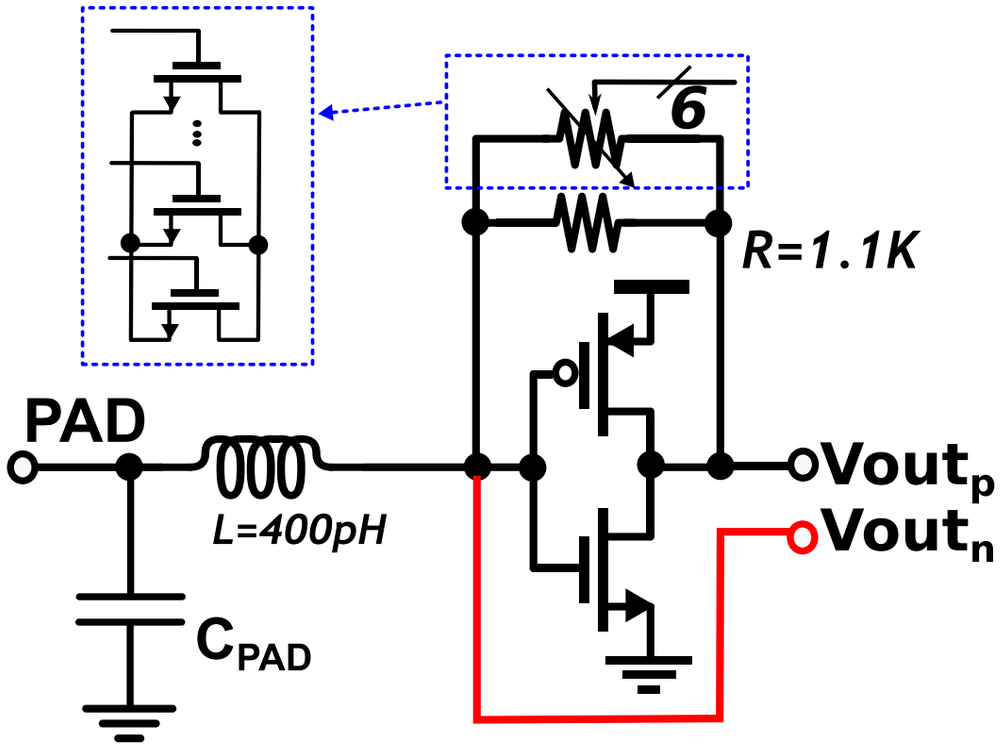
A 64-Gb/s 1.4-pJ/b NRZ Optical Receiver Data-Path in 14-nm CMOS FinFET

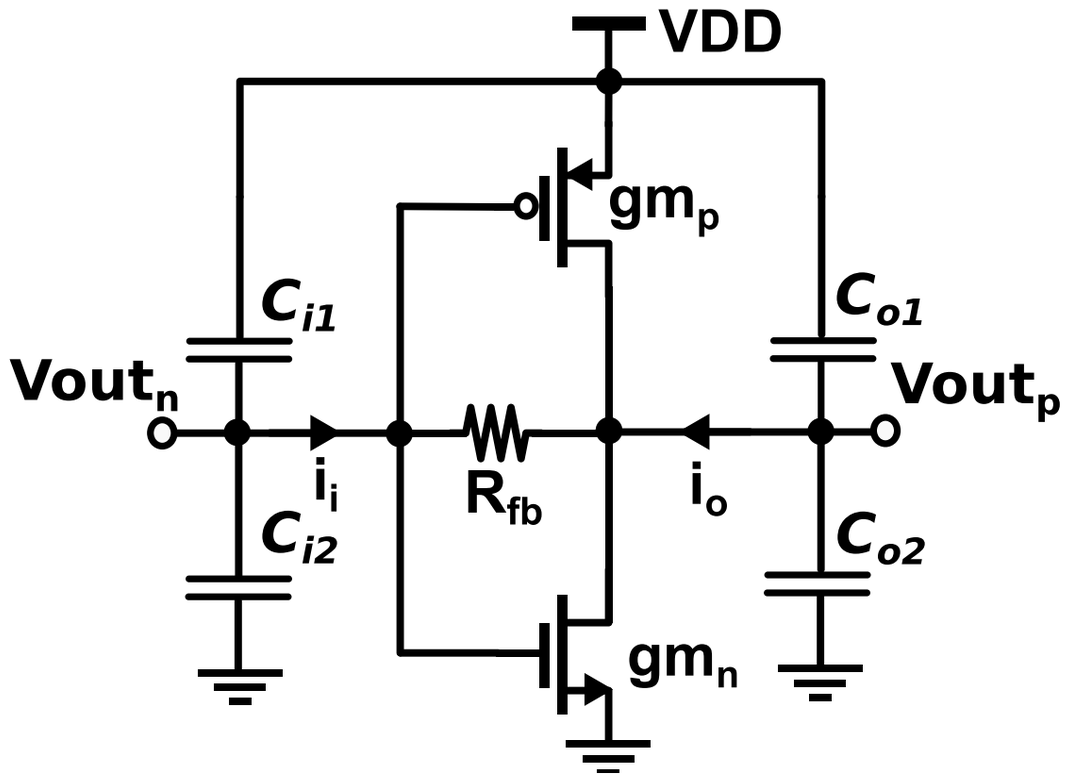
Ilter Ozkaya, *Student Member, IEEE*, Alessandro Cevrero, *Member, IEEE*, Pier Andrea Francese, *Senior Member, IEEE*, Christian Menolfi, *Member, IEEE*, Thomas Morf, *Senior Member, IEEE*, Matthias Brändli, Daniel M. Kuchta, *Senior Member, IEEE*, Lukas Kull, *Senior Member, IEEE*, Christian W. Baks, Jonathan E. Proesel, *Senior Member, IEEE*, Marcel Kossel, *Senior Member, IEEE*, Danny Luu, *Student Member, IEEE*, Benjamin G. Lee, *Senior Member, IEEE*, Fuad E. Doany, Mounir Meghelli, *Member, IEEE*, Yusuf Leblebici, *Fellow, IEEE*, and Thomas Toifl, *Senior Member, IEEE*





Front-end with 25 ps peaking time





$$\frac{C_{i1}}{C_{i2}} = \frac{gm_p}{gm_n} = \frac{C_{o1}}{C_{o2}}.$$

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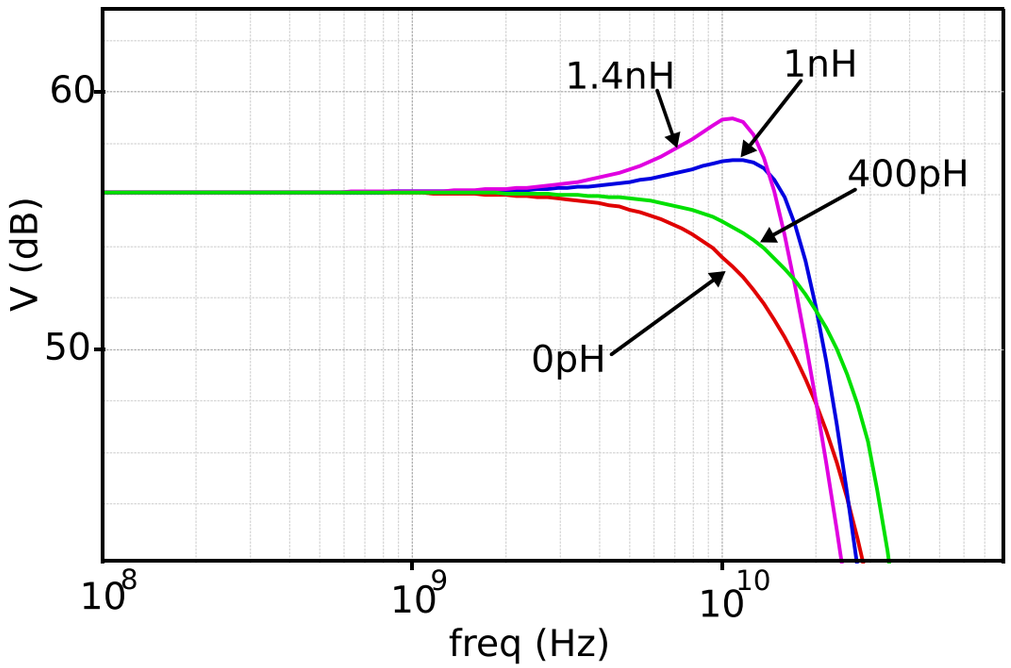
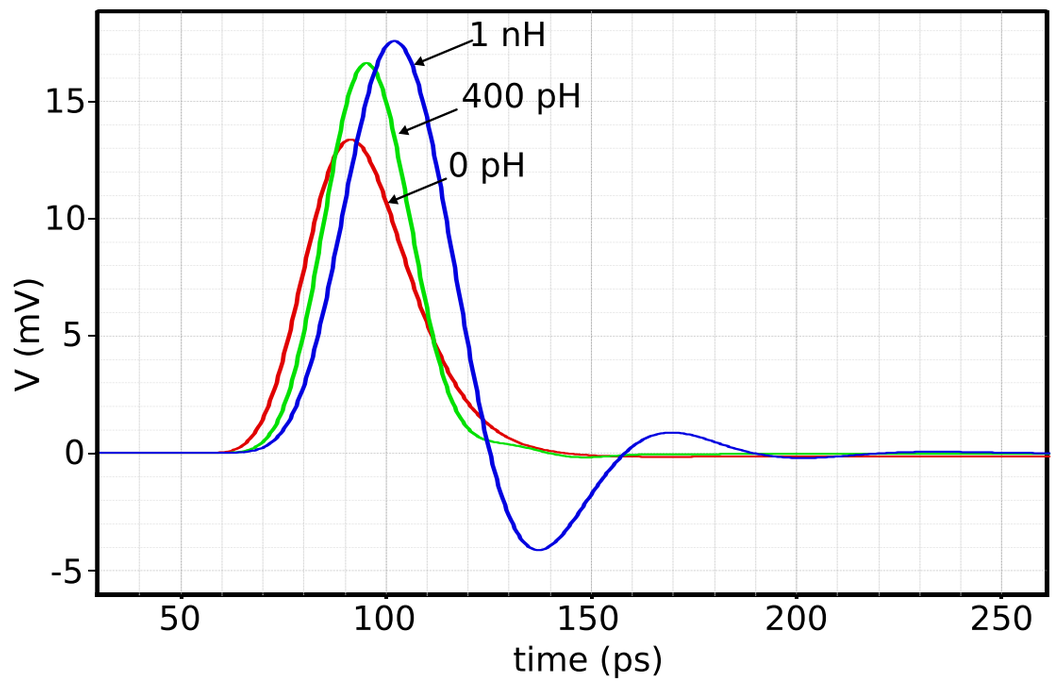
A 64-Gb/s 1.4-pJ/b NRZ Optical Receiver Data-Path in 14-nm CMOS FinFET

Front-end with 25 ps peaking time

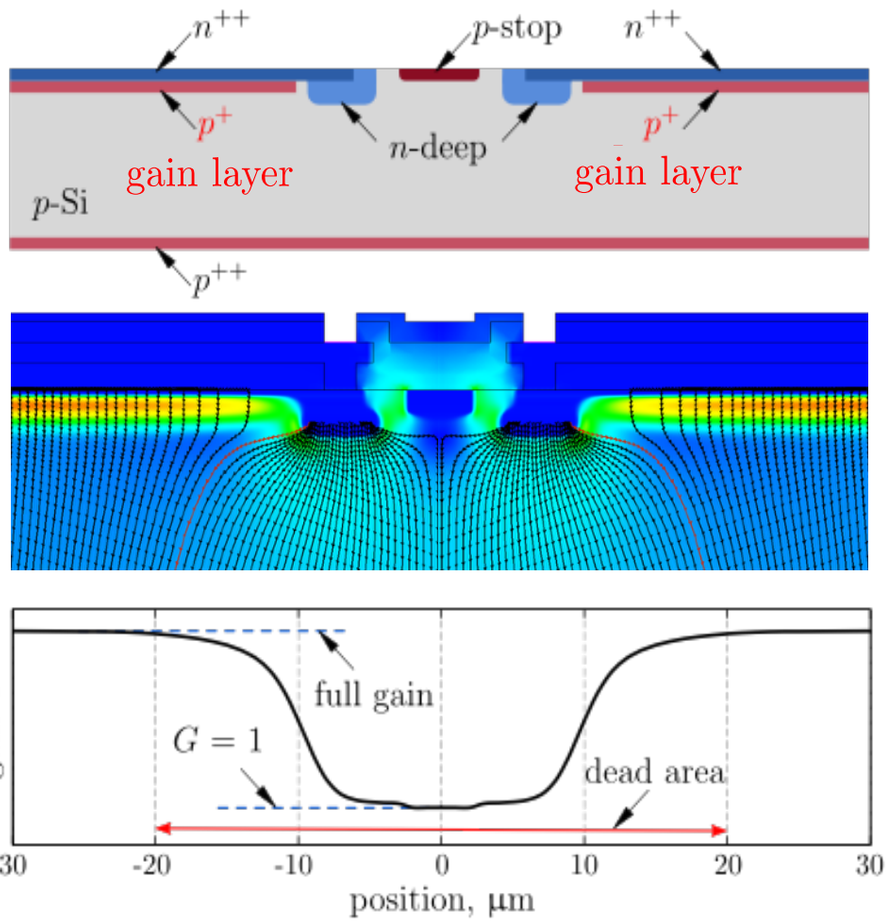




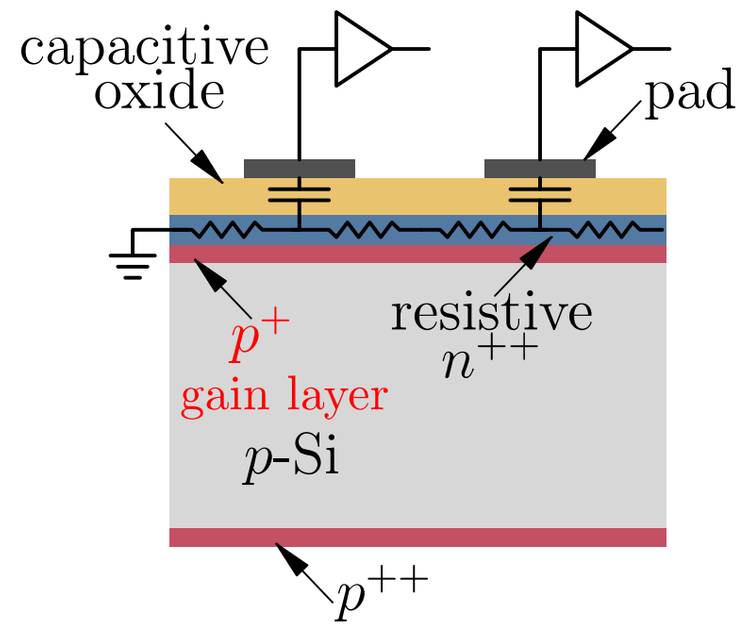
- Power O(10 mW) for 100 fF input capacitance

Again on LGAD

- No gain zone between pixel



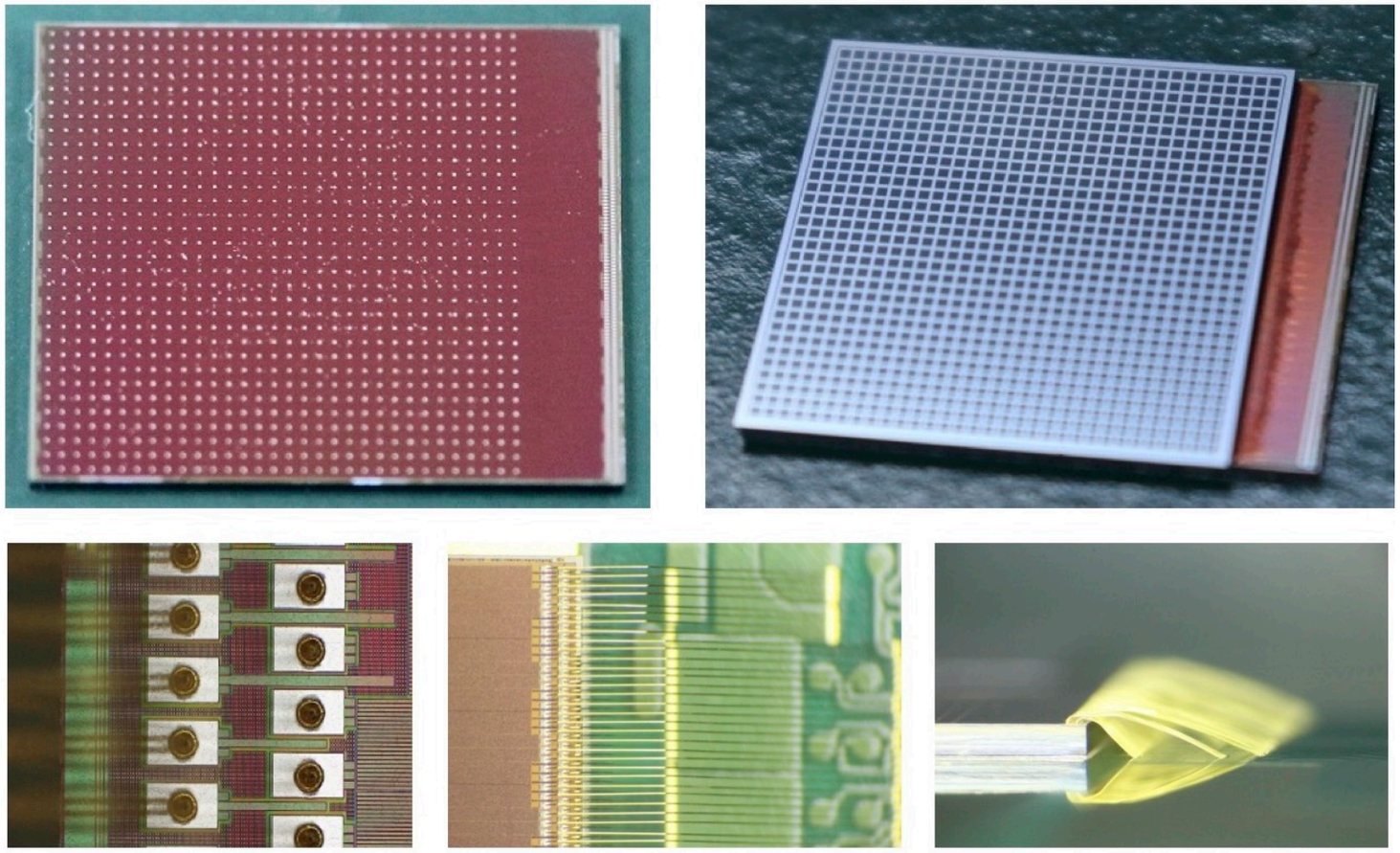
- Homogeneous gain layer
- Small pixels



RSD ingredients:

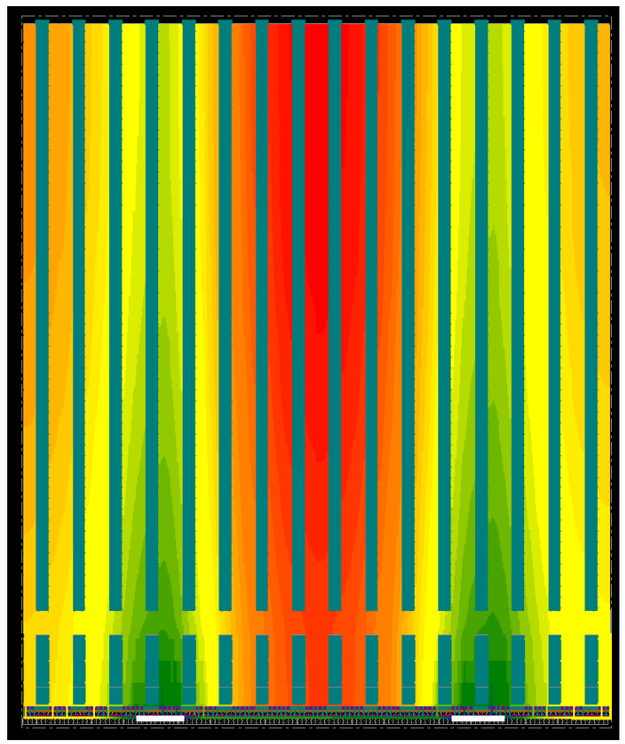
1. Resistive cathode: freeze the signal
2. Cap oxide: couple the signal with pads

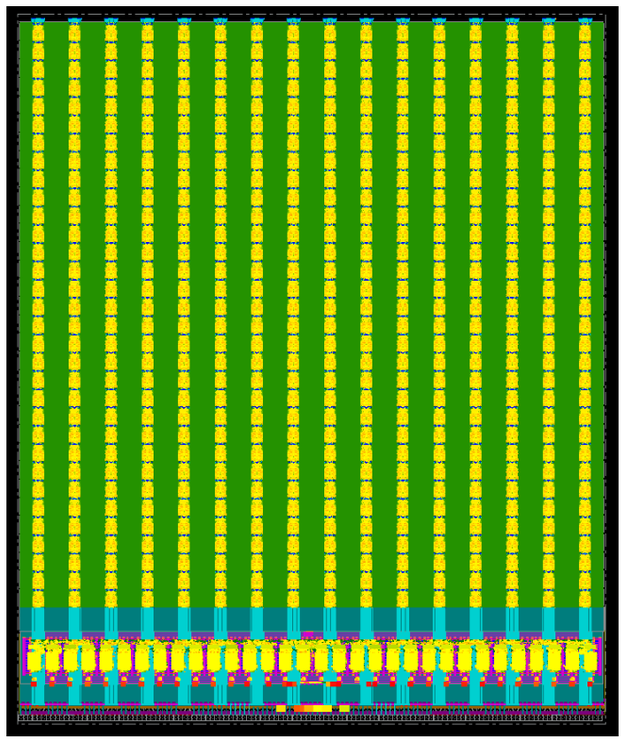
An example of timing chip



- Timing front-end ASIC: 1024 channels, 4096 TDC, 20 Gbit/s output bandwitdth
- Technology 110 nm CMOS
- Pixel size 400 μm$\times$400 μm
- TDC binning 20$\div$100 ps, DNL %
- Overall system jitter $\approx$ 30 ps r.m.s.

System level issues





- Best achievable performance often compromised by system-level issues
- Verification, verification, verification

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

A 12-bit 150-MS/s Sub-Radix-3 SAR ADC With Switching Miller Capacitance Reduction

Kwuang-Han Chang, *Member, IEEE*, and Chih-Cheng Hsieh, *Member, IEEE*

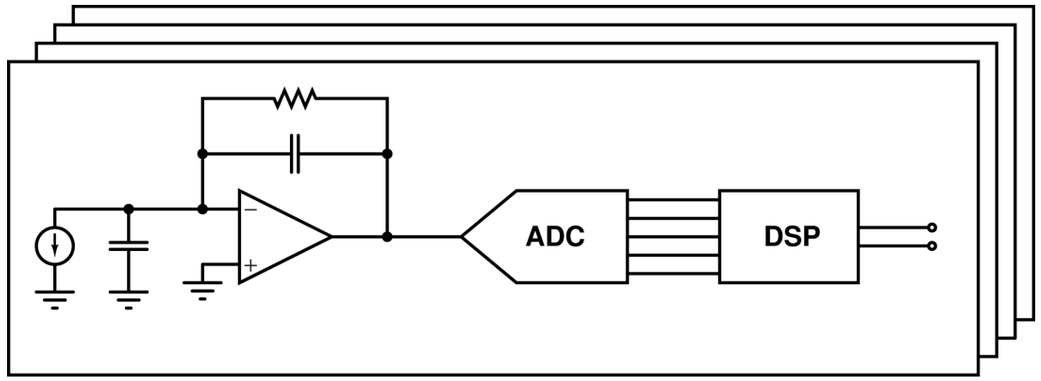
COMPARISON TABLE OF THE STATE-OF-THE-ART ADCs

	[25] Tseng, JSSC 2016		[8] Lin, TCASI 2016	[4] Hong, JSSC 2015	[9] Zhou, JSSC 2015	[10]Mathew, VLSI 2015	[26] Tsai, JSSC 2015	This work
Architecture	SAR		Pipelined-SAR (2-ch)	Pipelined	Two-step SAR	Flash-TDC SAR	SAR	SAR
Technology	28 nm		65 nm	65 nm	40 nm	45 nm	28 nm	40 nm
Supply Voltage	1.2V/1.1V		1.0 V	1.2 V	1.1 V	0.85 V	1.0 V	0.9 V
Resolution	12 bit		12 bit	12 bit	12 bit	12 bit	10 bit	12 bit
Sampling Rate	104 MS/s		210 MS/s	250 MS/s	160 MS/s	200 MS/s	240 MS/s	150 MS/s
SNDR @ peak (dB)	60.5*	63**	63.4	67.0	66.5	68.5	57.1	61.7
SFDR @ peak (dB)	76*	N/A**	77.5	84.6	85.9	N/A	73	74.4
SNDR @ Nyq (dB)	45*	N/A**	60.1	65.7	65.3	68.0	53	56.2
SFDR @ Nyq (dB)	52*	N/A**	74.8	79.0	86.9	N/A	63	63.5
DNL (LSB)	< 0.5		-0.57 / +0.66	-0.86 / +0.52	N/A	-0.60 / +0.40	+0.45 / -0.23	-0.91 / +1.77
INL (LSB)	< 1.1		-0.68 / +1.45	-0.90 / +1.08	N/A	-0.90 / +0.80	+0.55 / -0.45	-2.63 / +2.95
Power (mW)	3.06*	0.88**	49.7	5.3	4.96	3.4	0.68	1.5
FoM_w @ peak (fJ/conv.-step)	34*	7.3**	20.9	108.5	17.7	7.9	4.8	10.3
FoM_w @ Nyq (fJ/conv.-step)	203*	N/A**	30.3	126.8	20.7	8	7.8	18.9
Core Area (mm^2)	* 0.024	** 0.003	0.594	0.48	0.042	0.06	0.003	0.04

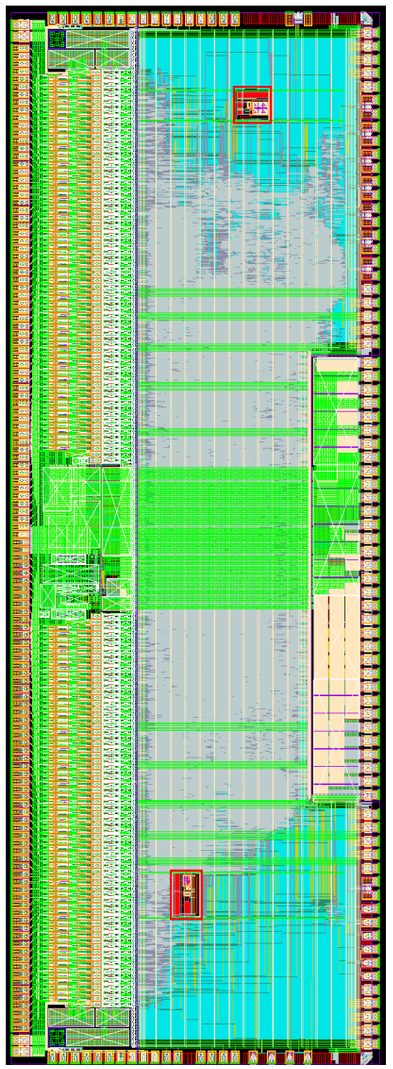
* : ADC+Ref+Buf

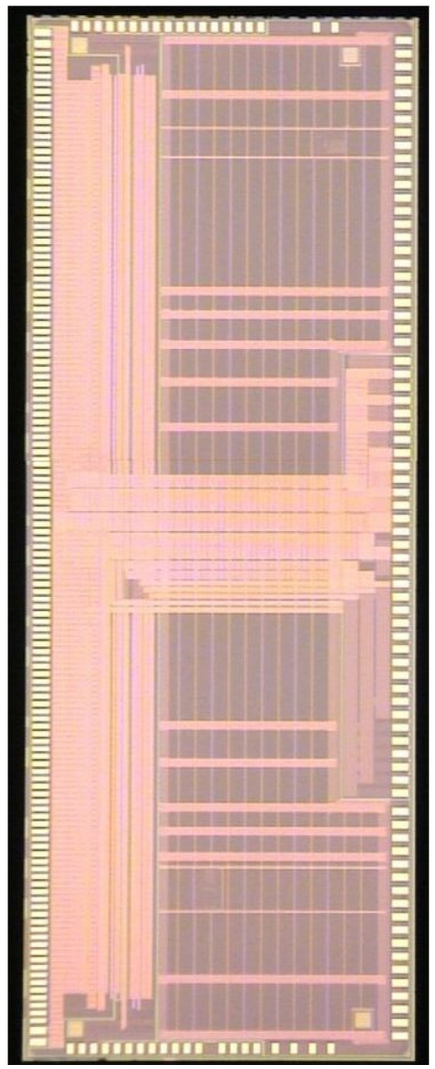
** : ADC only

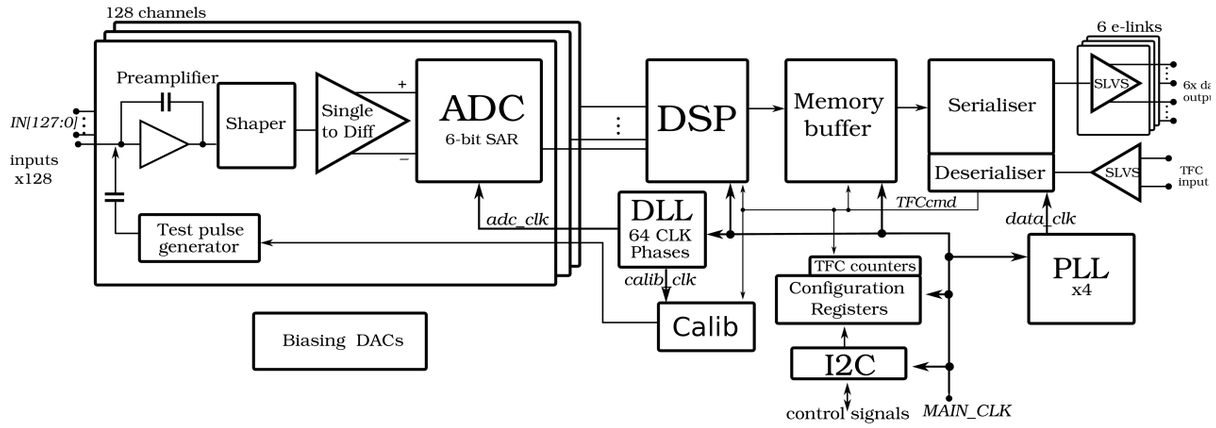
ADCs in front-end electronics



K. Swientek
The SALT, a 128-Channel Readout ASIC for Upstream Tracker in the Upgraded LHCb Experiment
https://indico.cern.ch/event/608587/contributions/2614090/

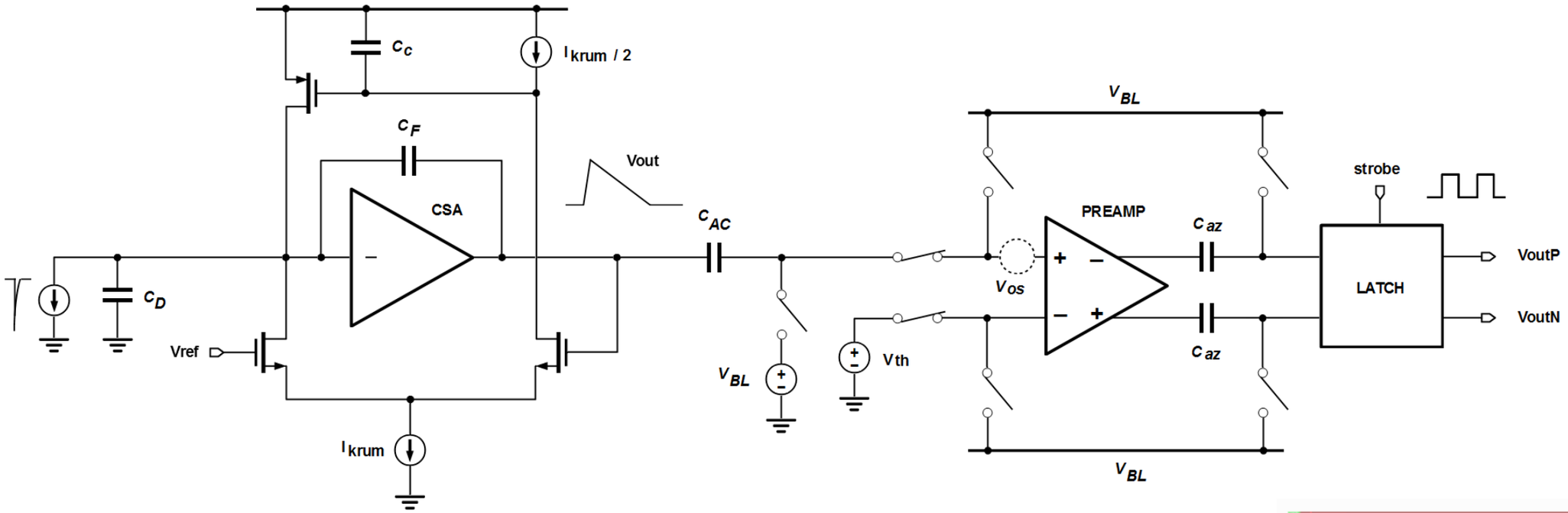




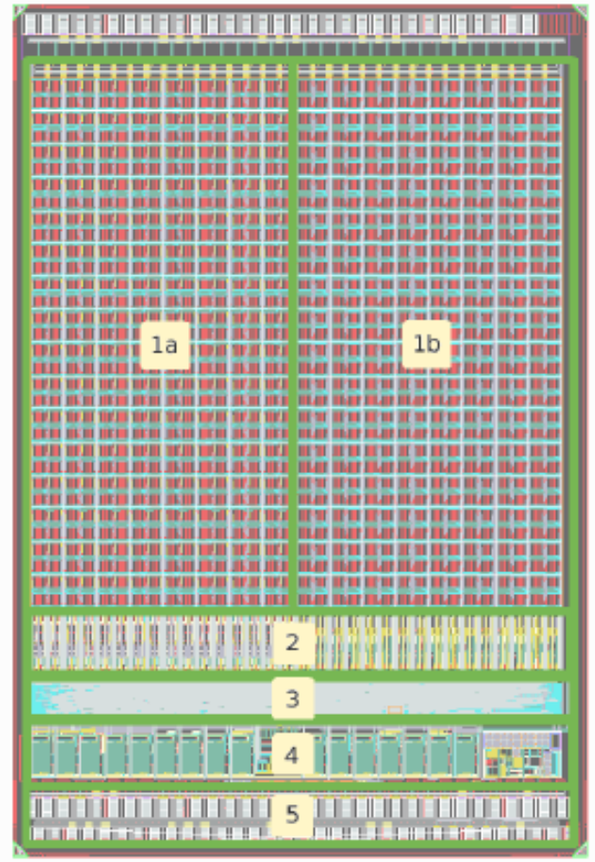


- 6 bit ADC
- designed for LHCb upgrade
- 128 channels

Compact electronics



- Part of a pixel front-end demonstrator chip
- INFN project CHIPIX65, funded by INFN R&D committee
- Fully compatible with HL-LHC specifications (50 um x 50 um pixels)
- Full regional logic, two different front-ends (synch and asynch)
- Synchronous front-end with:
  - Dynamic offset compensation (no calibration DACs)
  - Fast charge digitisation with ToT
- Front-end size: 35 um x 35 um



Compact front-end electronics

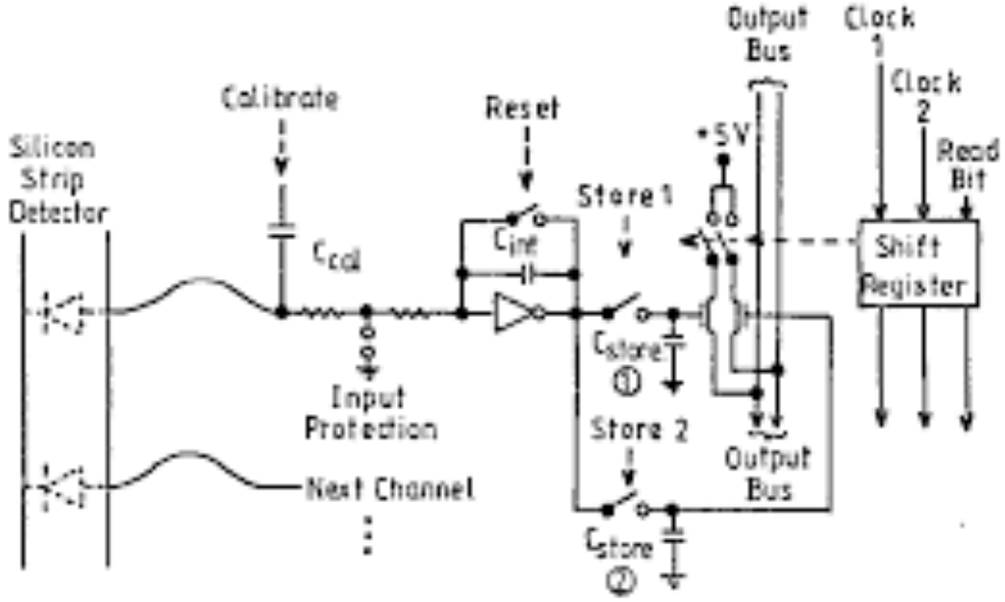
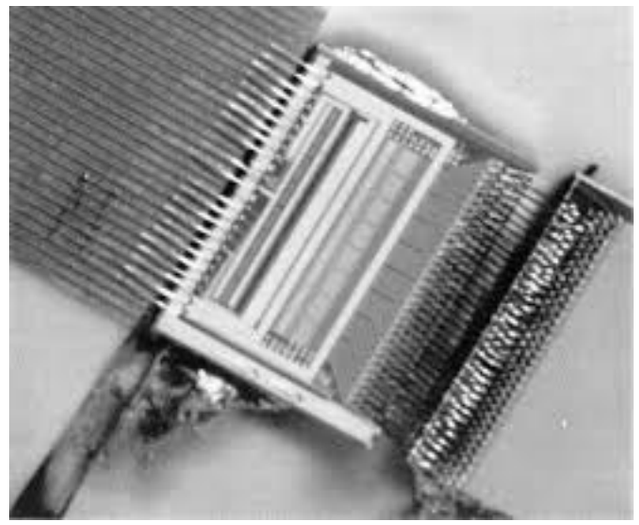
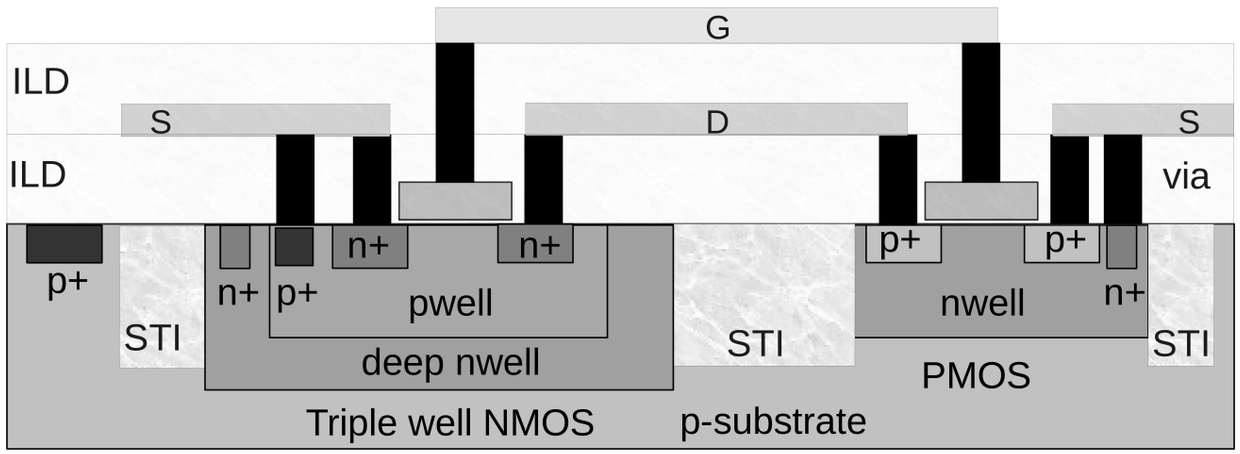


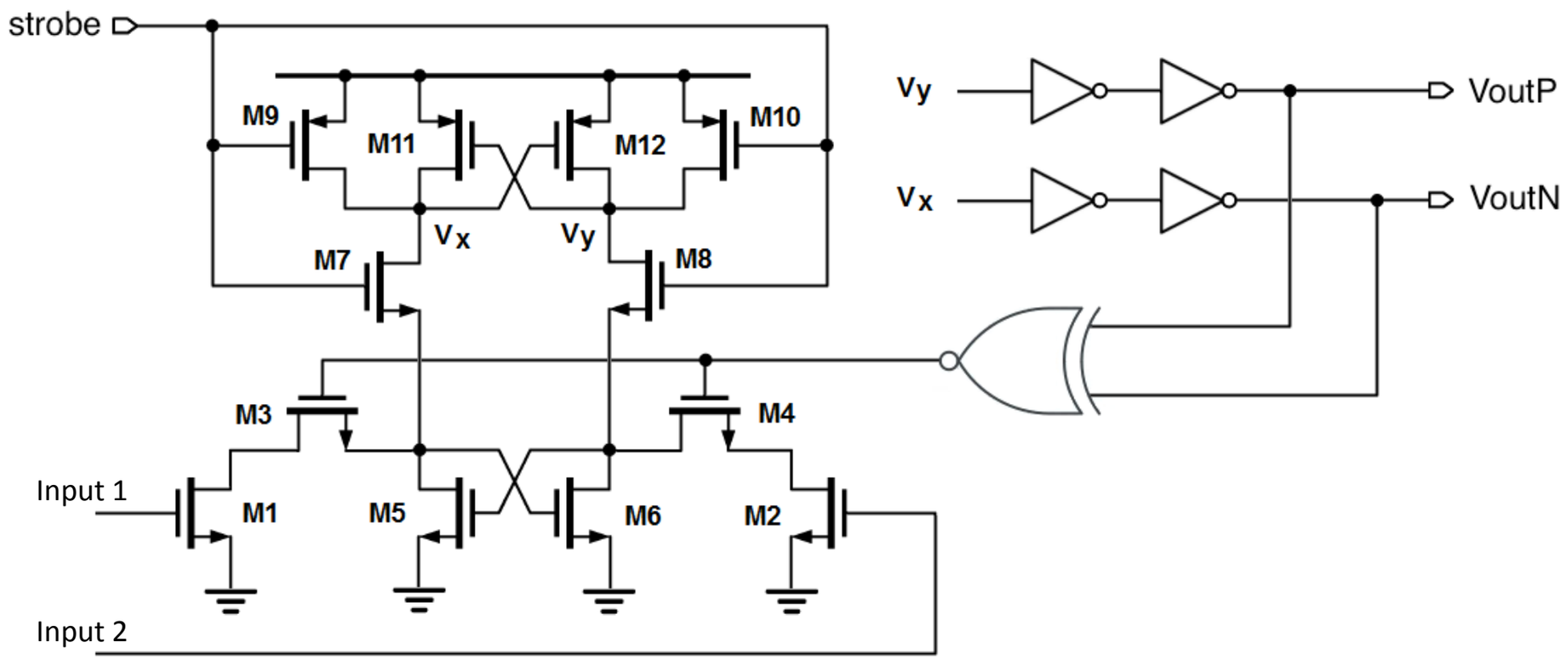
Figure 1. Block diagram of the Microplex circuit

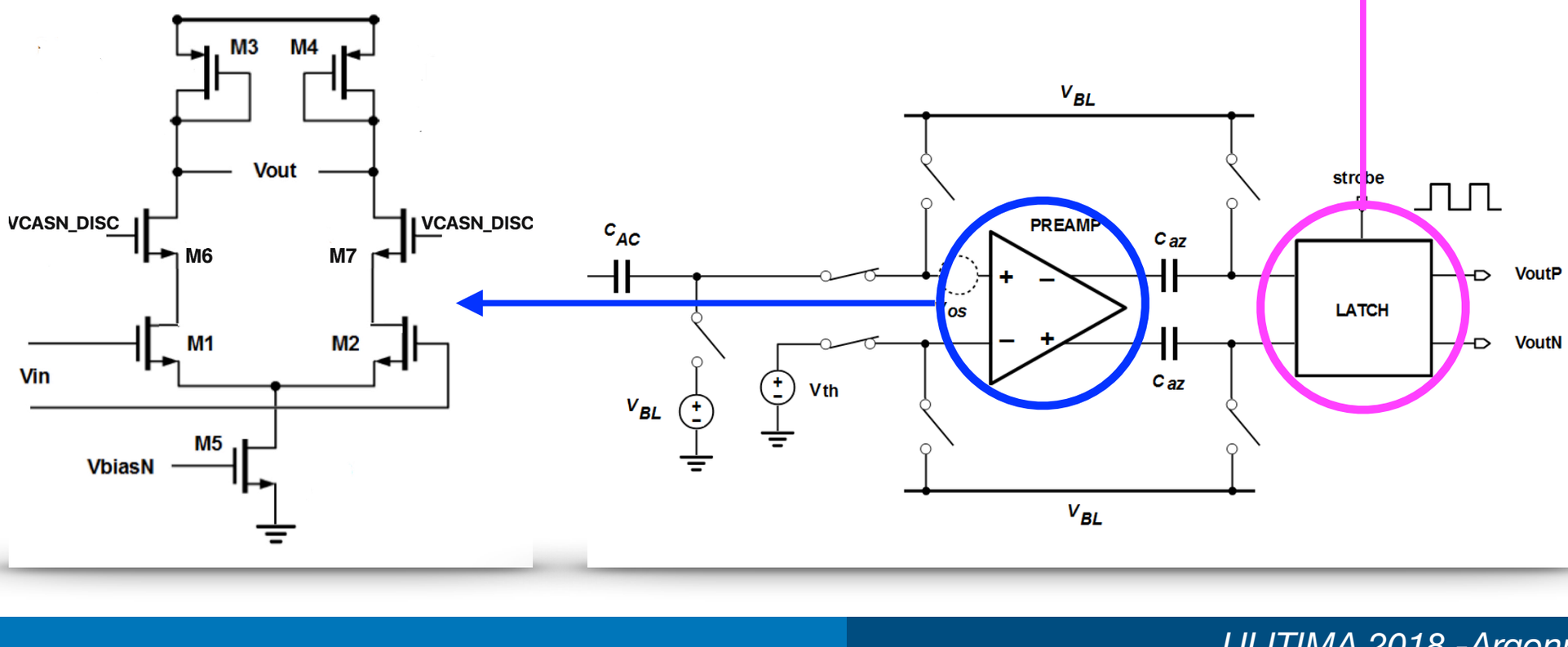


- First front-end electronics for radiation detectors based on switched-capacitor circuits
- Maximum charge stored in a transistor in 65 nm about 5% of that of a 350 nm
- Charge injection greatly reduced
- Advanced isolation features

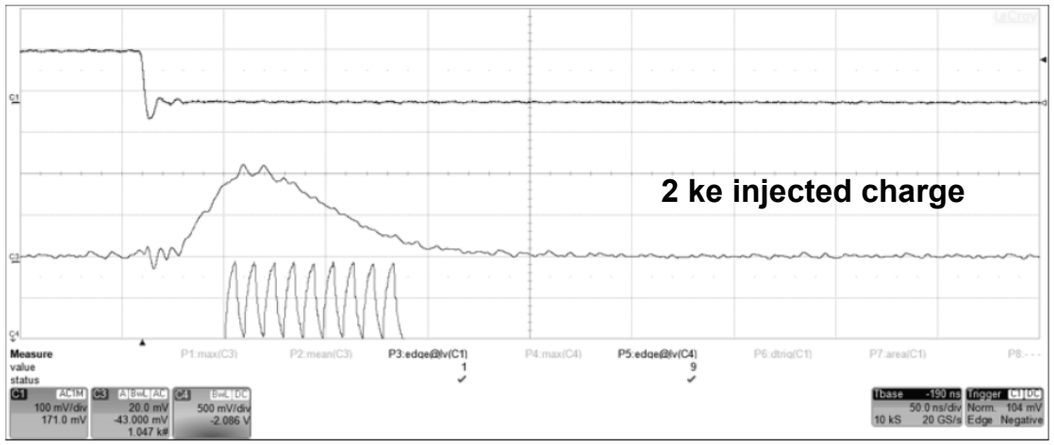


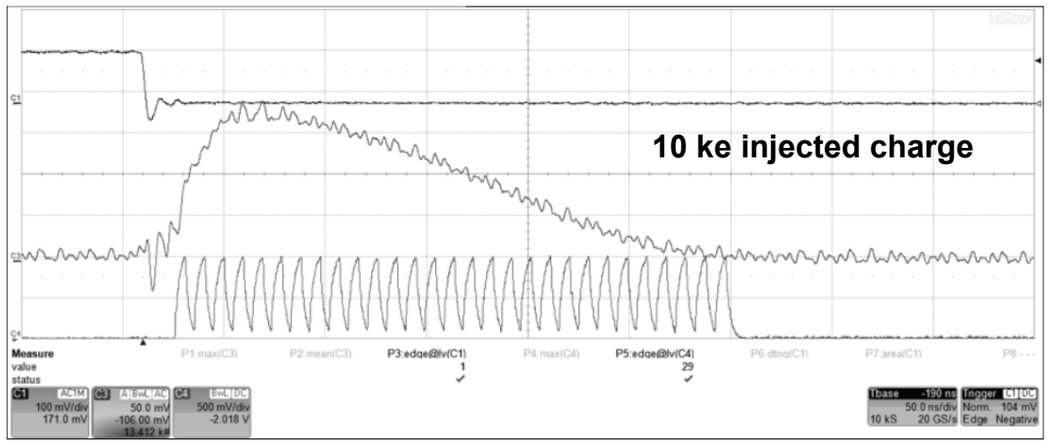
Some circuit details

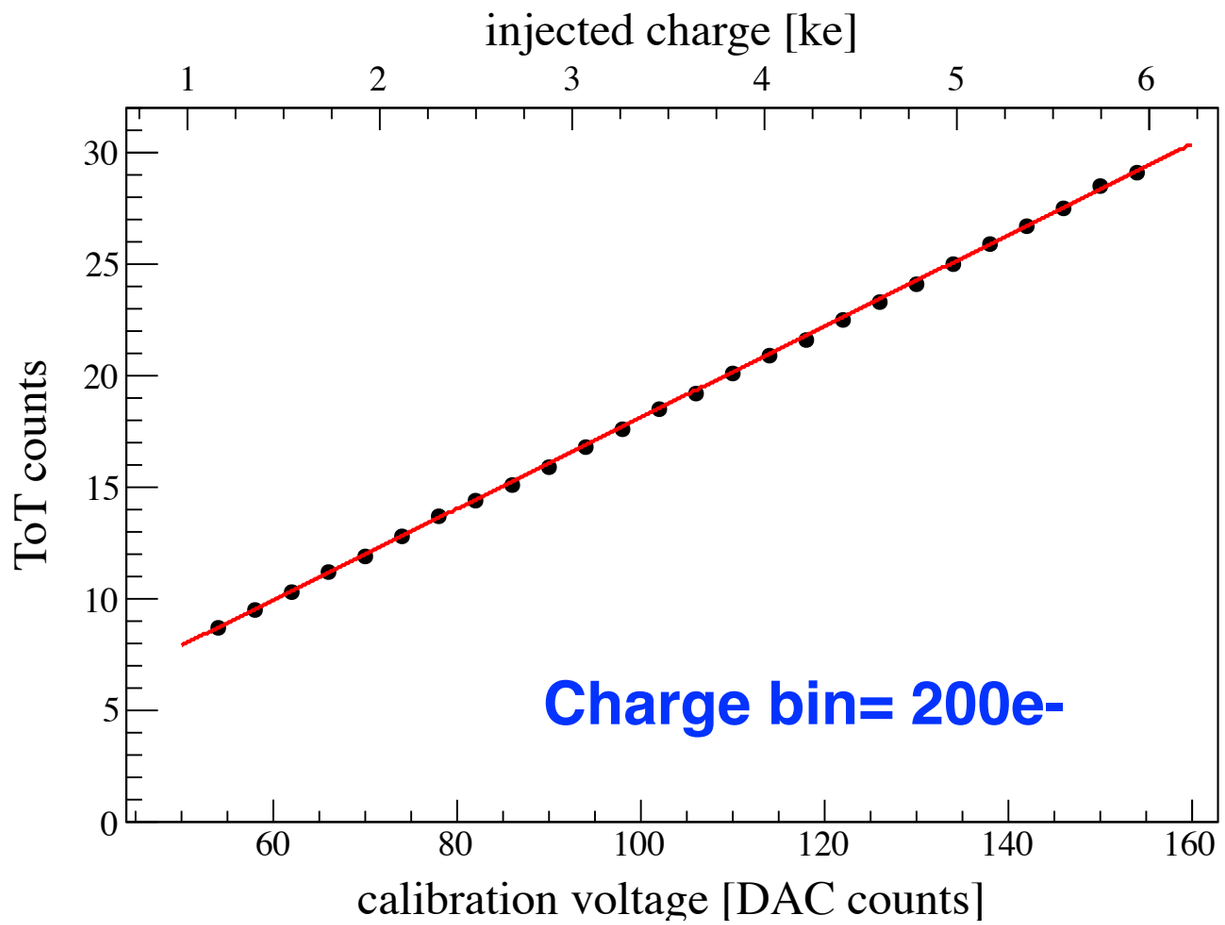




ToT linearity

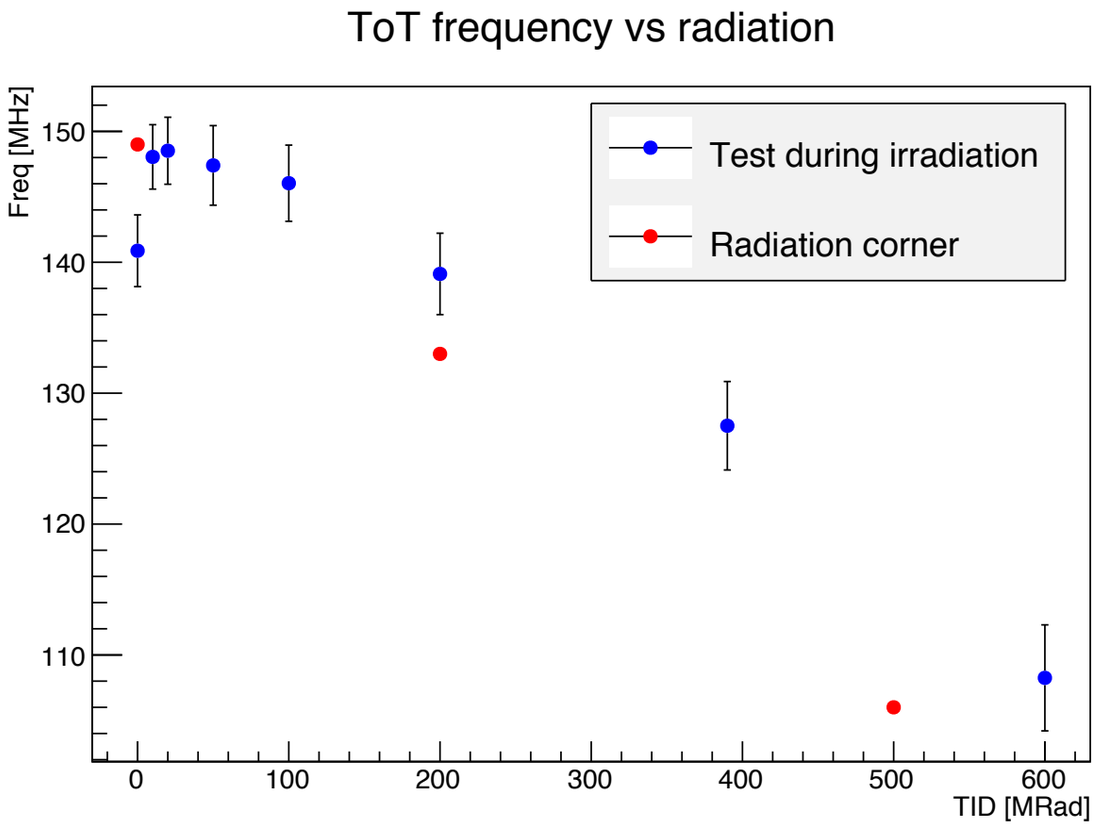


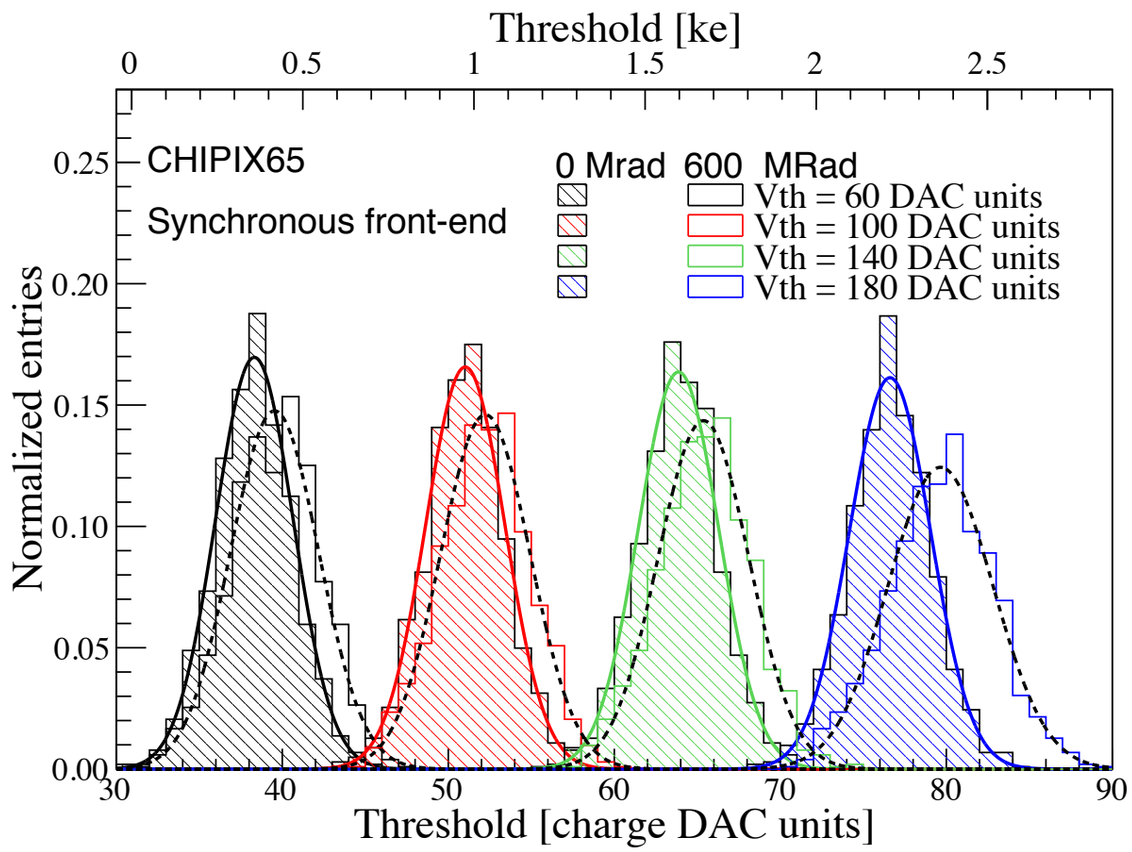




- Oscillation frequency: 320 MHz, but could be significantly higher (>> 1 GHz)
- Power primarily depends on number of cycles
- Number of bits primarily depends on data storage
- Mostly digital, good for scaling

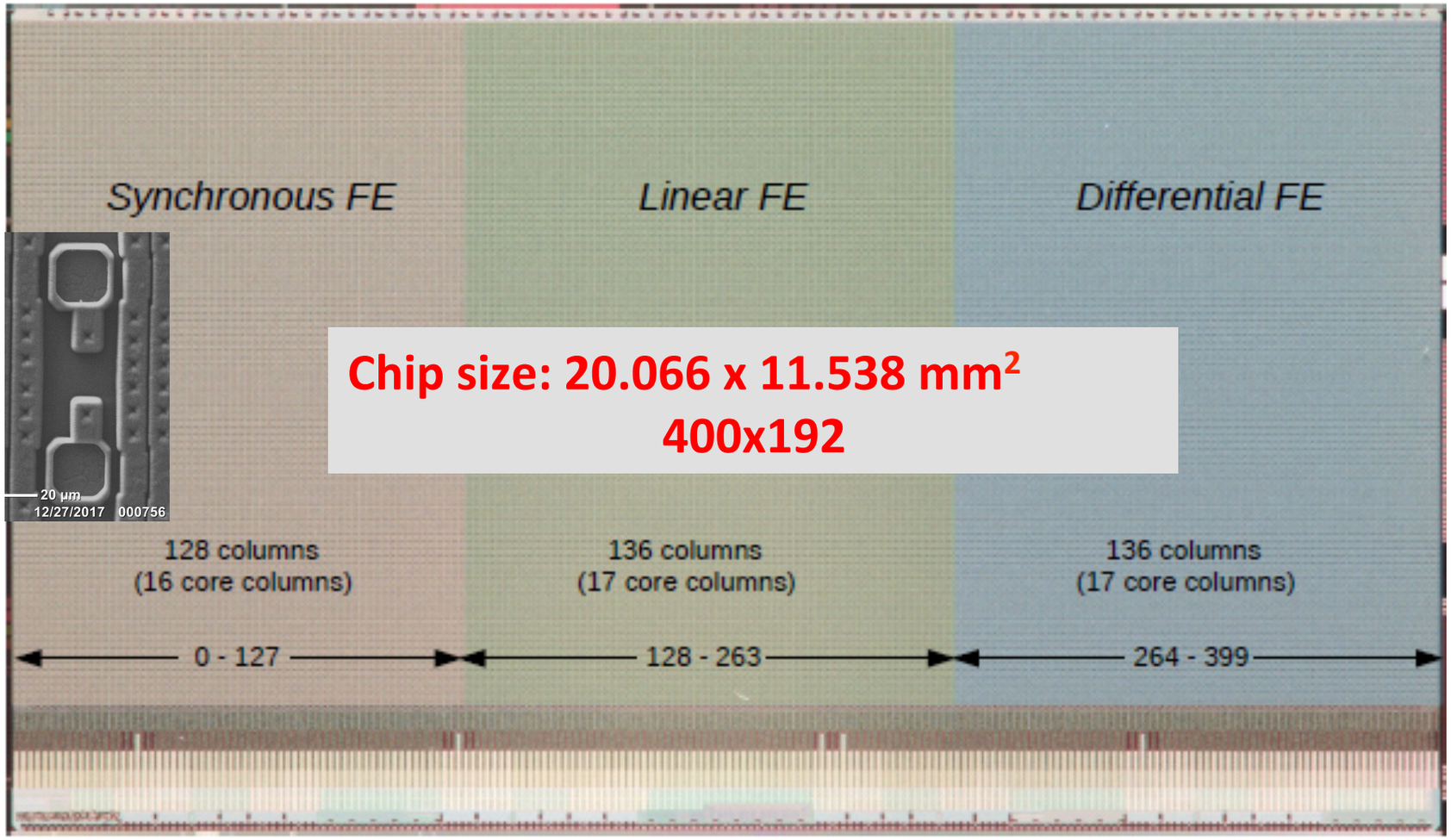
Radiation performance





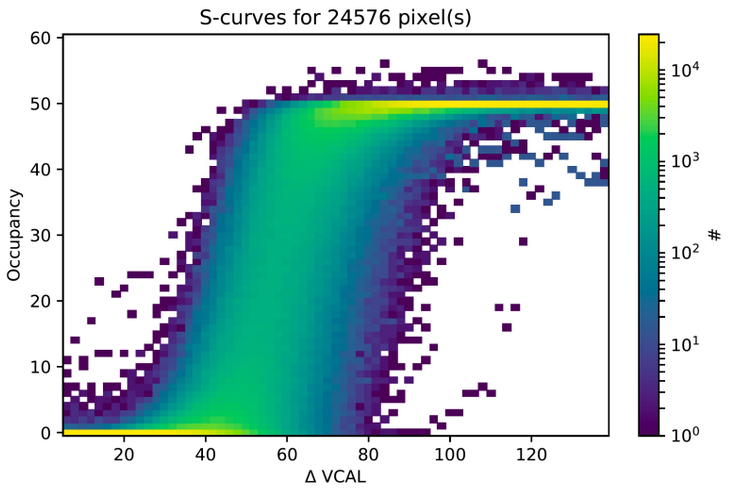
- **Some degradation, but still functional after 600 Mrad**

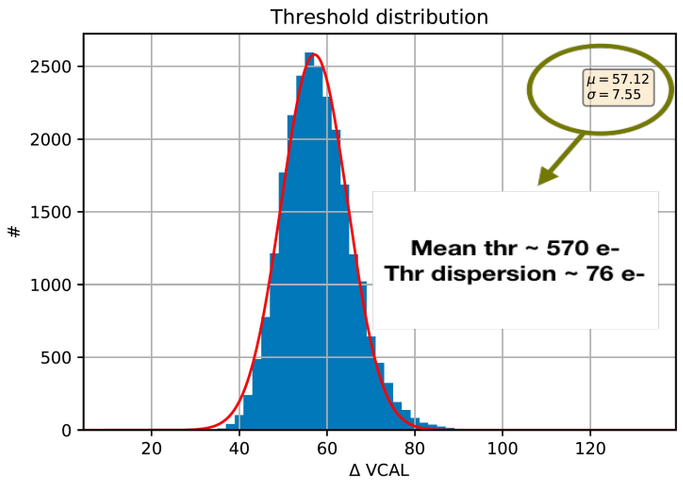
Test on larger system

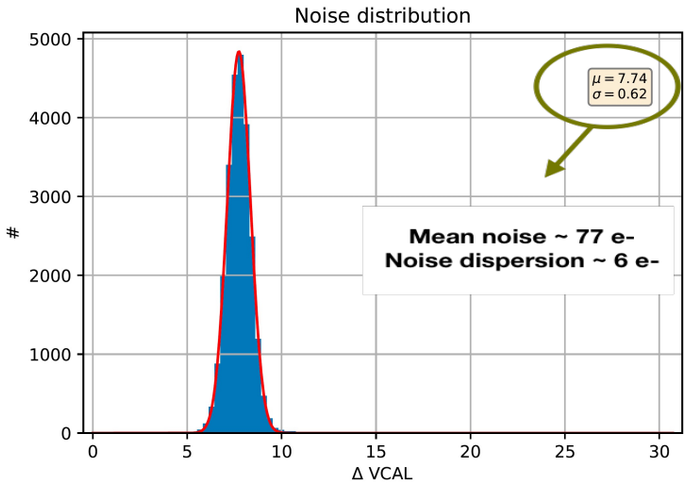


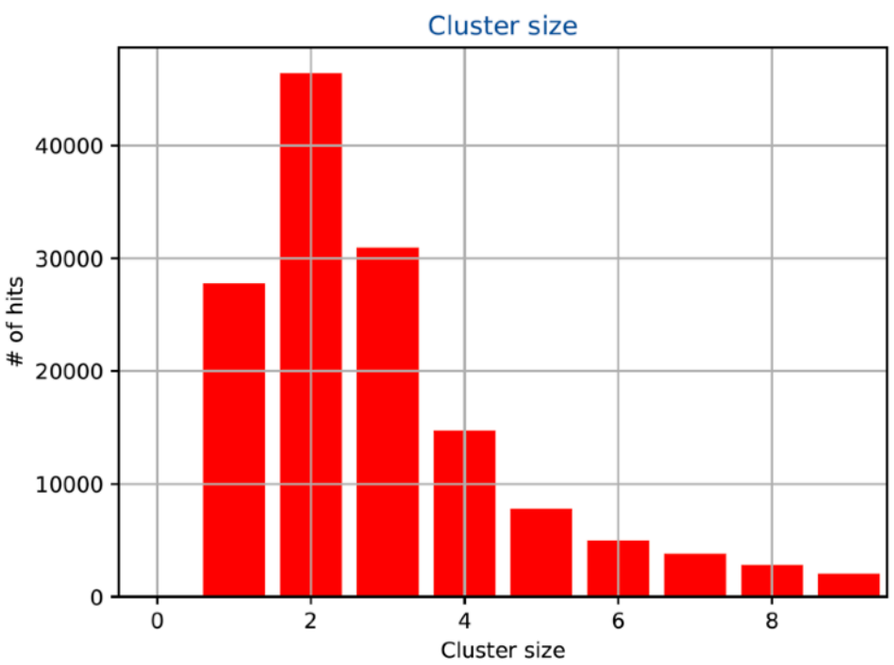
- One of three front-end concepts tested in the RD53A chip

Some performance



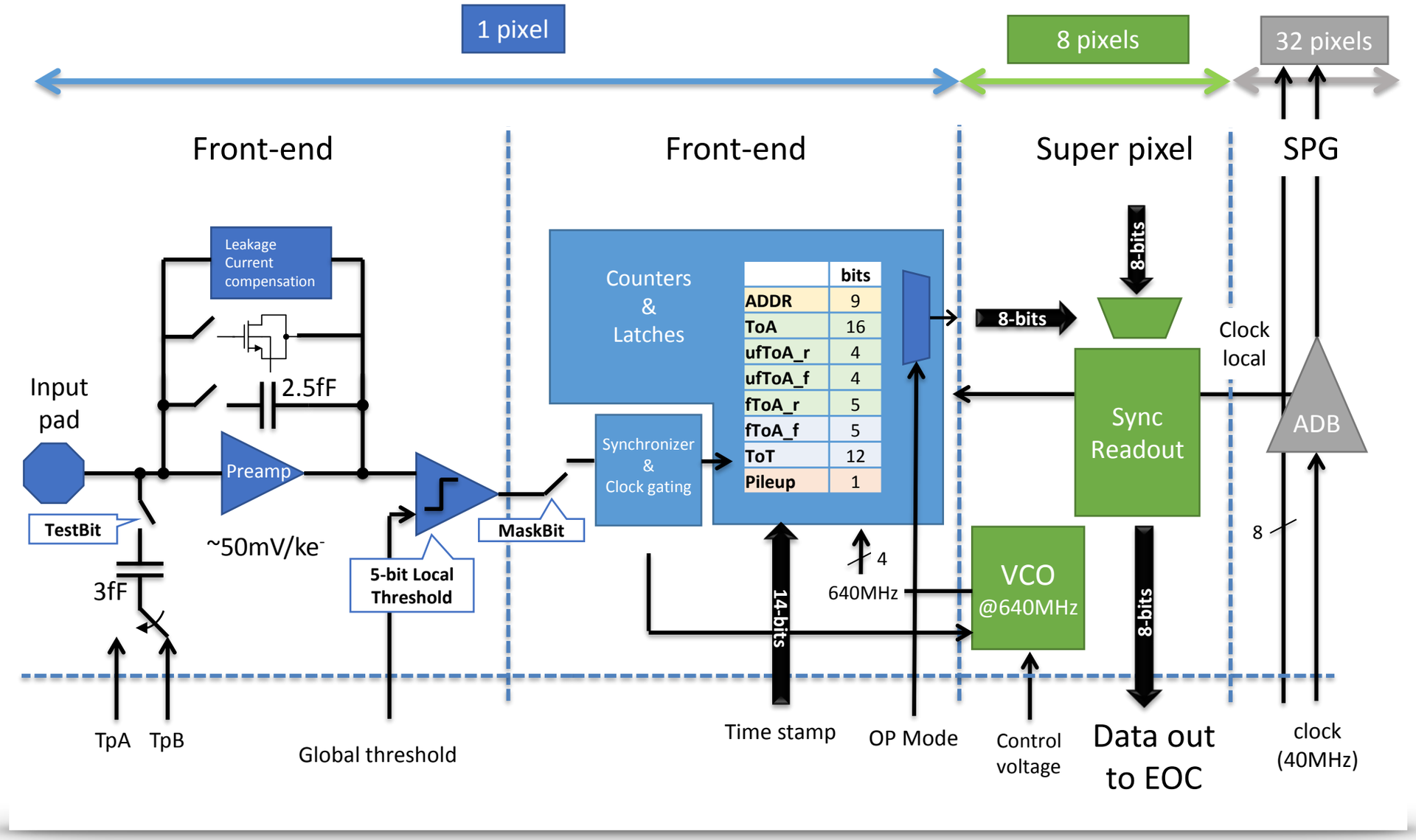






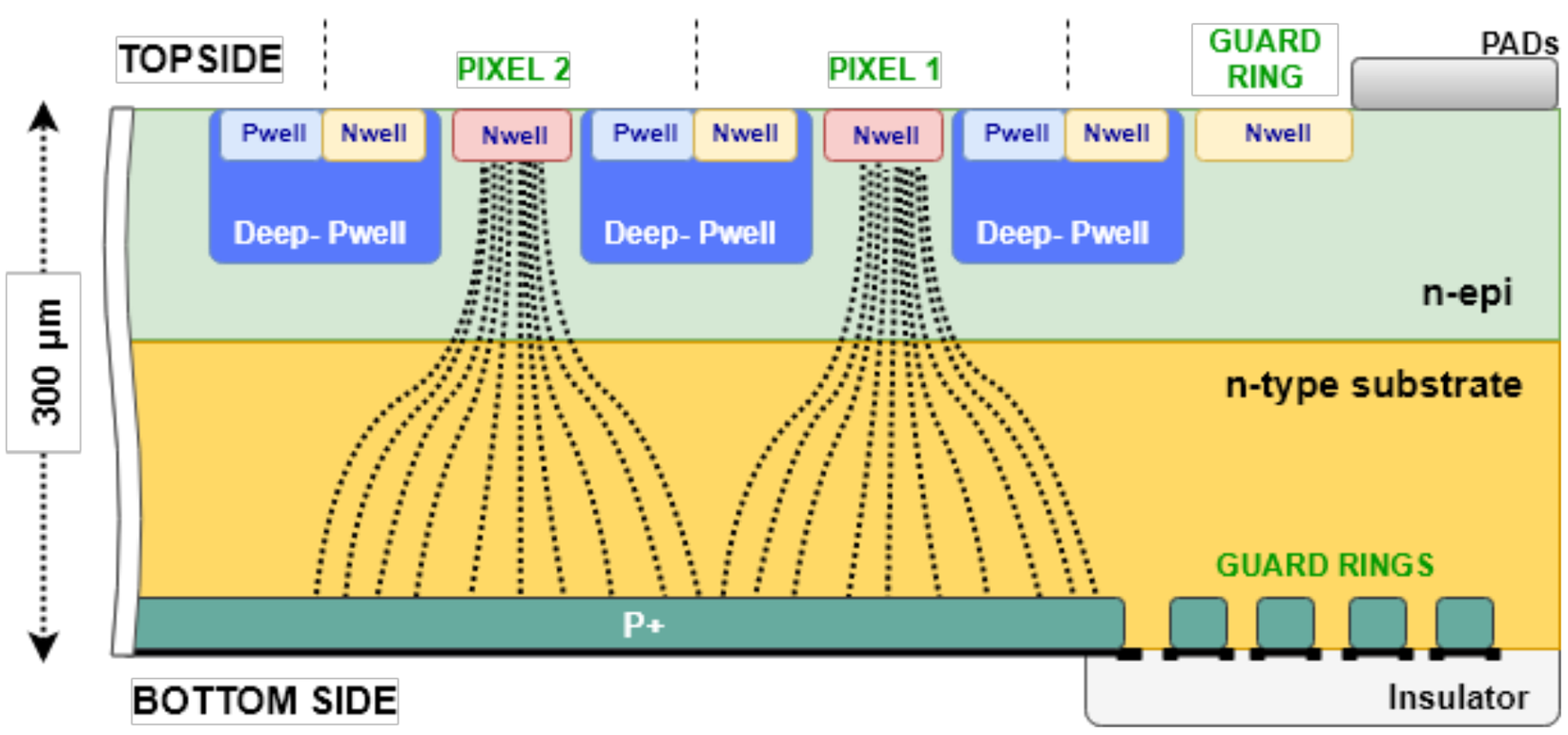
Pixels with fast oscillator: another example

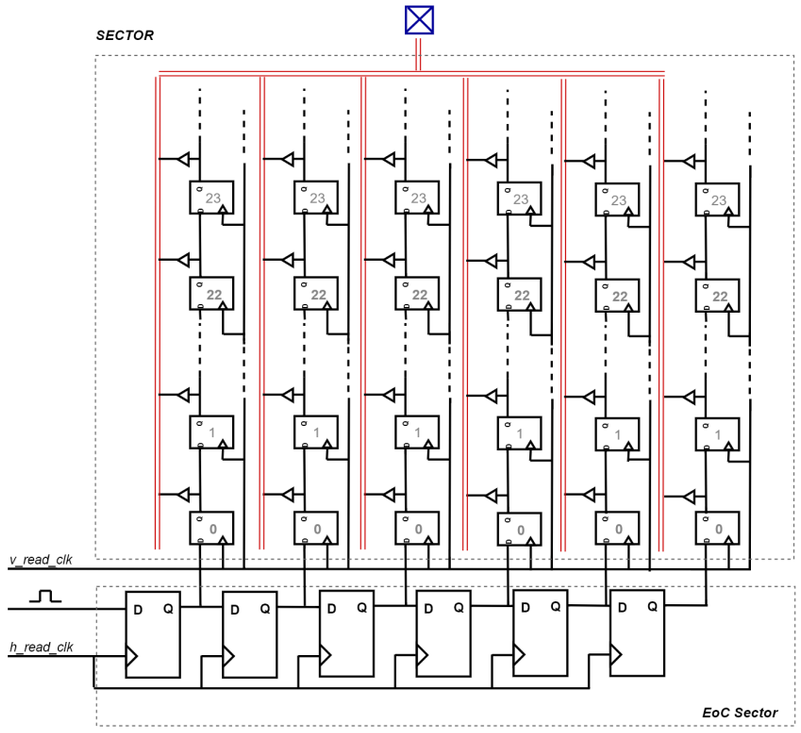
X. Llopart: Towards a new generation of Medipix and Timepix ASICs
https://indico.cern.ch/event/688153/contributions/2964568/- FEE 2018 meeting, Jouvence, Canada)

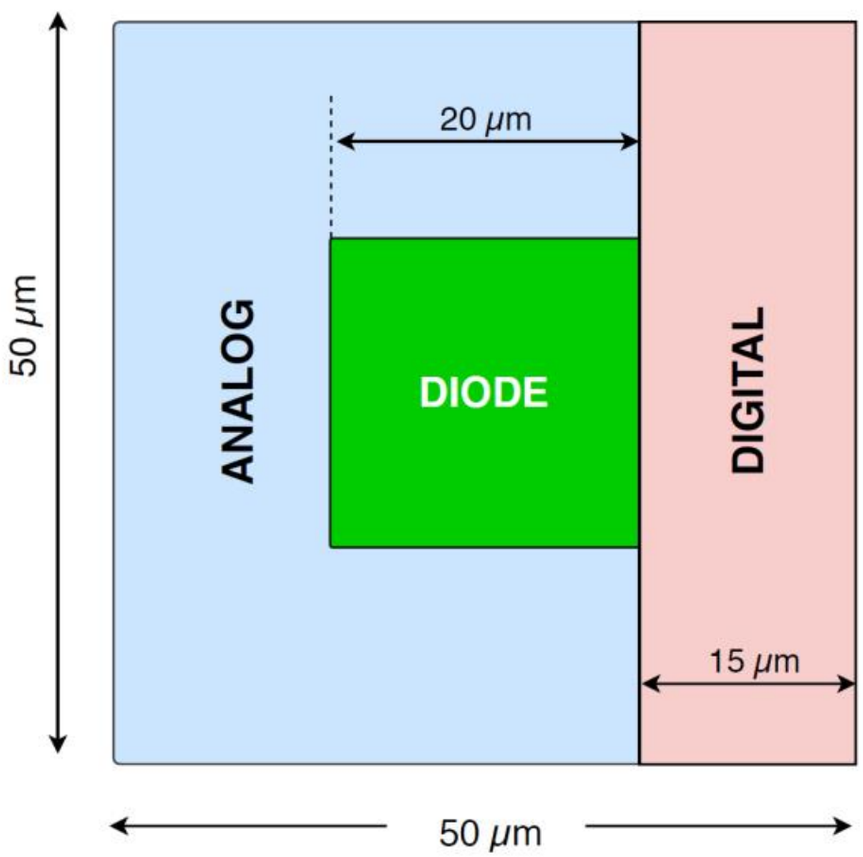


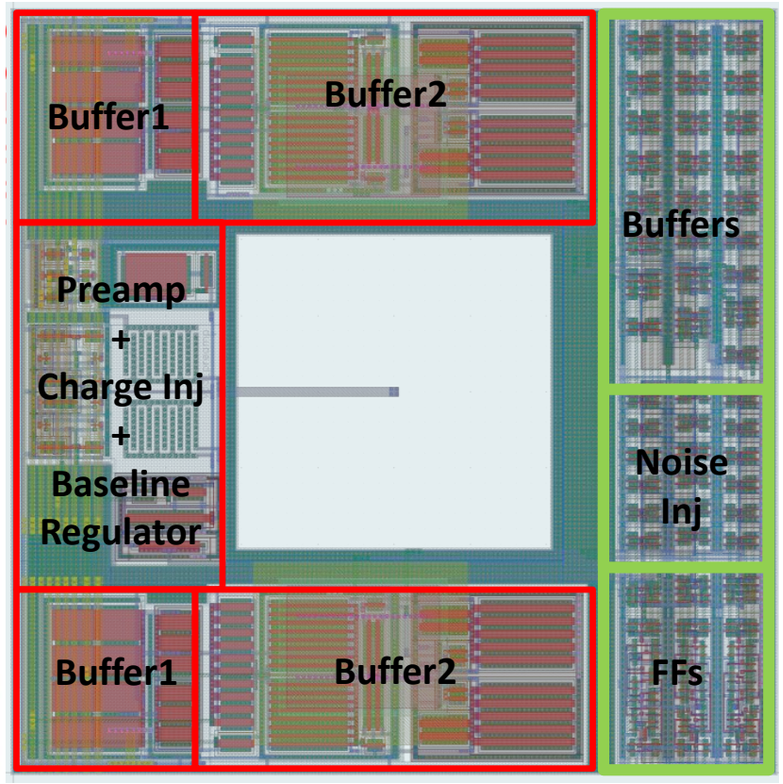
- Fast TDC/oscillators can also be shared among pixels (e.g. Timepix3, Timepix4)

Fully depleted MAPS







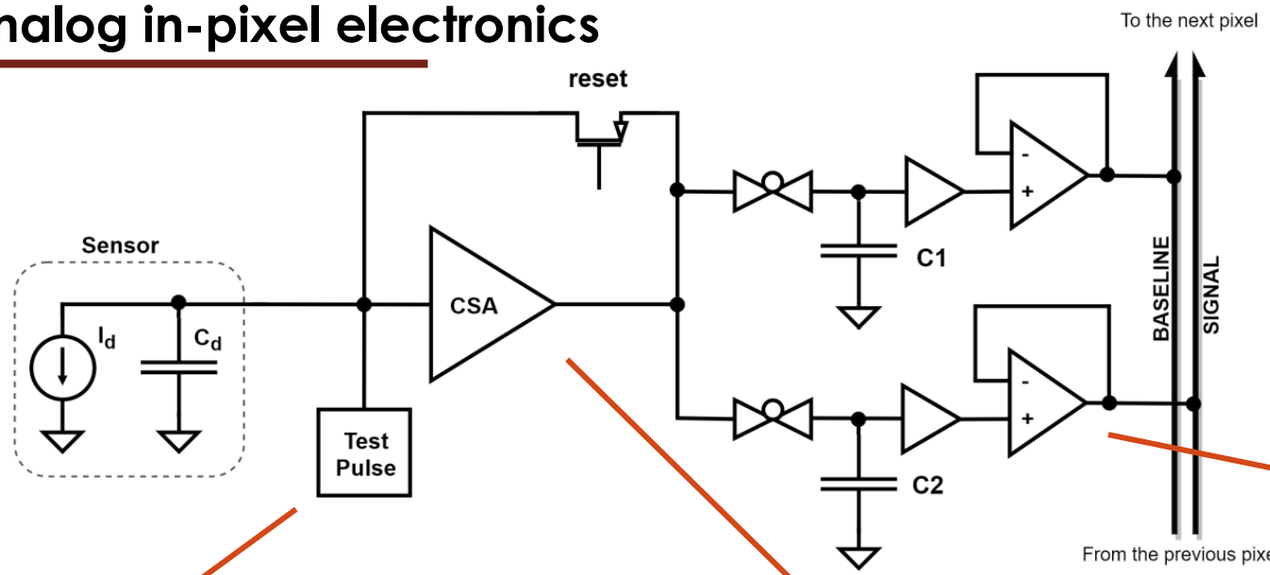


Sensors with Embedded Electronics Design (SEED)

Supported by INFN R&D Committee

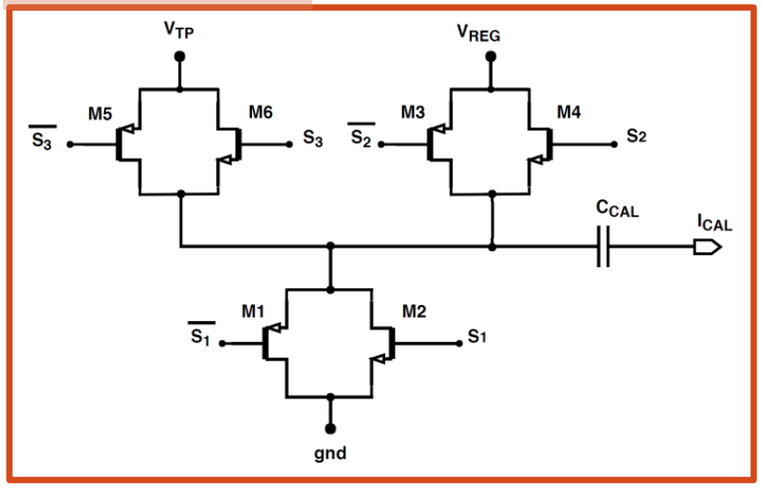
Analog electronics

Analog in-pixel electronics

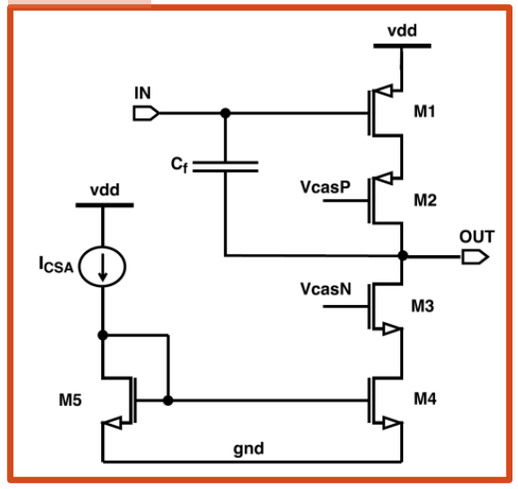


- Analog gain = $1/C_f$
- Analog buffer based on a switched o amp amplifier → high dynamic range
- The calibration system: test pulse injection and baseline regulation

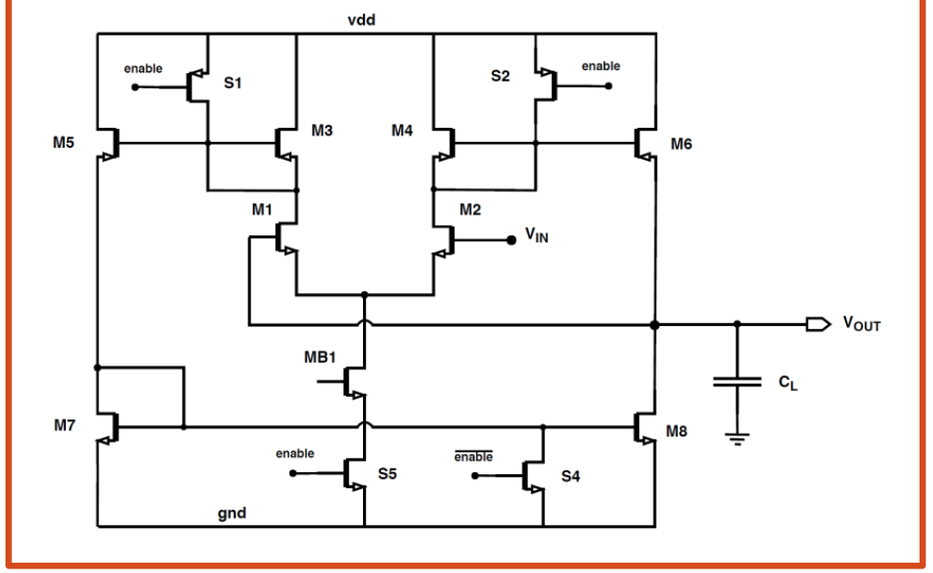
Calibration



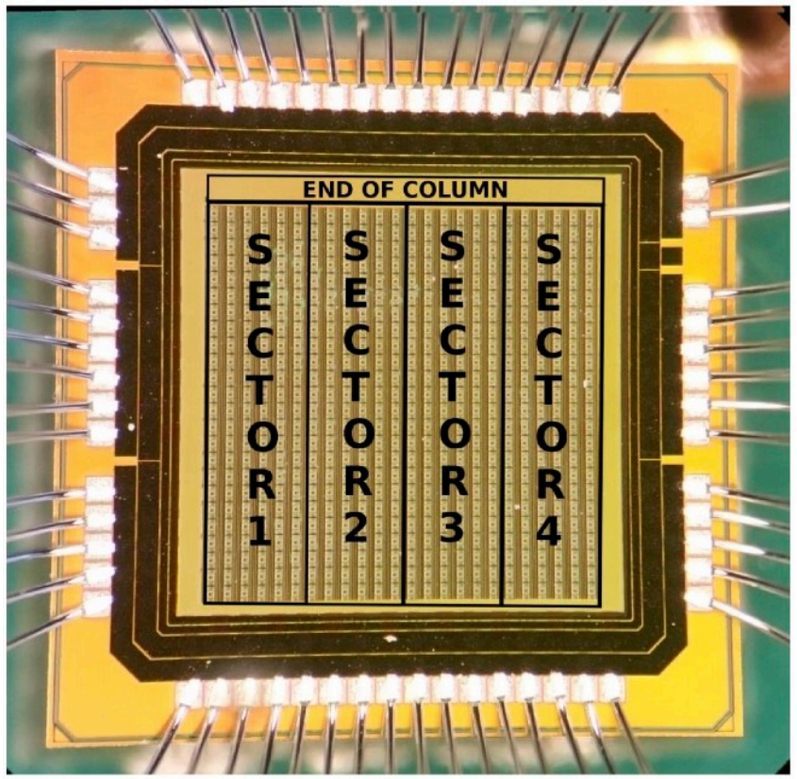
CSA

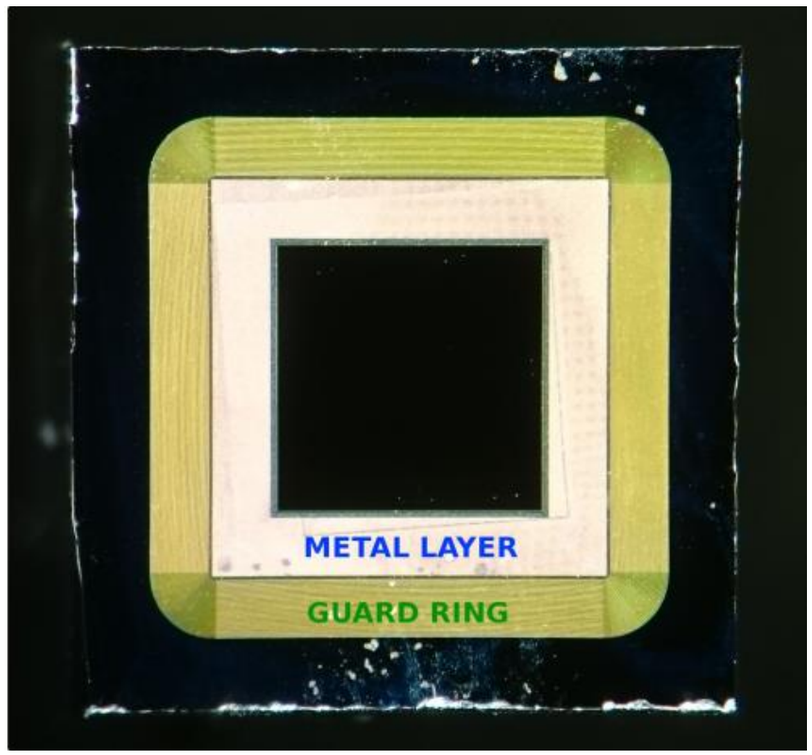


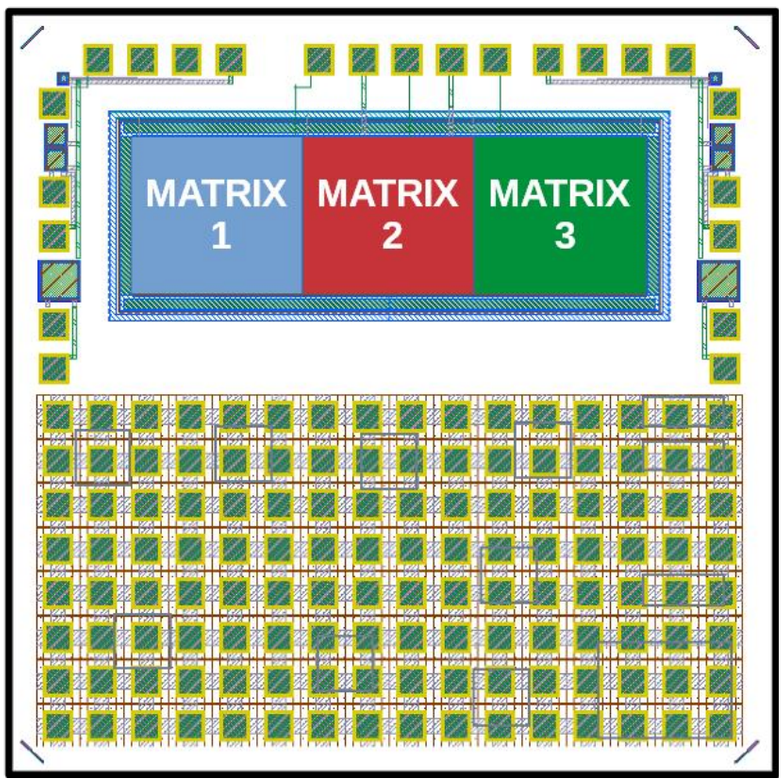
Analog buffer

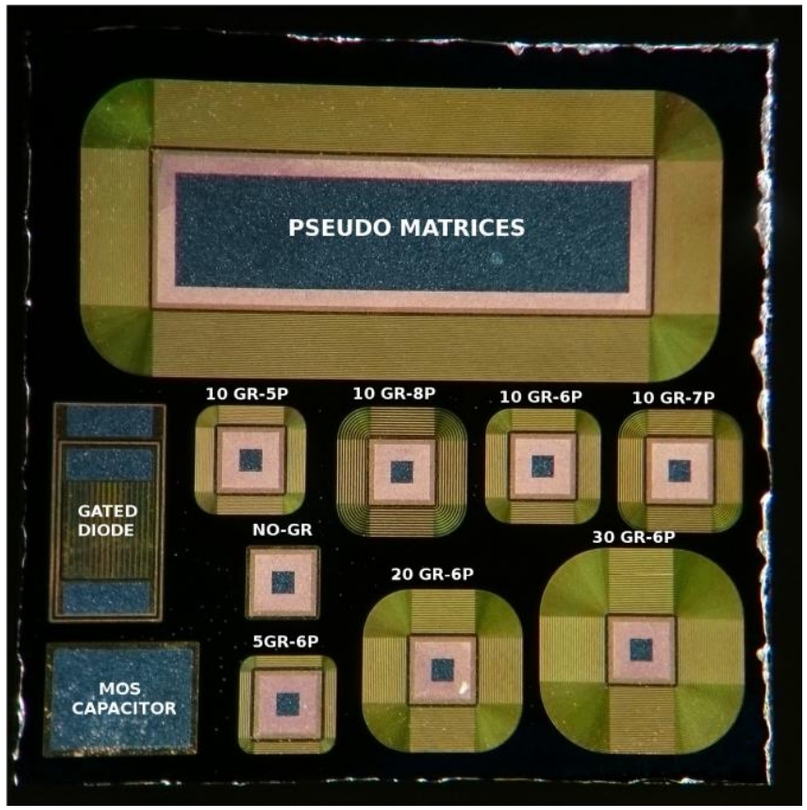


Test structures

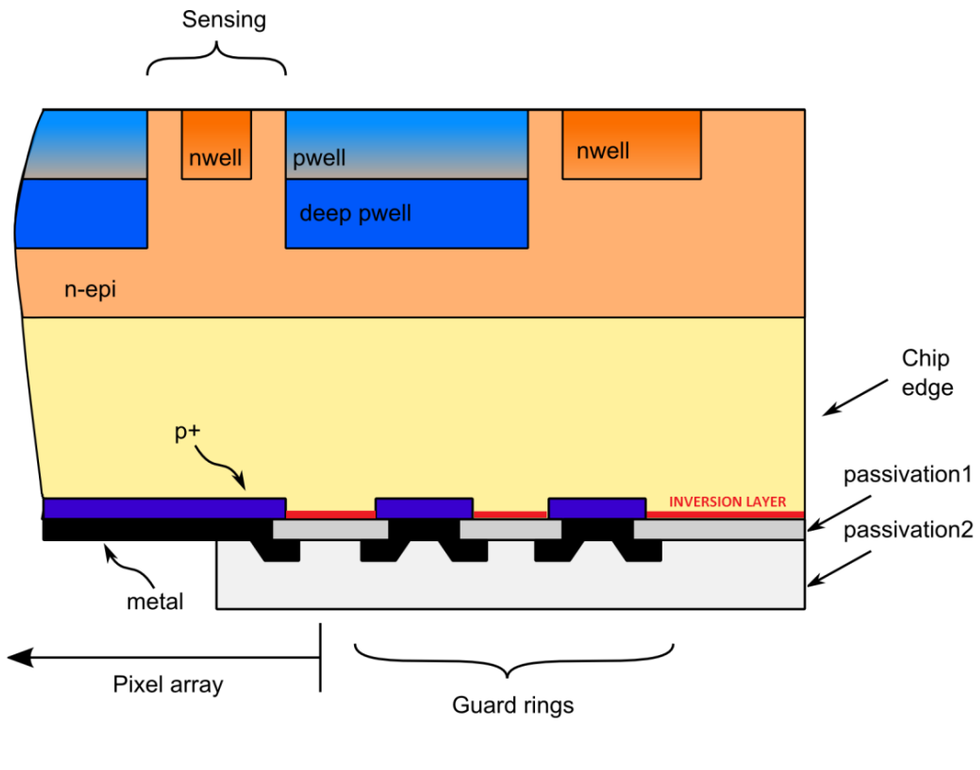


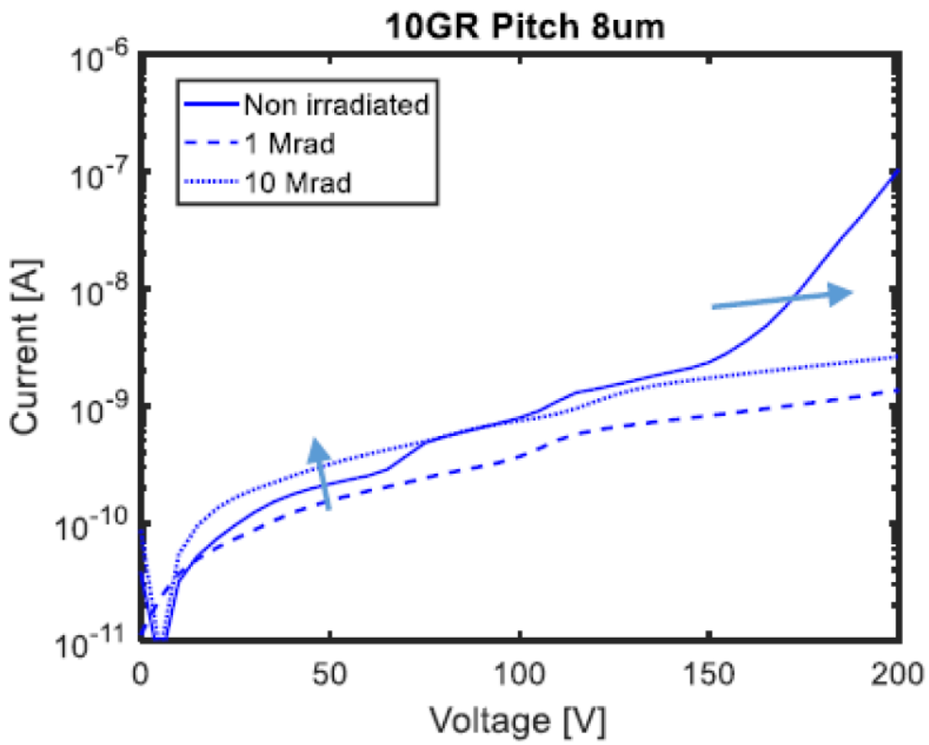






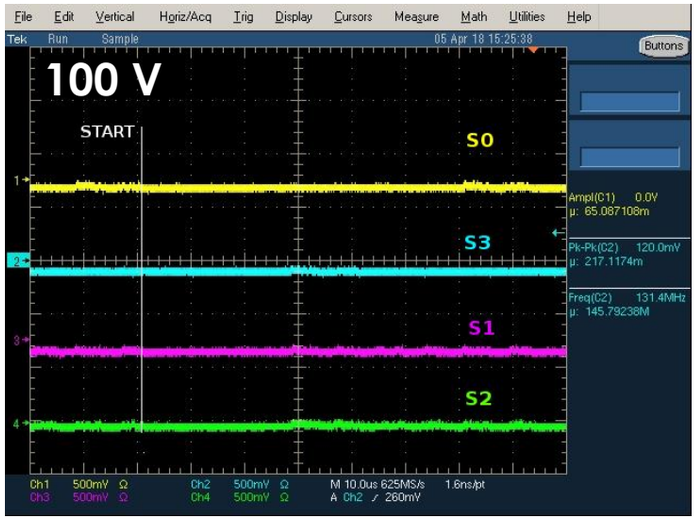
Some results

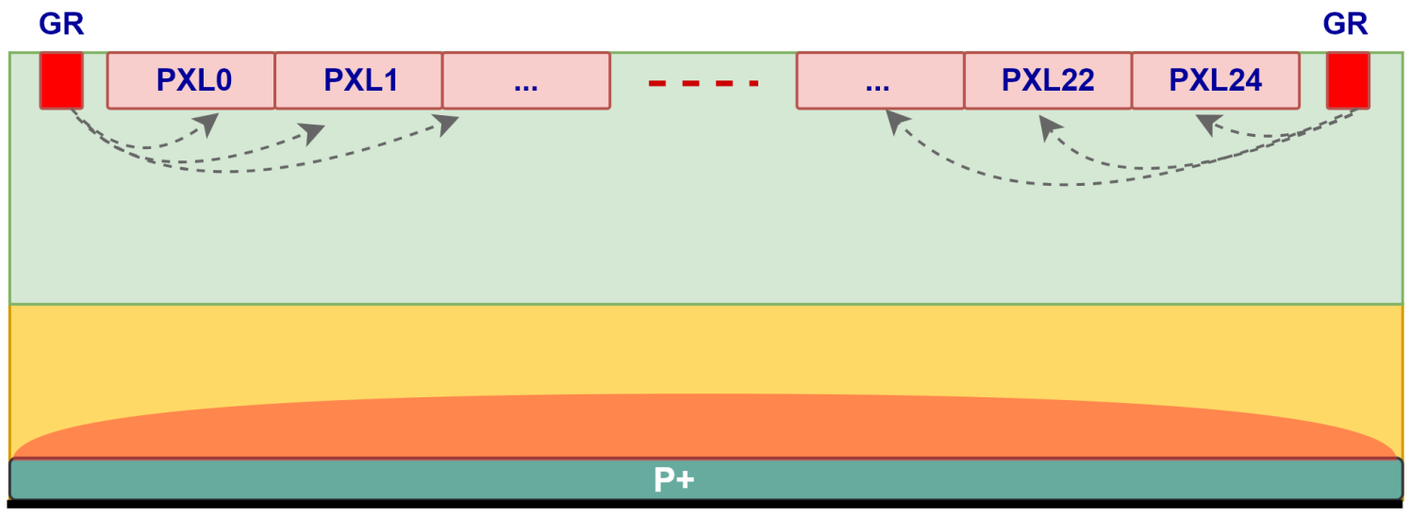


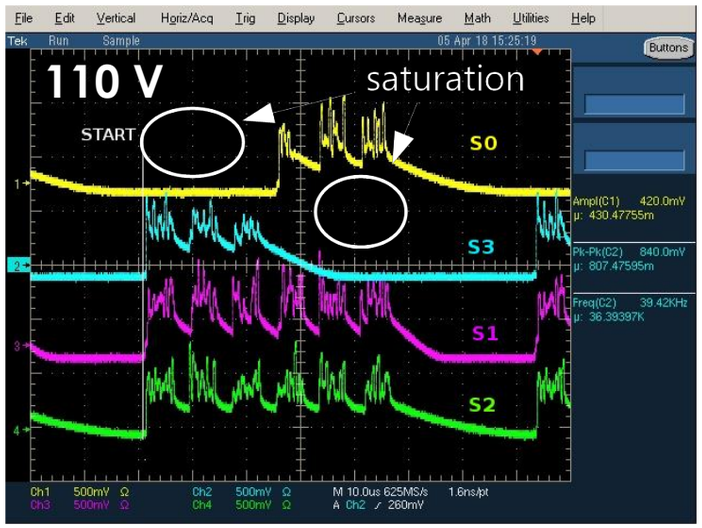


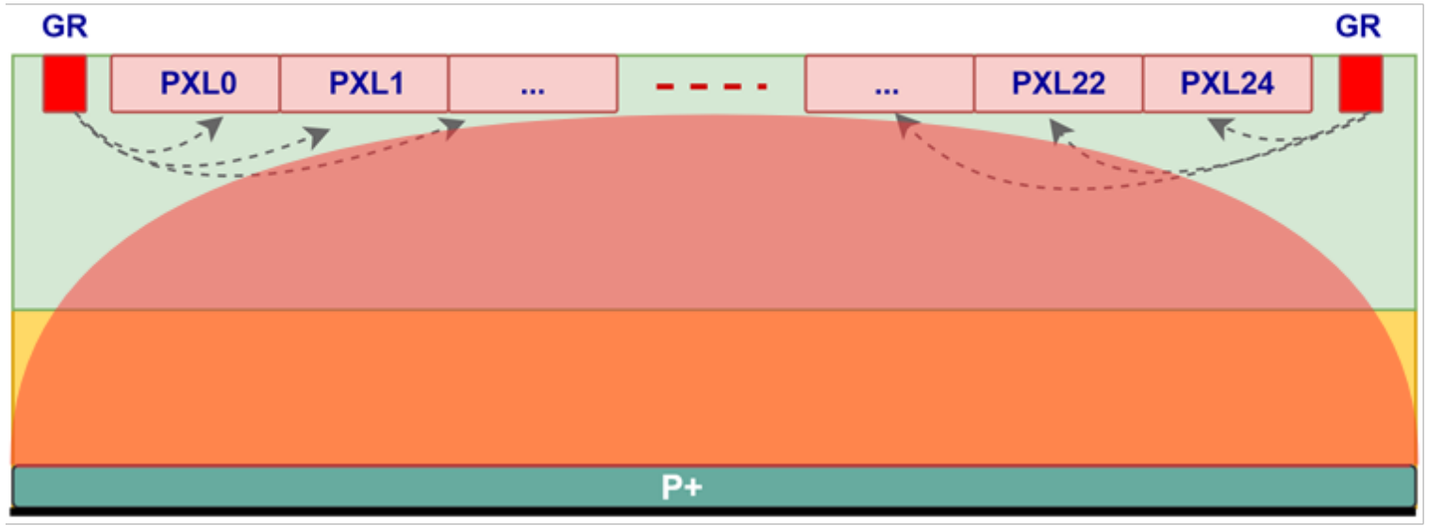
- Several test structures with different guard-ring design
- Inversion layer may compromise guard-rings
- Can be partially cured with irradiation
- Cause understood and fixed in the next release just delivered by the foundry

Non-depleted matrix

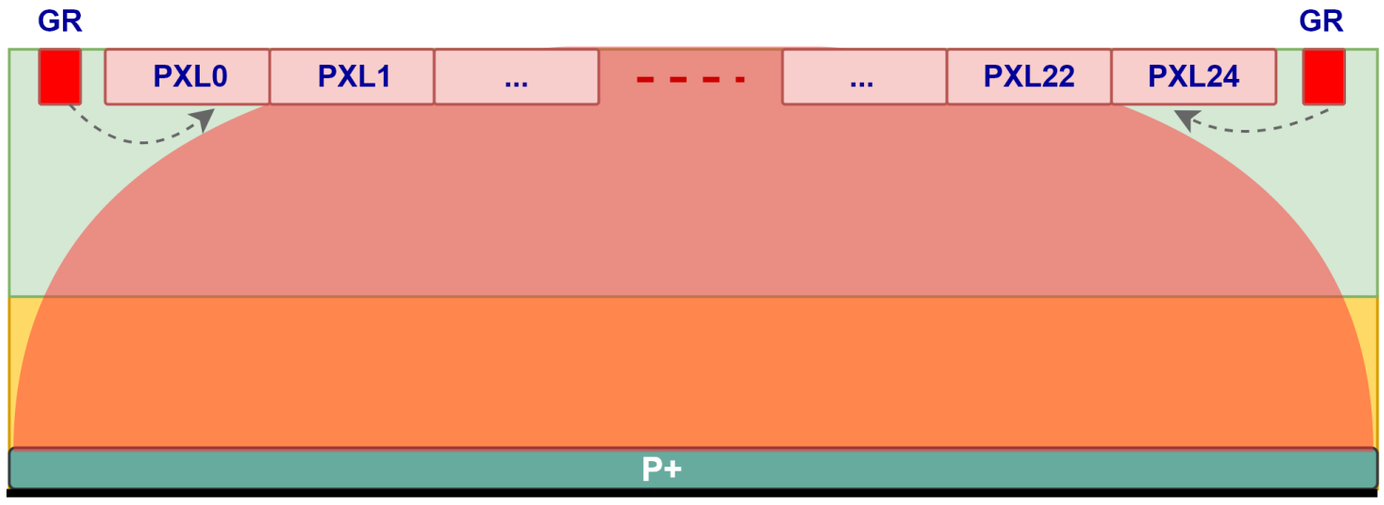


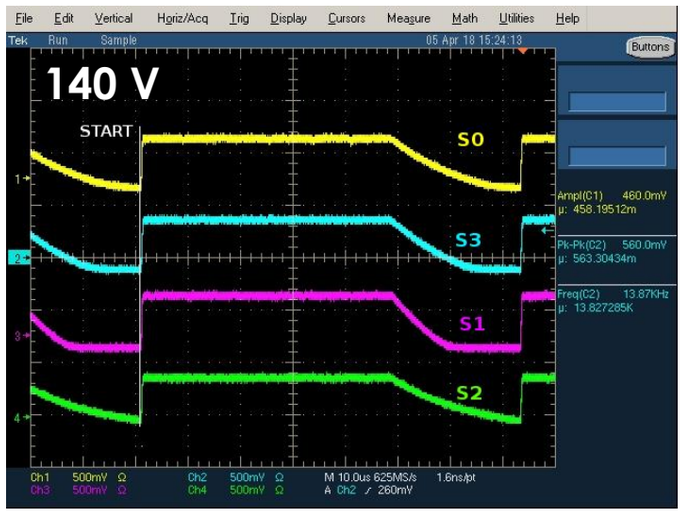


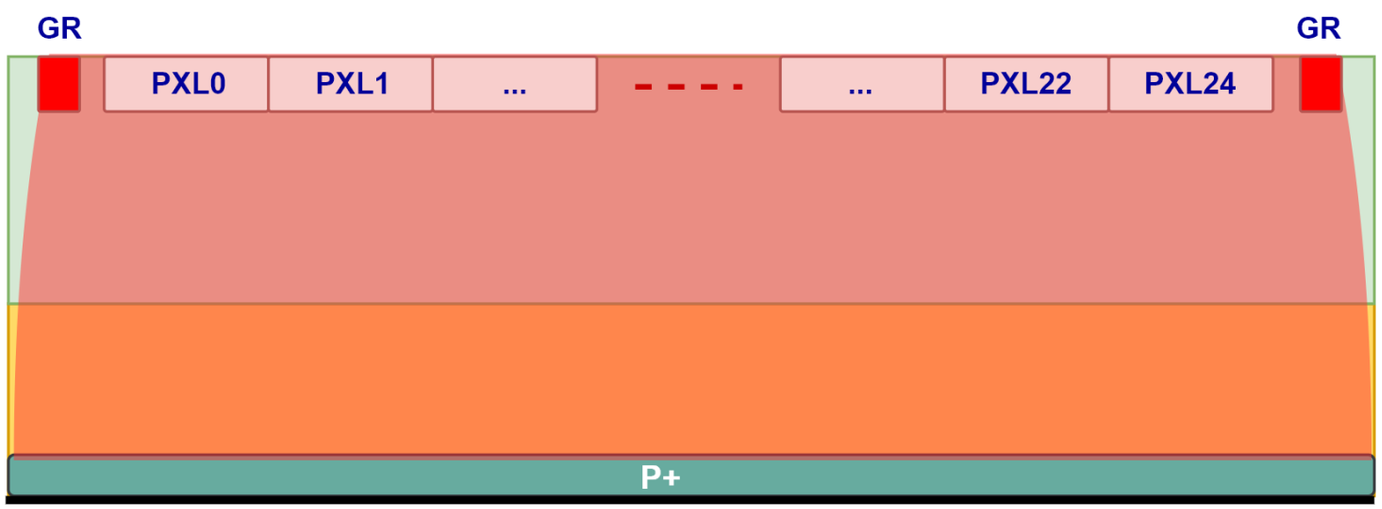




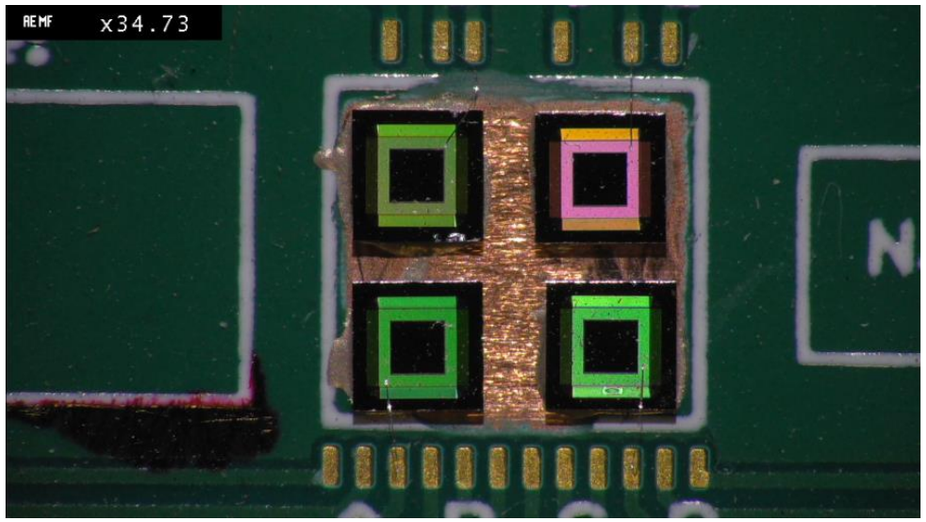
Fully depleted matrix



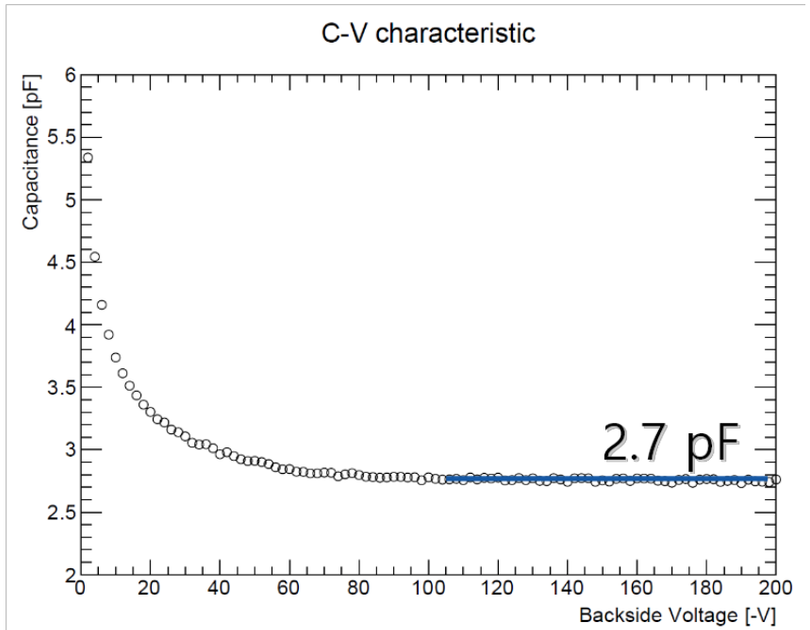


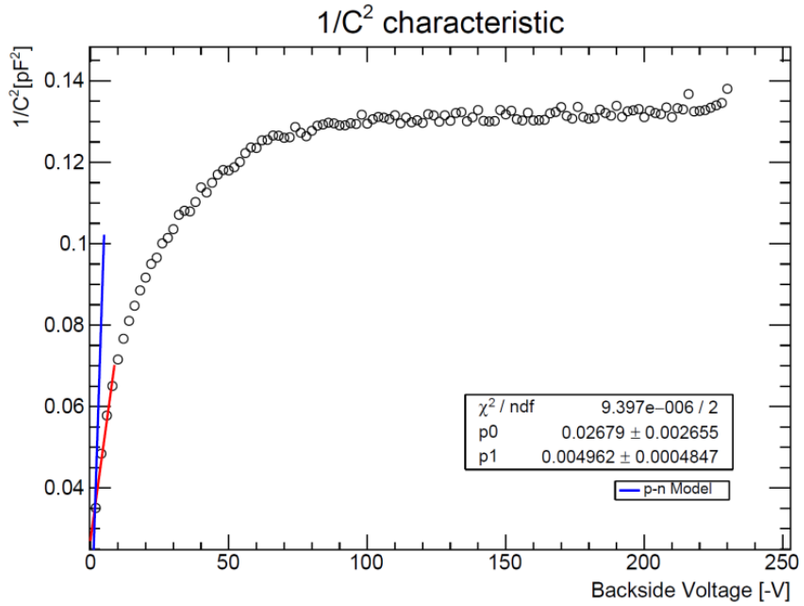


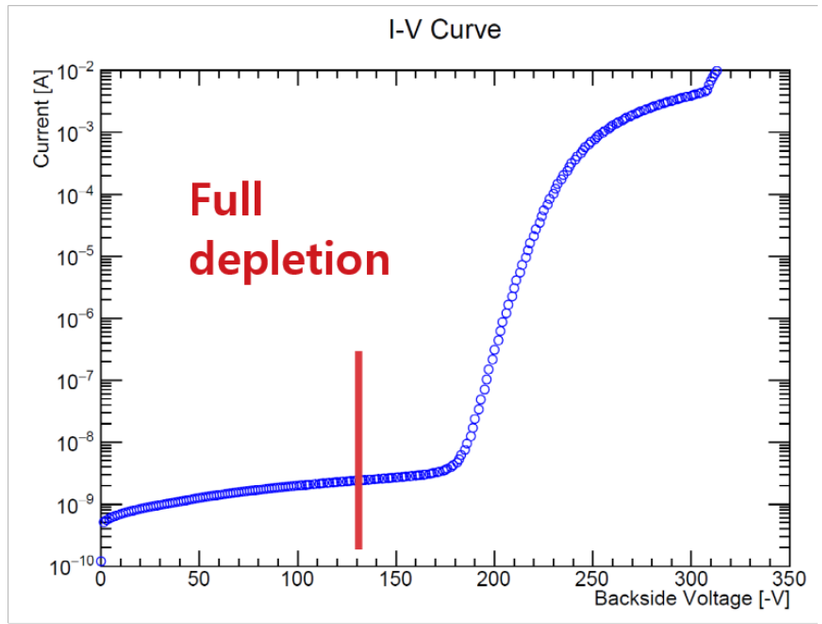
C-V and I-V curve



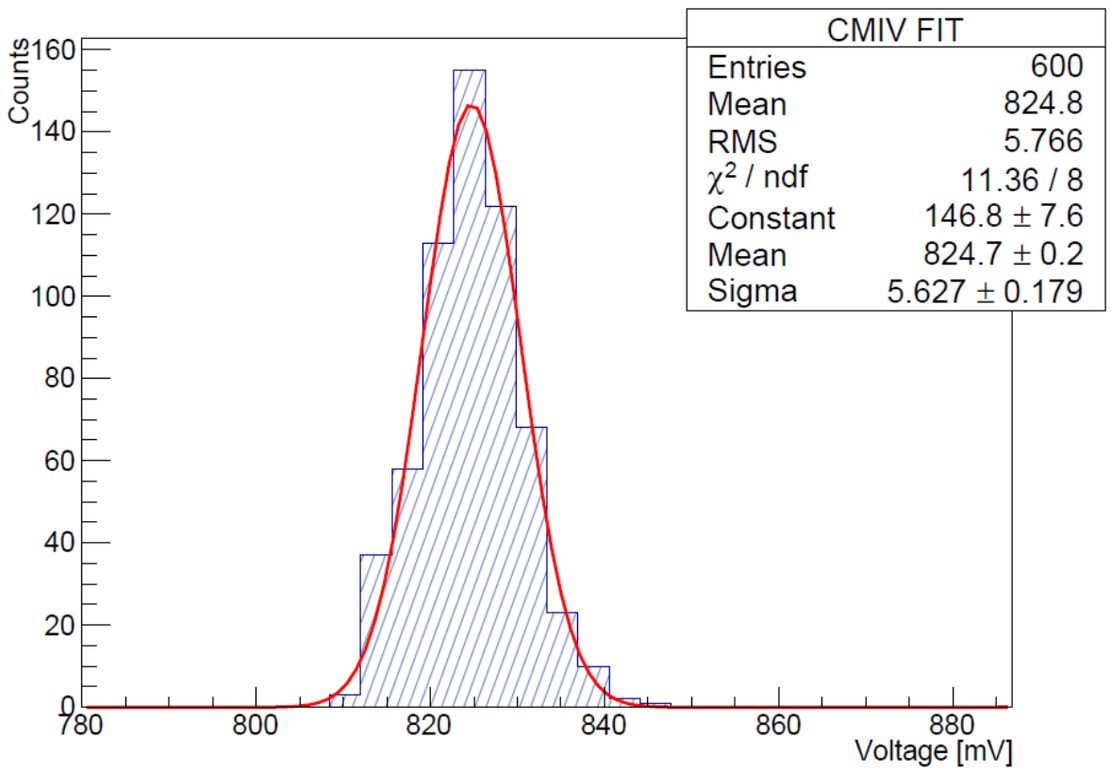
- In full depletion, total matrix capacitance is 2.7 pF
- I-V cure: few nA up to 180 V
- Maximum voltage before breakdown 240 V

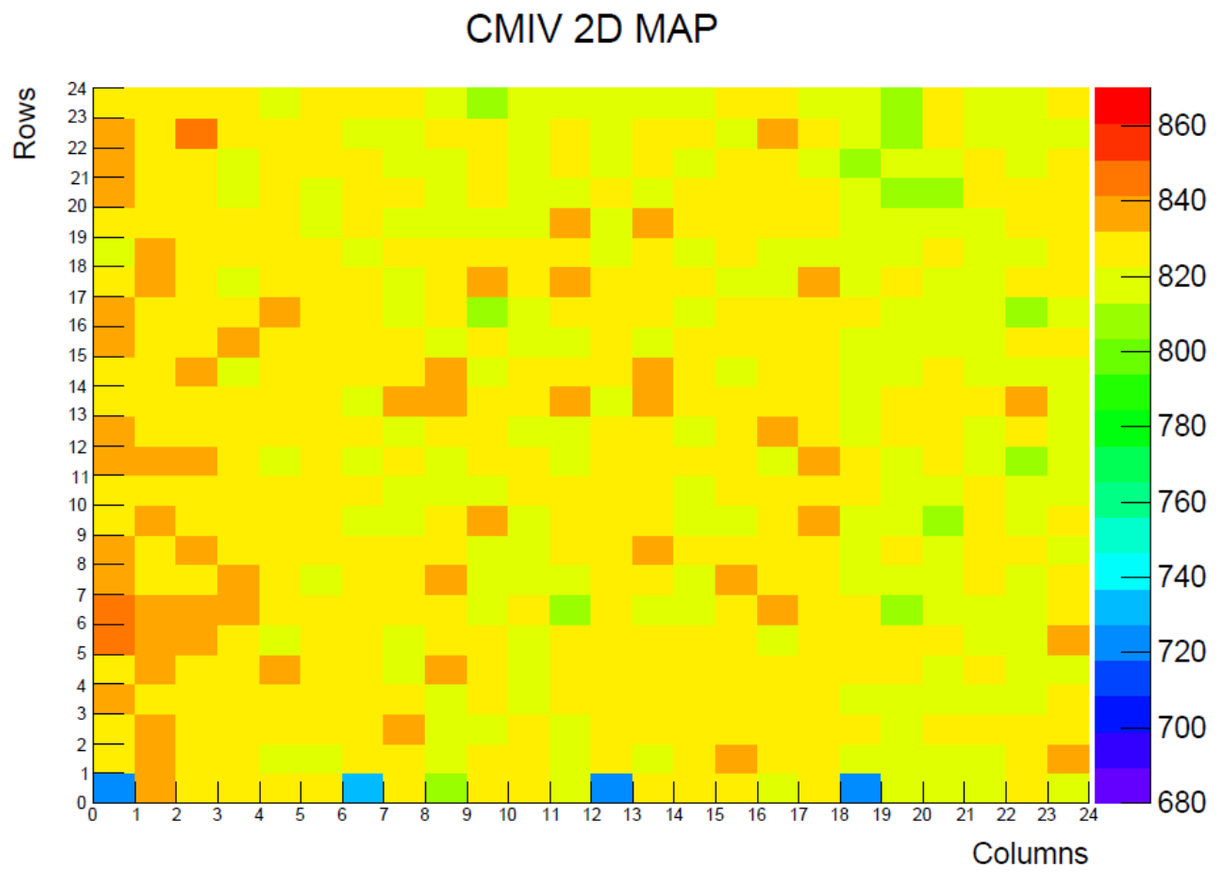




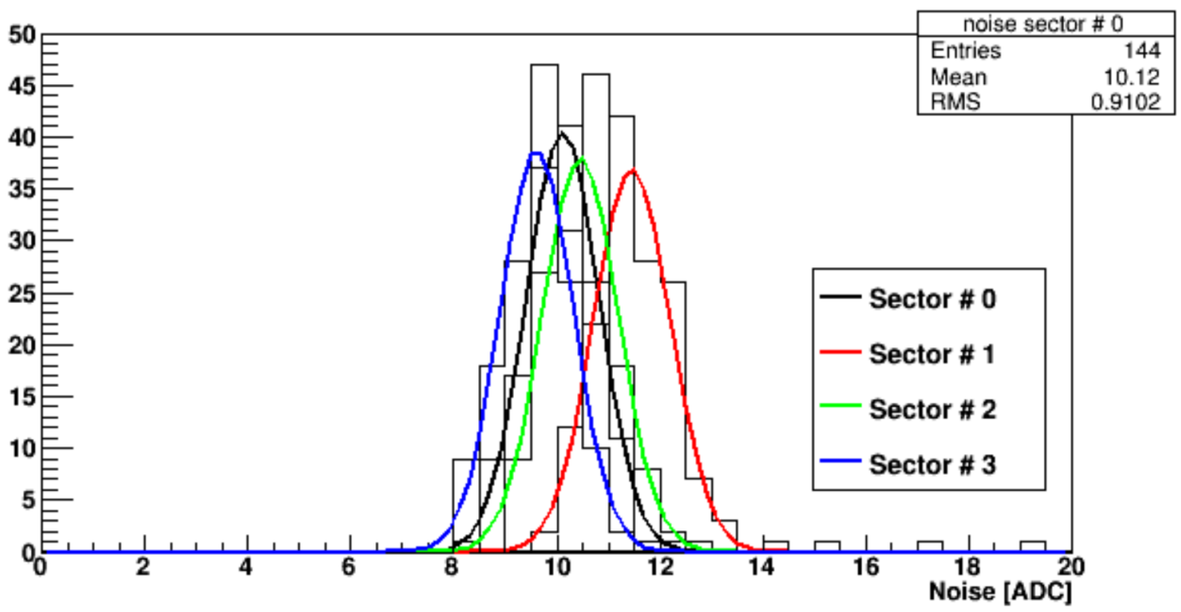


Uniformity and noise

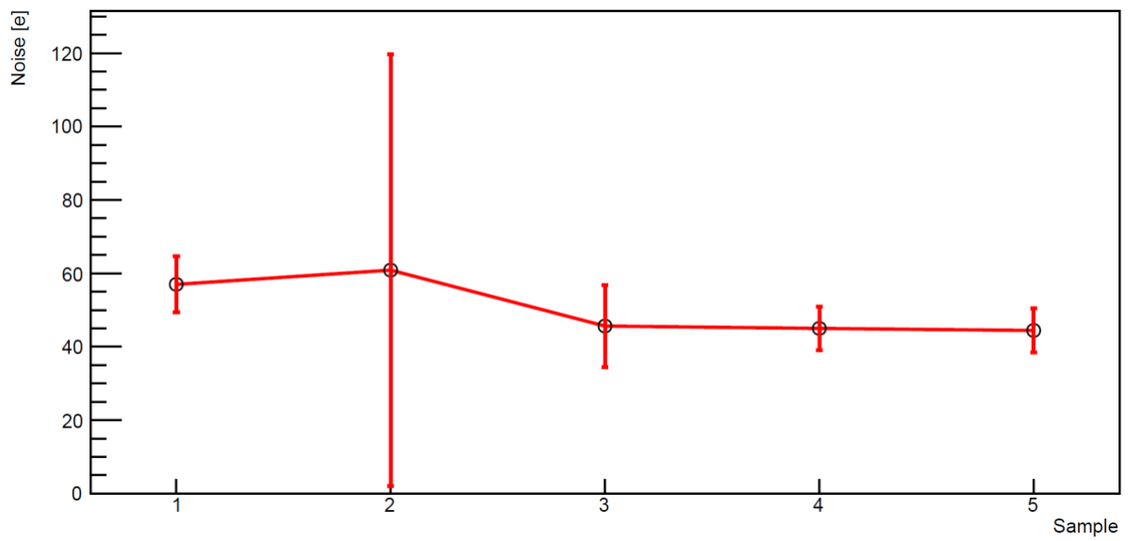




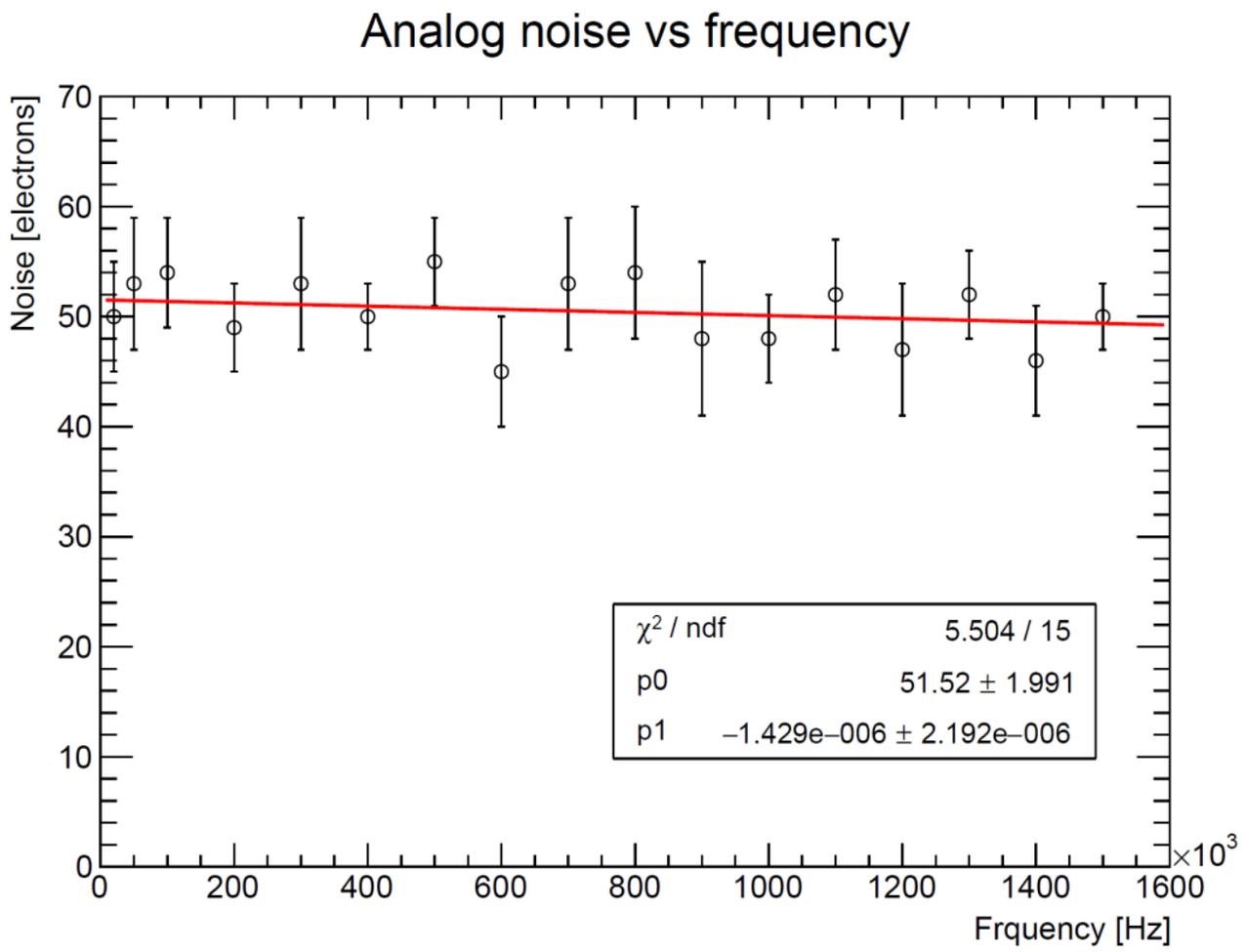
All sectors



More samples



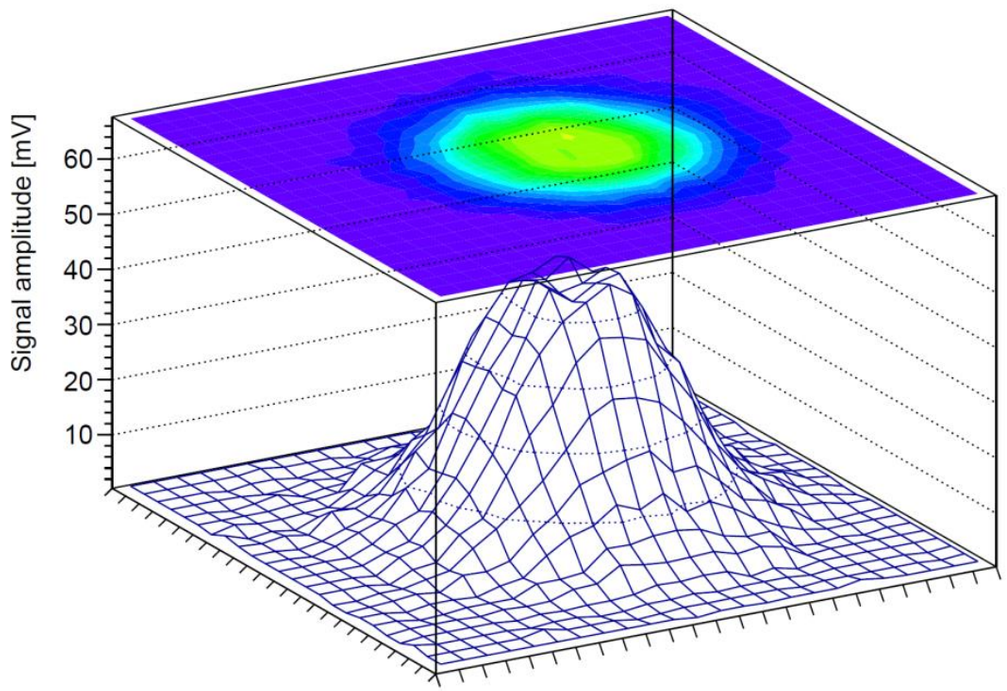
Digitally induced noise

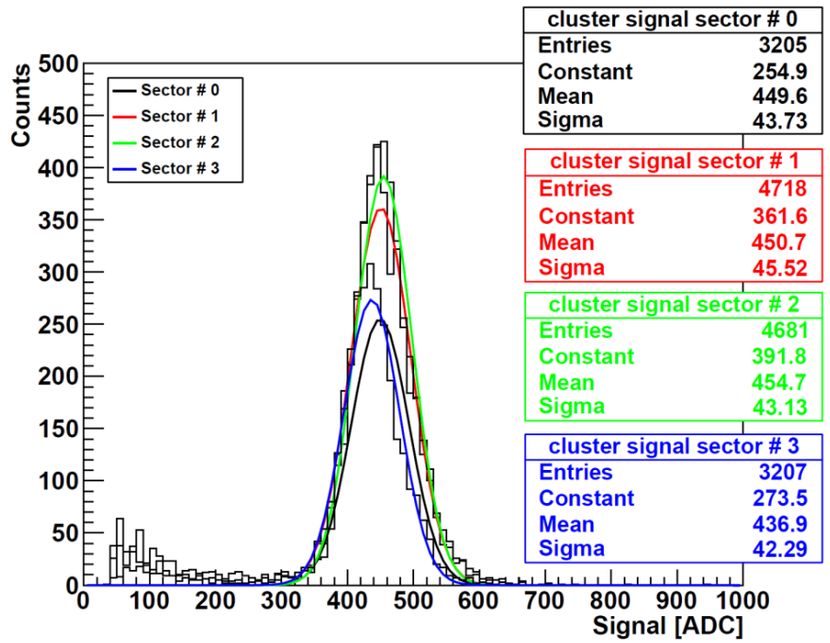


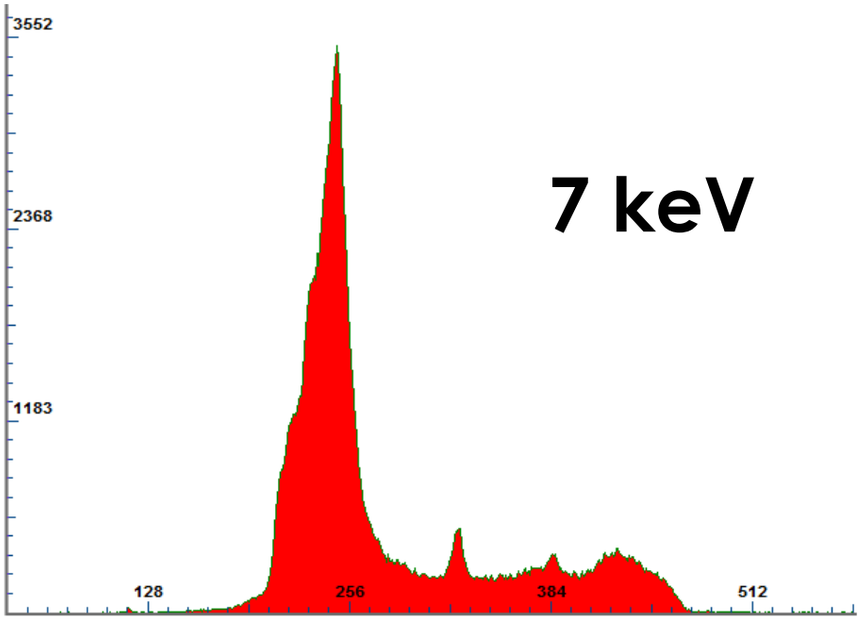
- **Good separation between analog and digital circuits**

With lasers and X-rays

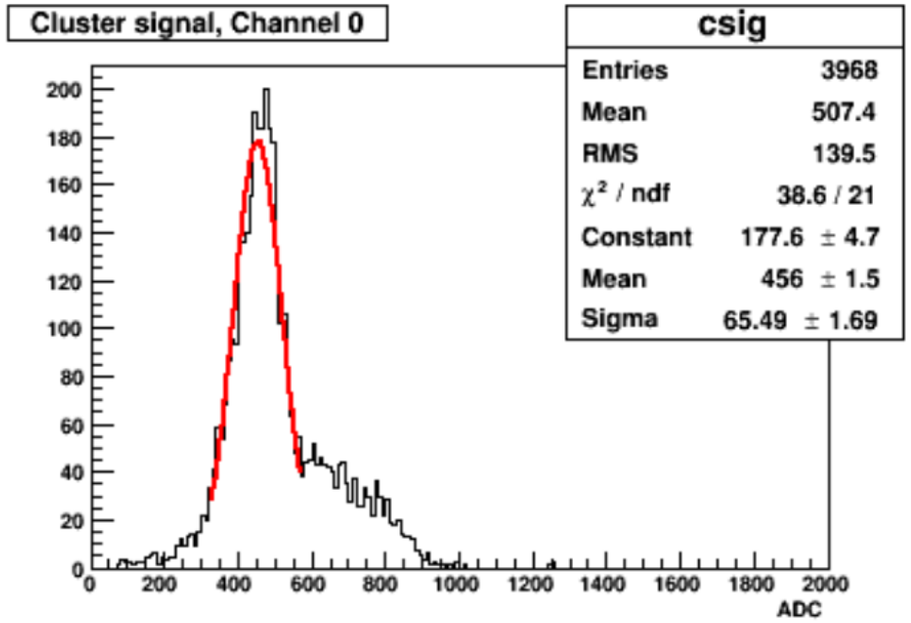
Unfocused pulse







7 keV

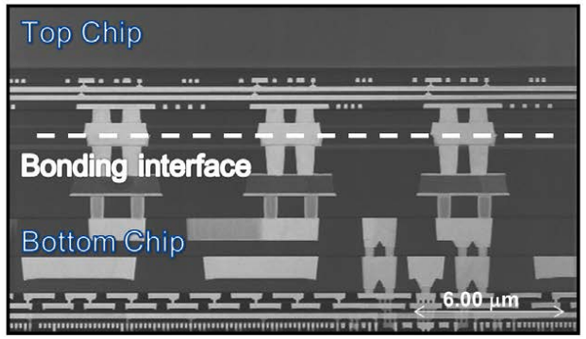


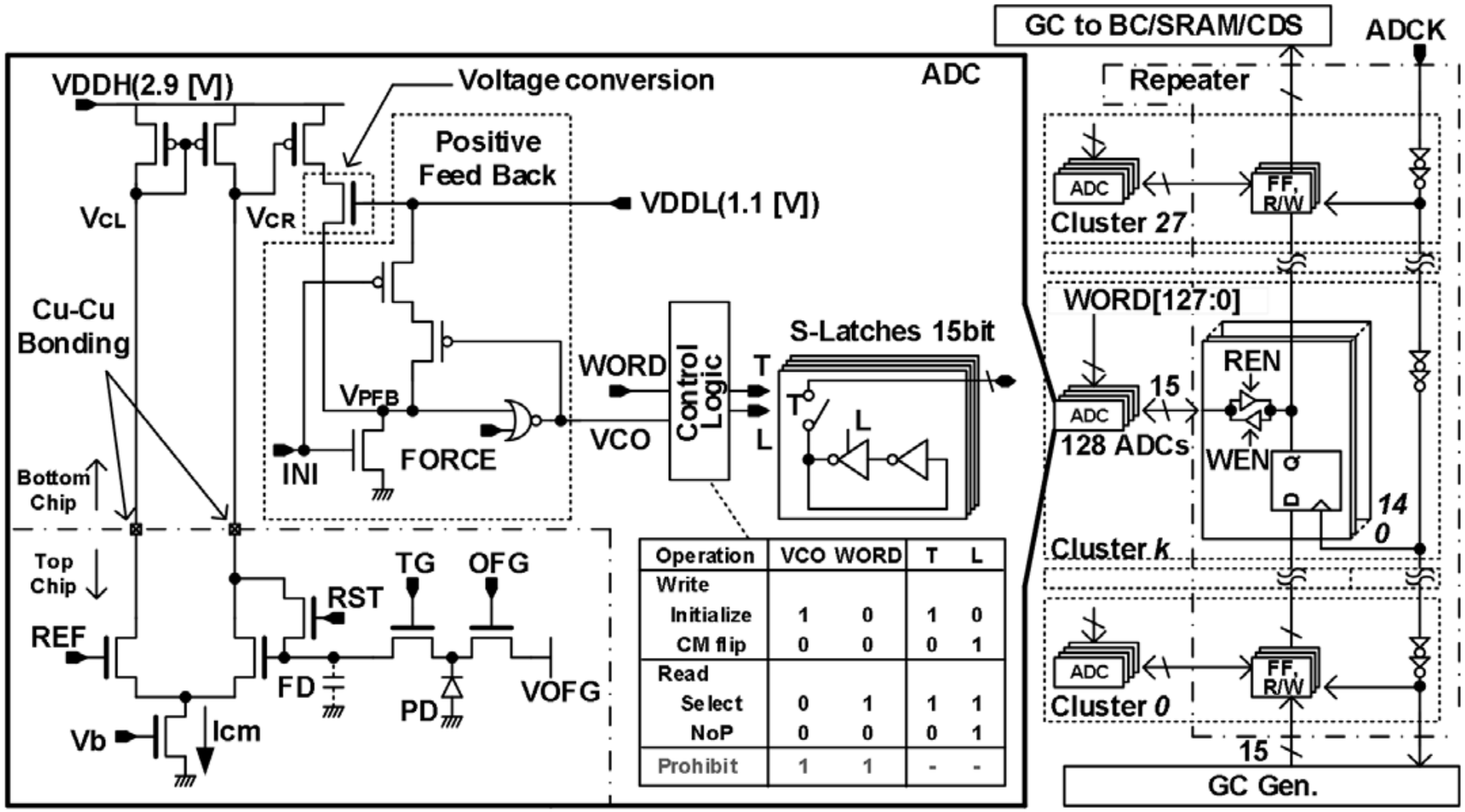
About integration density

5.1 A Back-Illuminated Global-Shutter CMOS Image Sensor with Pixel-Parallel 14b Subthreshold ADC

Masaki Sakakibara[1], Koji Ogawa[1], Shin Sakai[1], Yasuhisa Tochigi[1], Katsumi Honda[1], Hidekazu Kikuchi[1], Takuya Wada[1], Yasunobu Kamikubo[1], Tsukasa Miura[1], Masahiko Nakamizo[1], Naoki Jyo[2], Ryo Hayashibara[2], Yohei Furukawa[3], Shinya Miyata[3], Satoshi Yamamoto[1], Yoshiyuki Ota[1], Hirotsugu Takahashi[1], Tadayuki Taura[1], Yusuke Oike[1], Keiji Tatani[1], Takashi Nagano[1], Takayuki Ezaki[1], Teruo Hirayama[1]

[1]Sony Semiconductor Solutions, Atsugi, Japan
[2]Sony Semiconductor Manufacturing, Kumamoto, Japan
[3]Sony LSI Design, Fukuoka, Japan





Operation	VCO	WORD	T	L
Write				
Initialize	1	0	1	0
CM flip	0	0	0	1
Read				
Select	0	1	1	1
NoP	0	0	0	1
Prohibit	1	1	-	-

Summary

- CMOS sensors for tracking are making very good progress
  - 2-layer devices for high-density, high-speed environments
  - 1-layer sensor for outer layers
- Power likely to be limited by data transfer
- Very good perspective for timing trackers…but devil is the details