

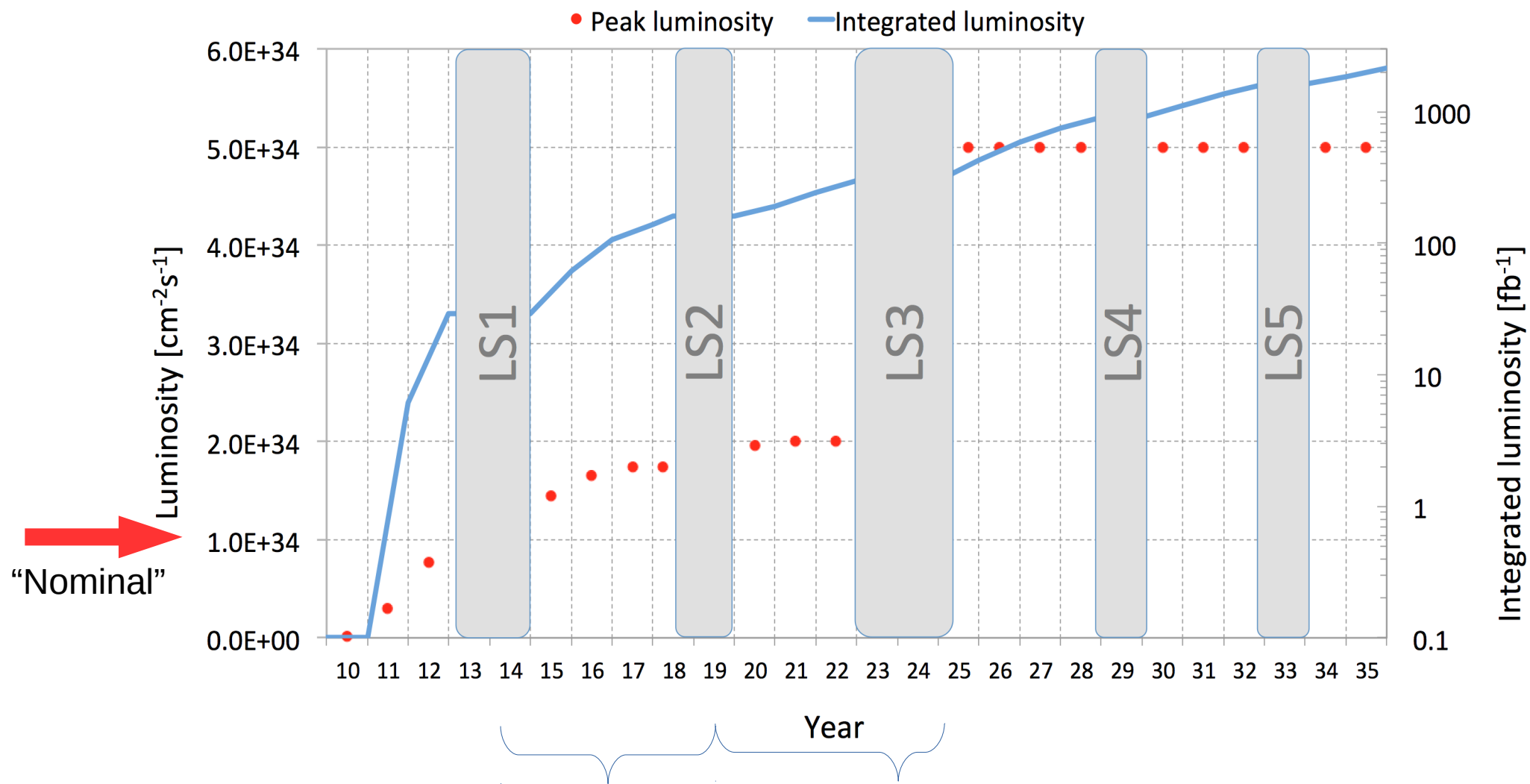


# *The CMS Upgrades*

Jeremiah Mans  
November 13, 2014



# The Coming Challenges



**Phase 1 Upgrades**  
 Targeted at managing 2x nominal pileup  
 and integrated luminosity up to  $\sim 500 \text{ fb}^{-1}$

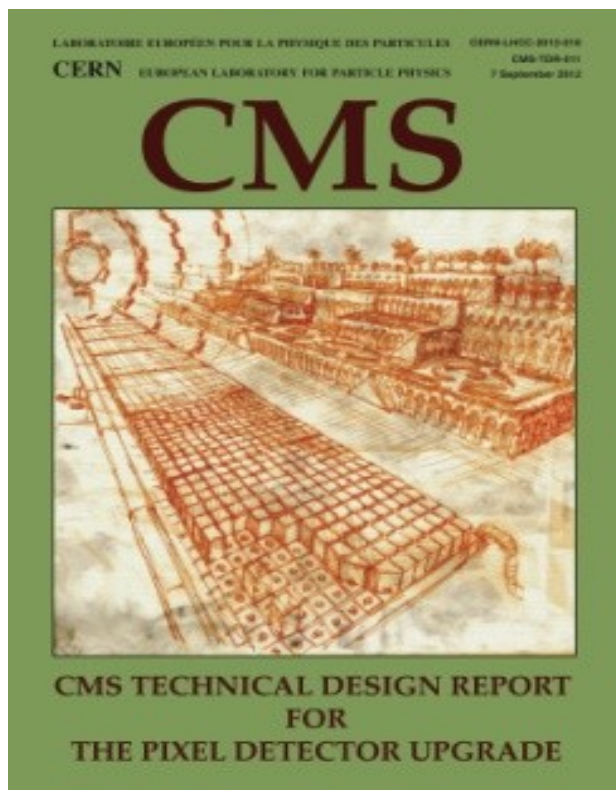
**Phase 2 Upgrades**  
 Targeted at managing 5x-8x nominal pileup  
 and integrated luminosity up to  $\sim 3000 \text{ fb}^{-1}$



# Phase 1: Tuning Up

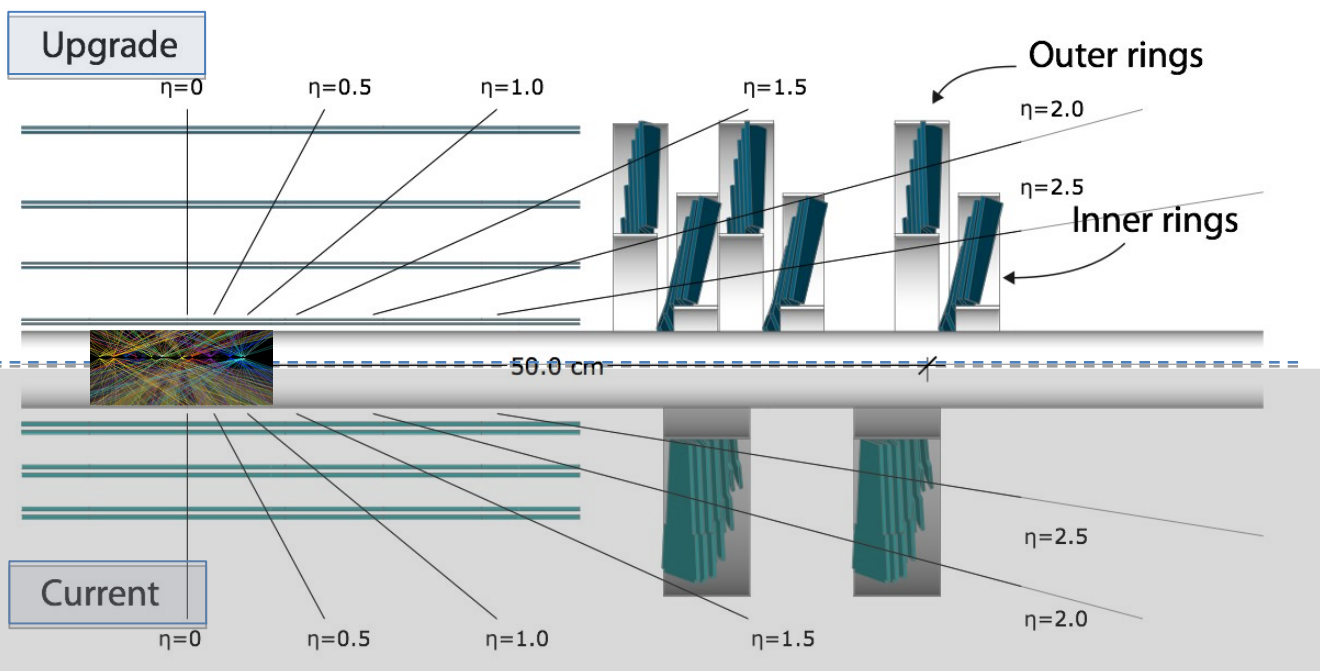


- Incremental changes to manage higher pileup and take advantage of new technologies developed since original construction
- Major US Roles in all these upgrades, successful DOE CD 2/3 review in August

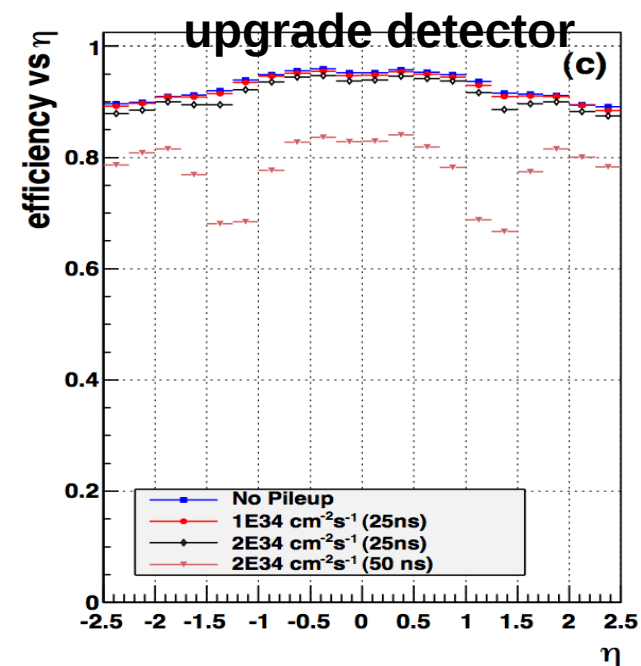
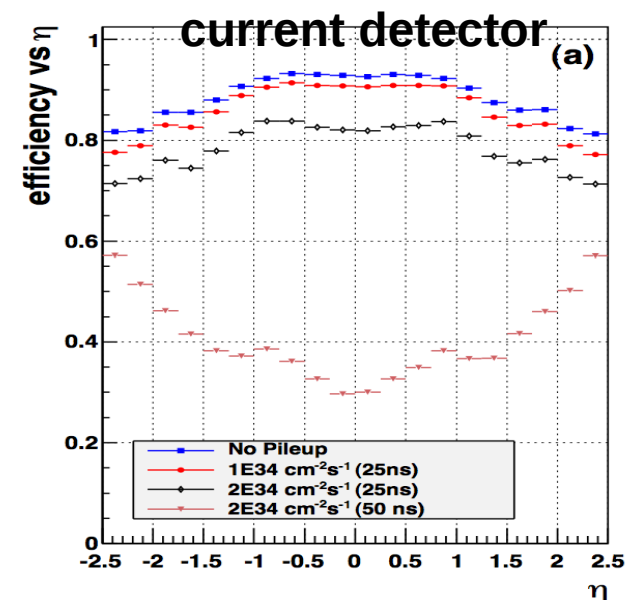




# CMS Pixel Upgrade

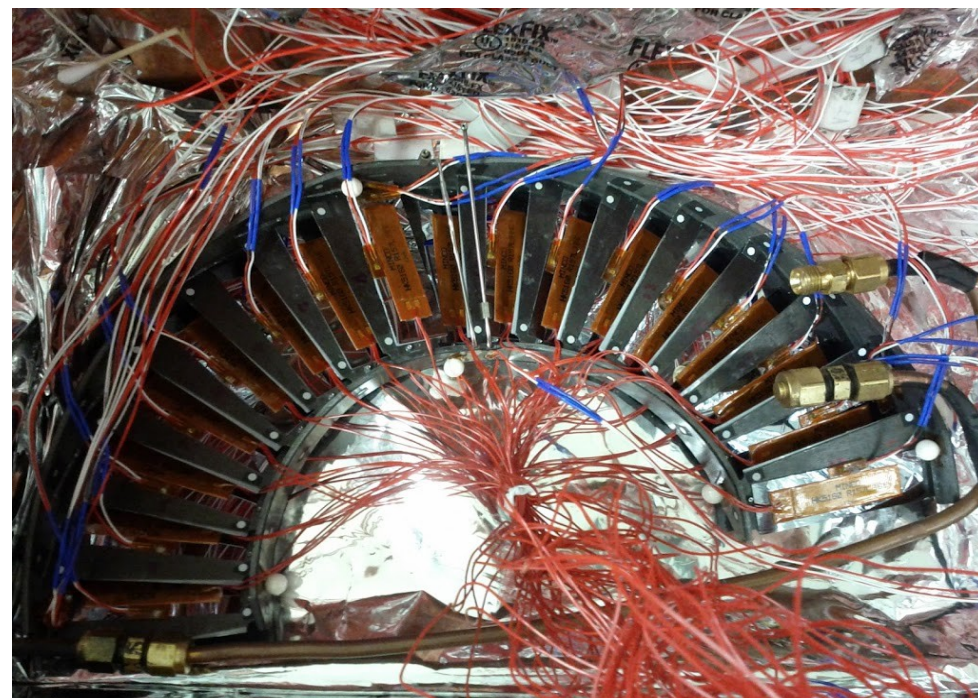
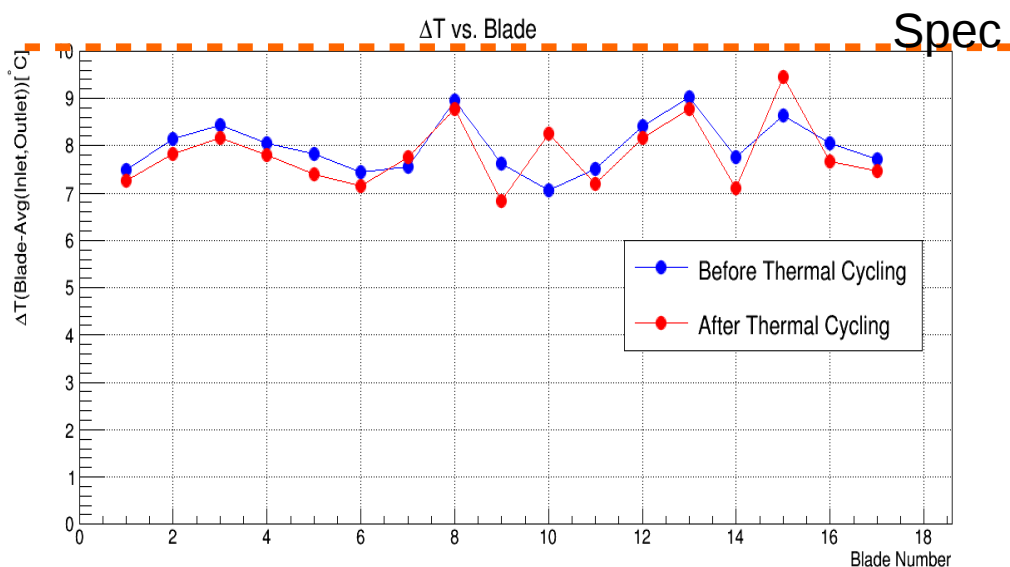


- Increase number of pixel hits from three to four within  $|\eta| < 2.5$
- New ROC allows operation at 50 PU/100kHz without hit loss and acceptable hit loss up to PU~100
- US responsible for construction of the forward pixel system (three stations at each end)



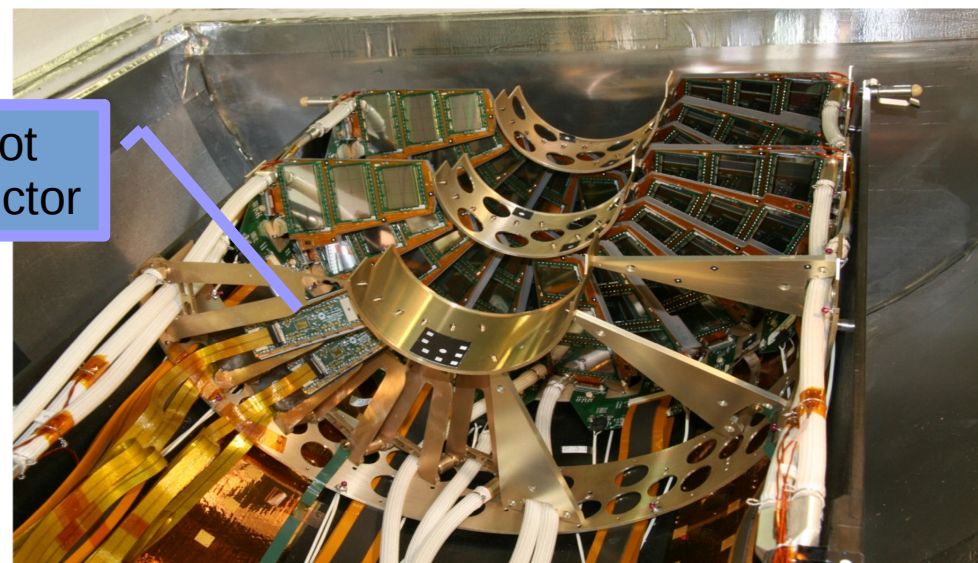


# Progress on the Forward Pixels



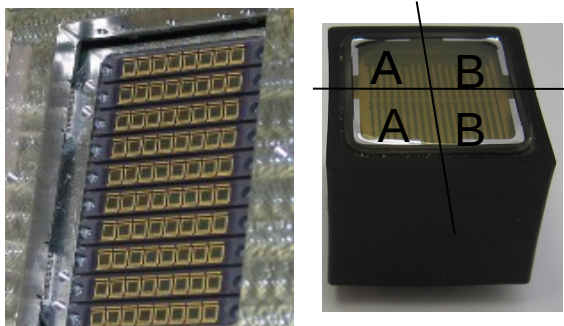
- Thermal test of cooling setup for half-disk successful
- Pilot detector (sensors, chips, powering, cables) mounted on CMS pixel assembly for Run 2

Pilot Detector

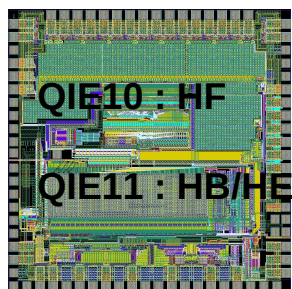
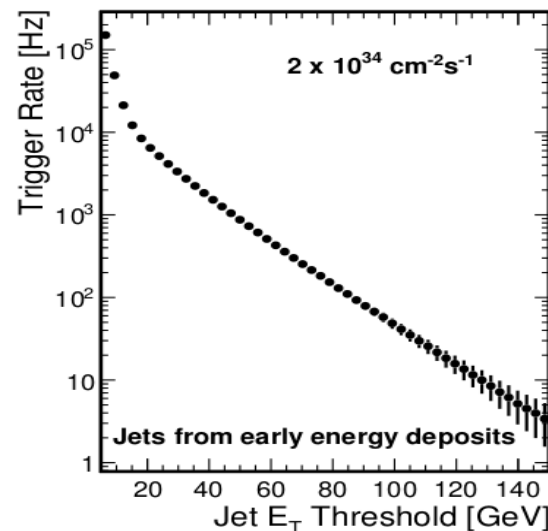




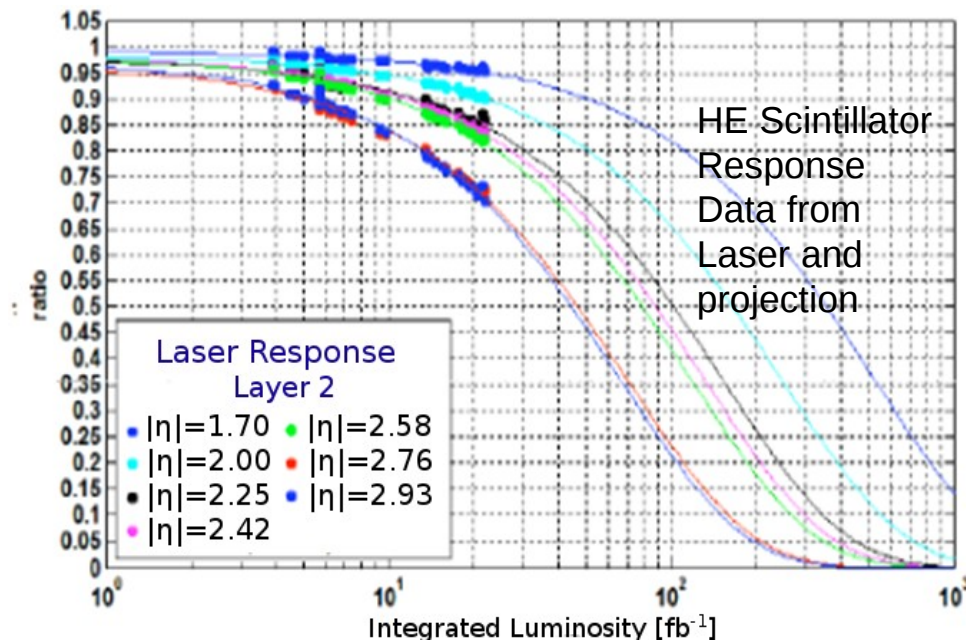
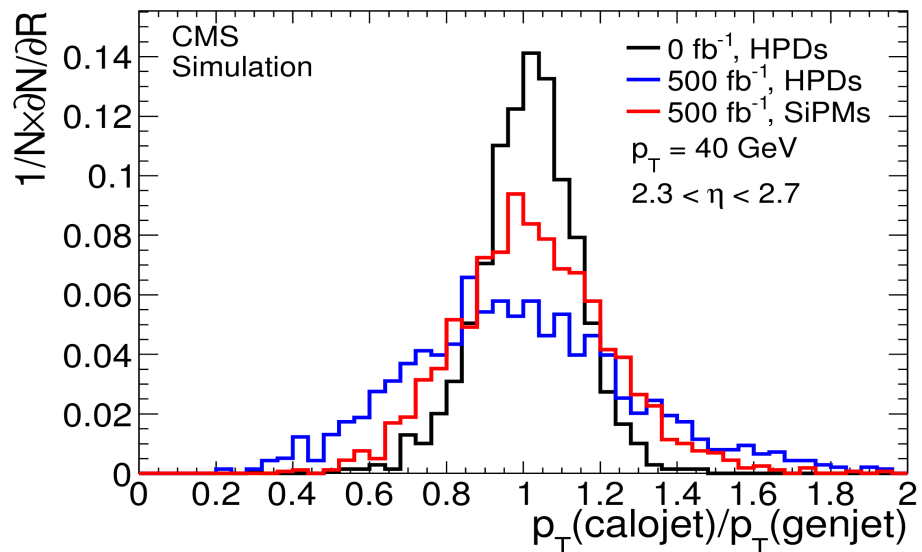
# HCAL Upgrade



- New photodetectors (SiPMs) and capabilities (TDC) to manage radiation damage and anomalous signals
- US responsible for design, much of construction



Igloo2  
FPGA

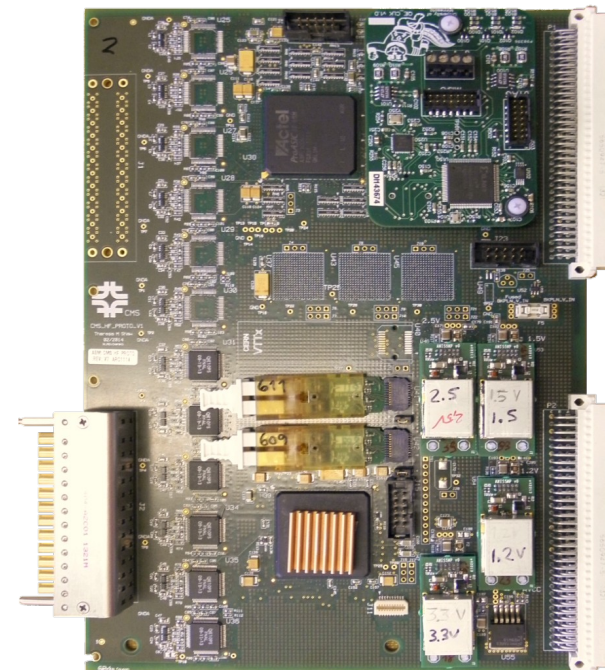




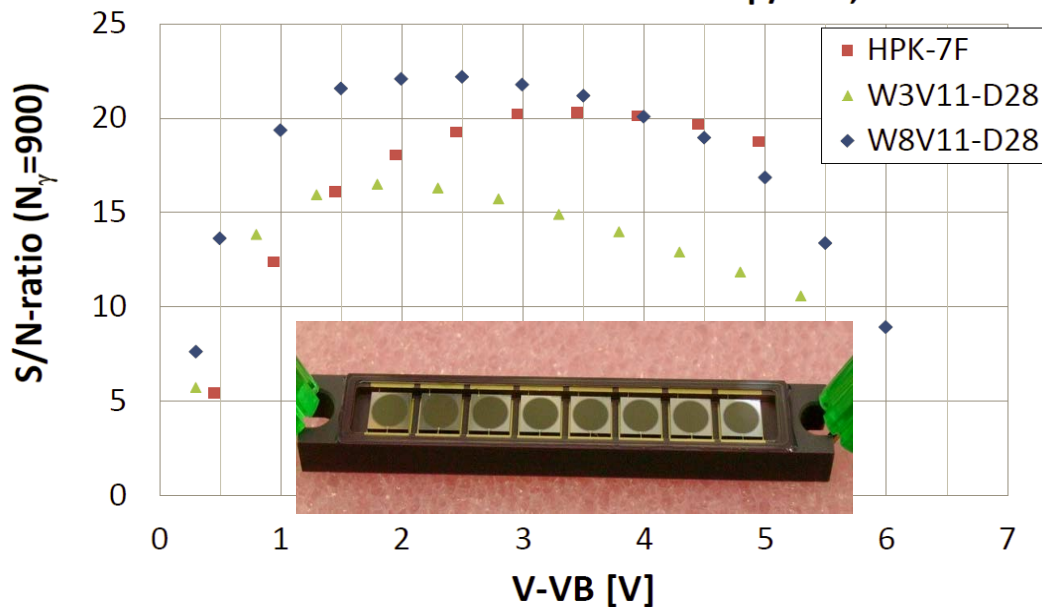
# Progress on the HCAL Phase 1



- Successful QIE10/11 engineering run
- Pre-production cycles underway
  - HF front-end card
  - SiPM and SiPM packages



2.8 mm dia. SiPMs after  $1E11$  p/cm<sup>2</sup>, T=24 C

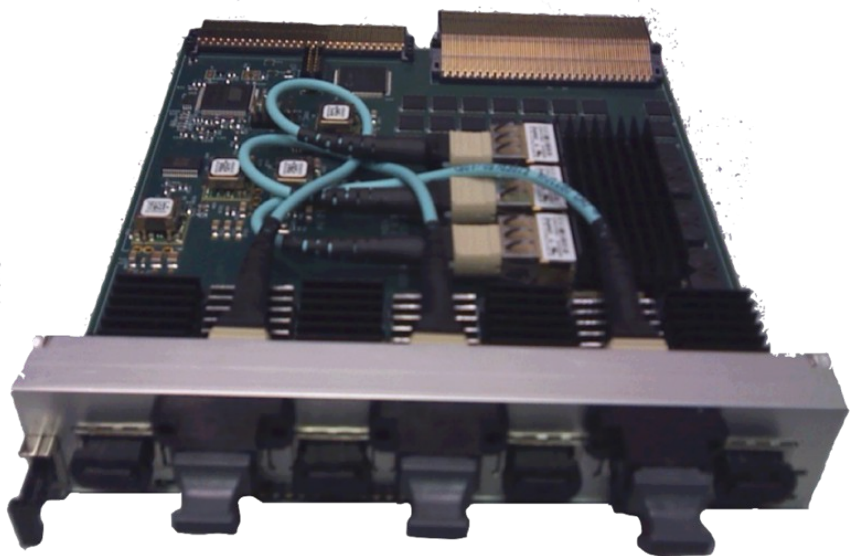




# L1 Trigger Upgrade



- Move to new, high-performance FPGAs to enhance both calorimeter and muon triggering with higher-granularity processing
  - Common use of uTCA architecture
- Strong US leadership in both muon and calo triggers



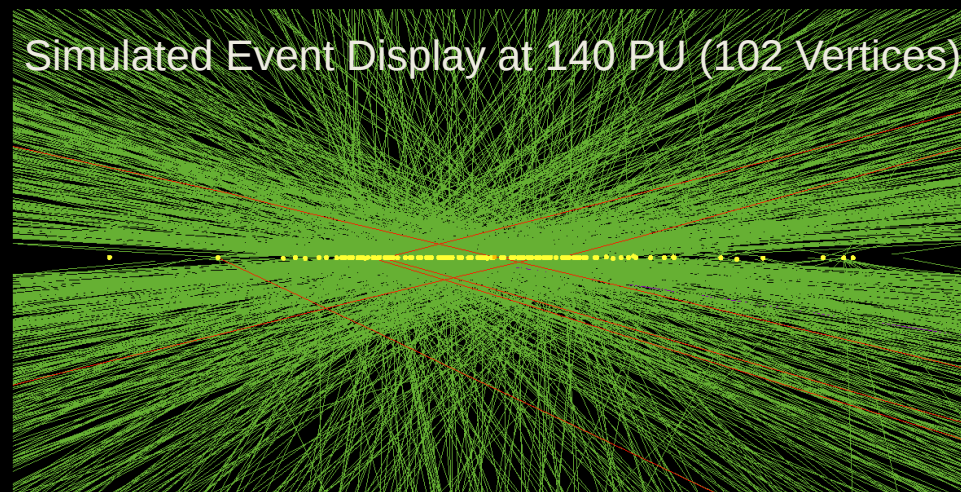
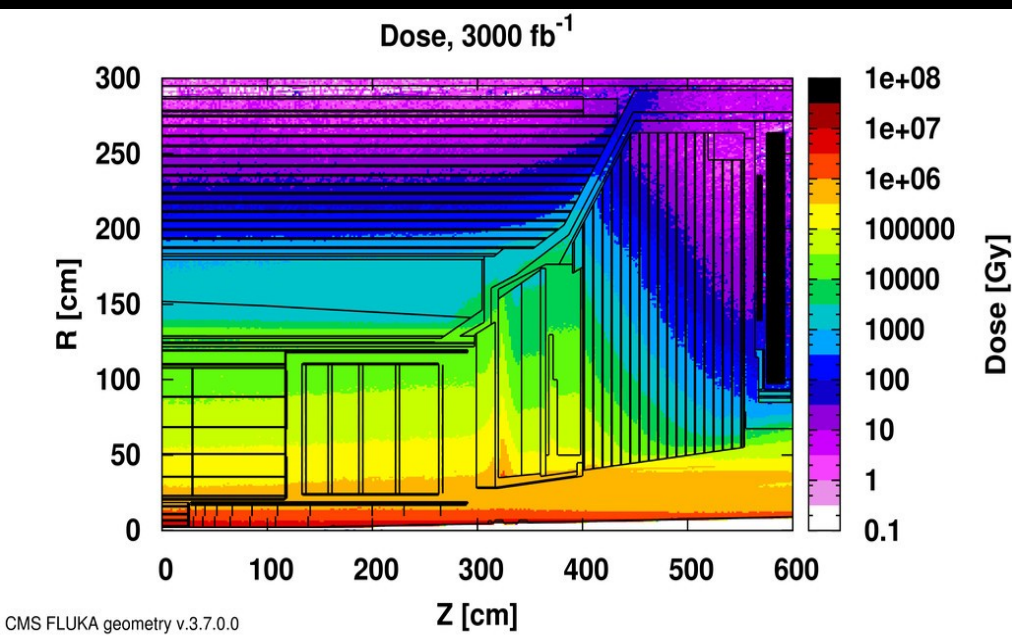




# HL-LHC: Phase 2

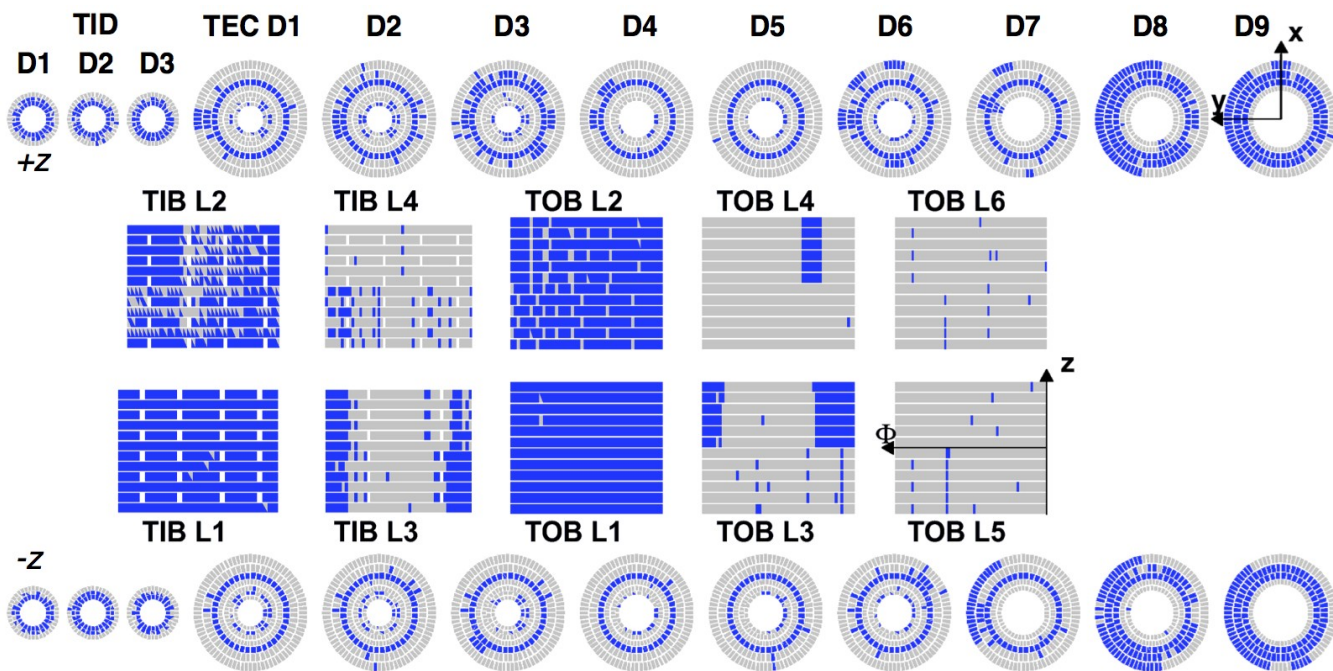


# Bright Light, Big Challenges

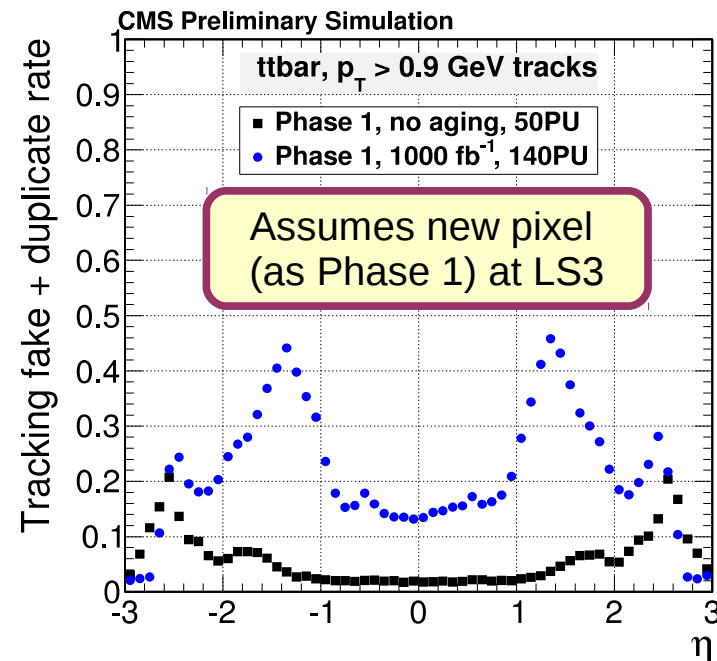
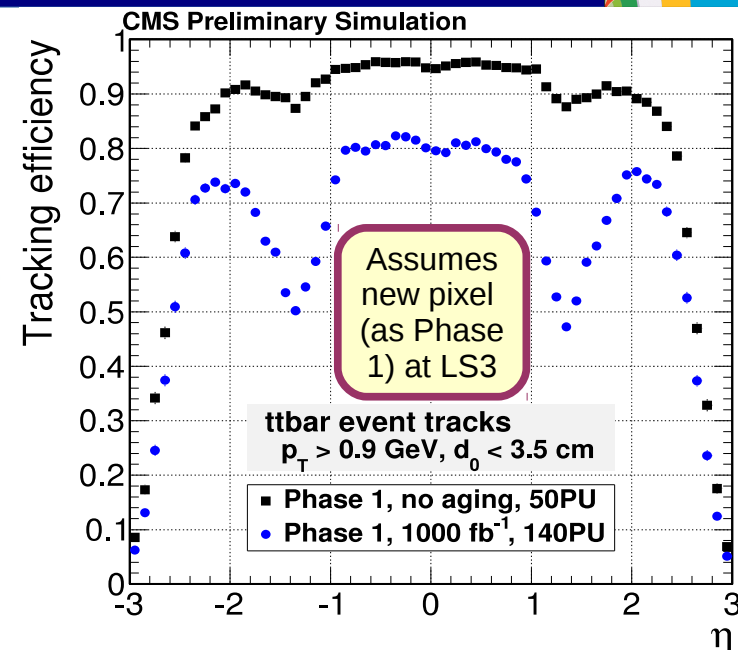




# “Bleaching” of the Tracker

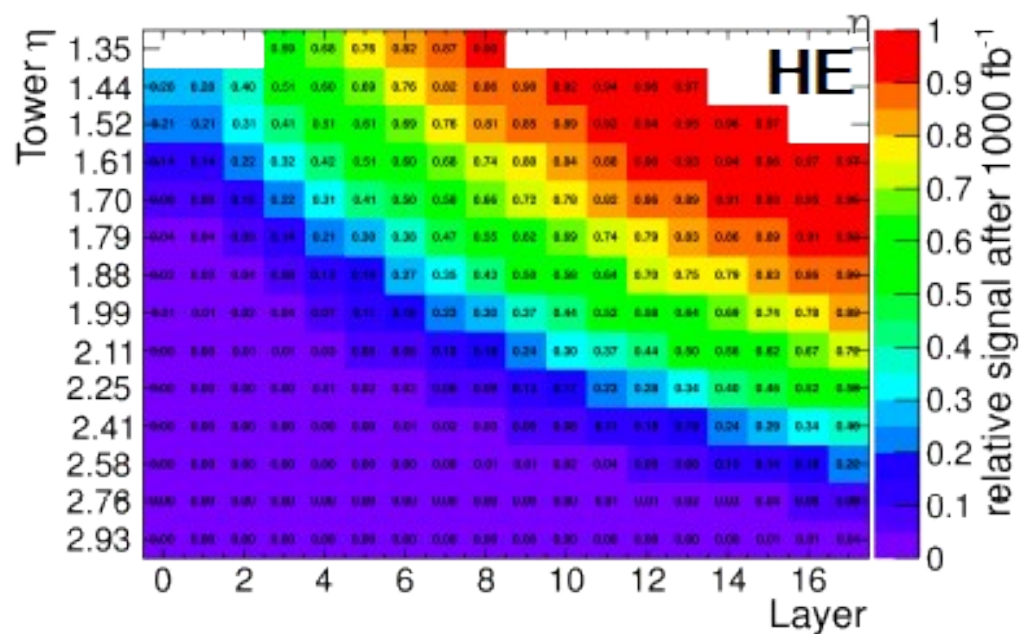
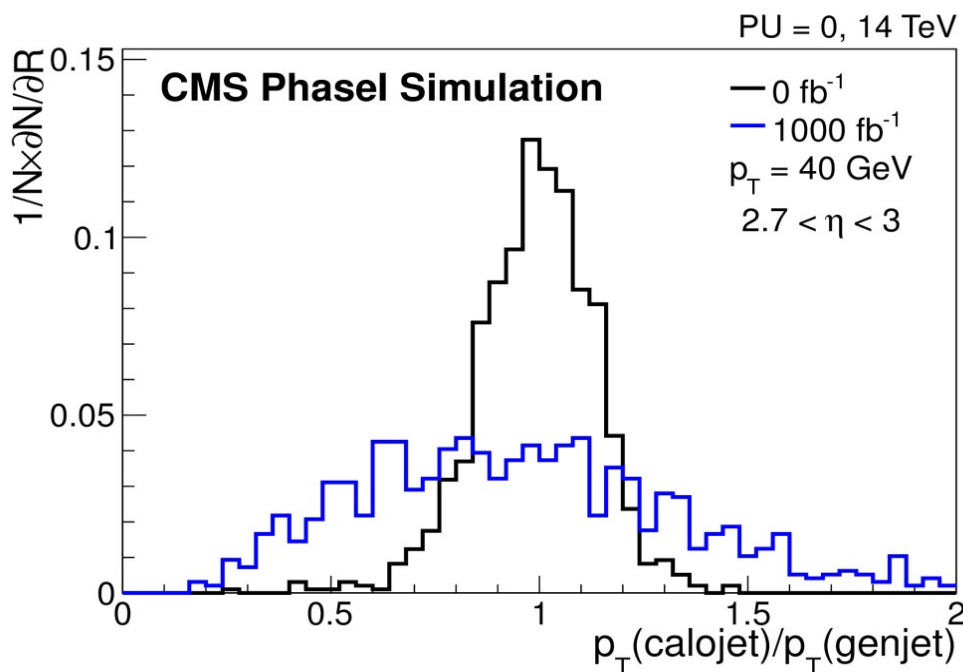
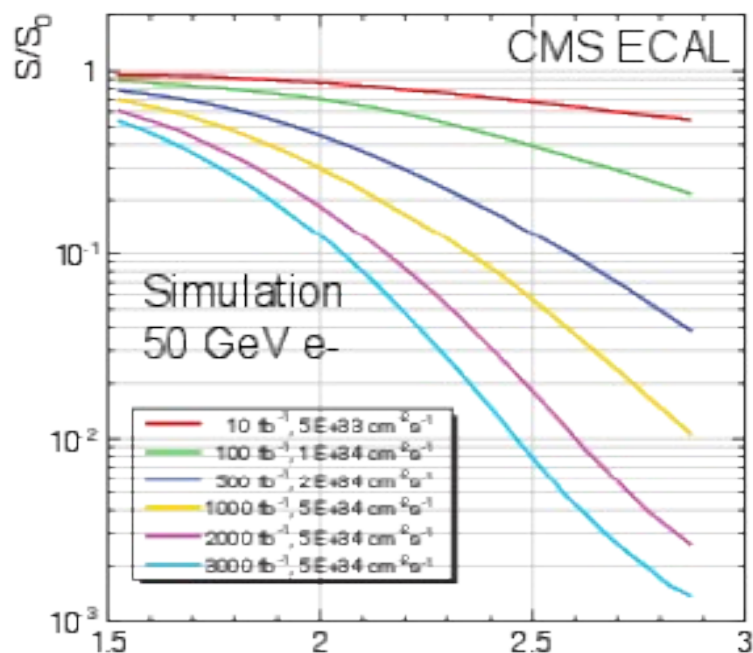
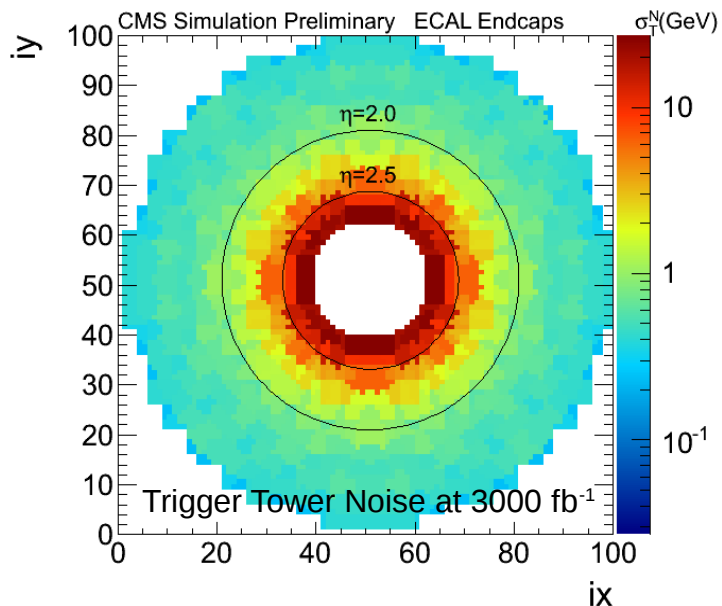


Blue tracker modules are inactive after 1000 fb<sup>-1</sup> due to very high leakage currents induced by hadron fluence.





# “Blackening” of Calorimeters





### New Tracker

- Radiation tolerant - high granularity - less material
- Tracks in hardware trigger (L1)
- Coverage up to  $\eta \sim 4$

### Muons

- Replace DT FE electronics
- Complete RPC coverage in forward region (new GEM/RPC technology)
- Investigate Muon-tagging up to  $\eta \sim 3$

### Barrel ECAL

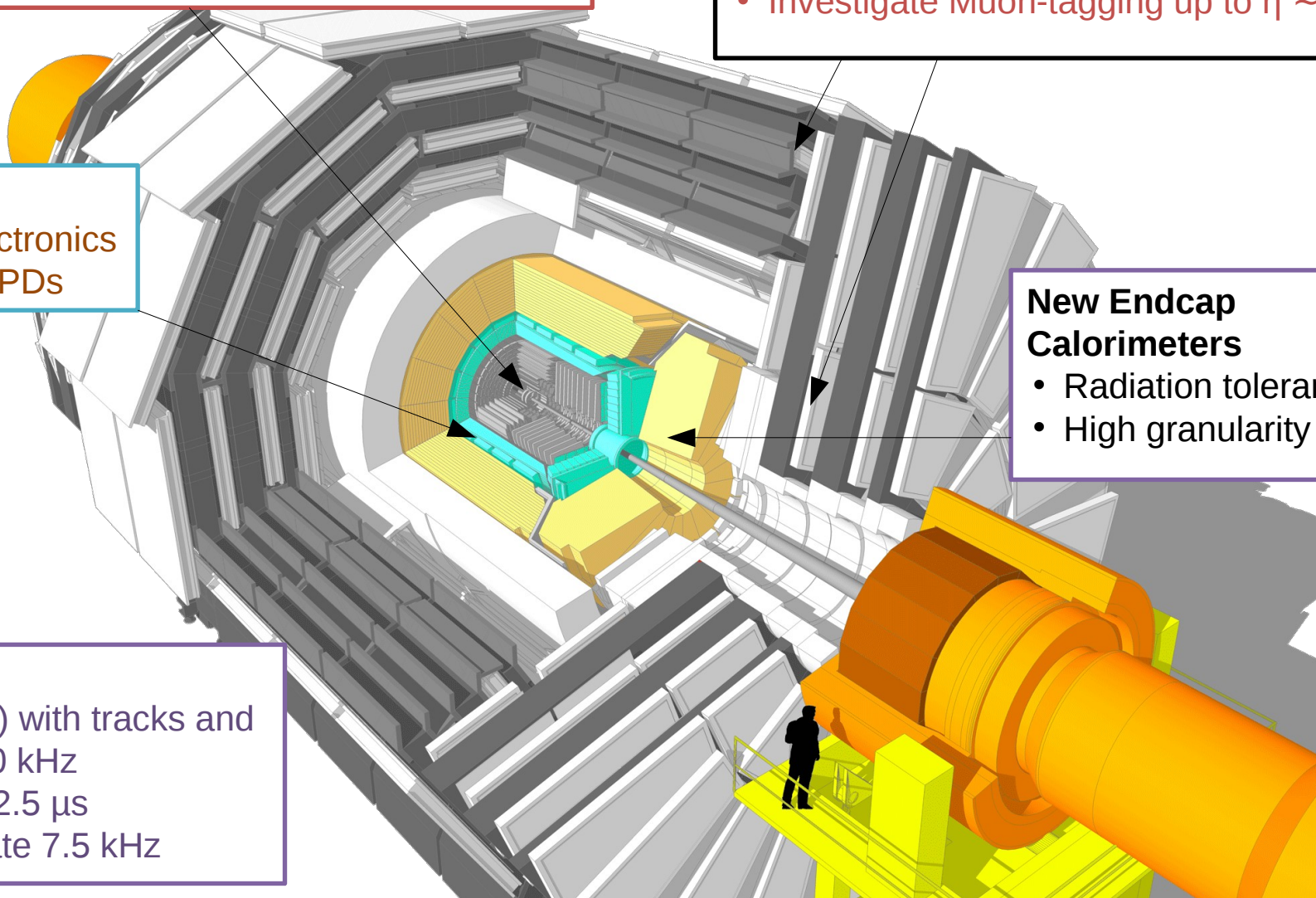
- Replace FE electronics
- Cool detector/APDs

### New Endcap Calorimeters

- Radiation tolerant
- High granularity

### Trigger/DAQ

- L1 (hardware) with tracks and rate up  $\sim 750$  kHz
- L1 Latency  $12.5 \mu\text{s}$
- HLT output rate  $7.5$  kHz

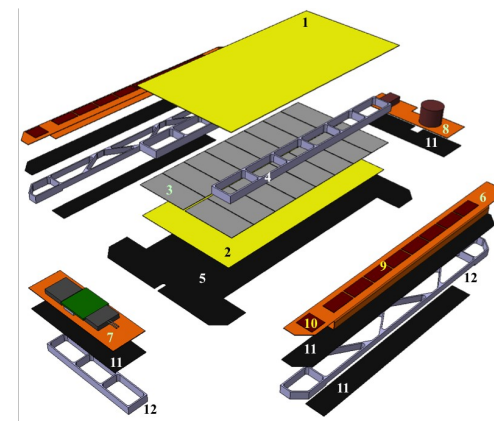
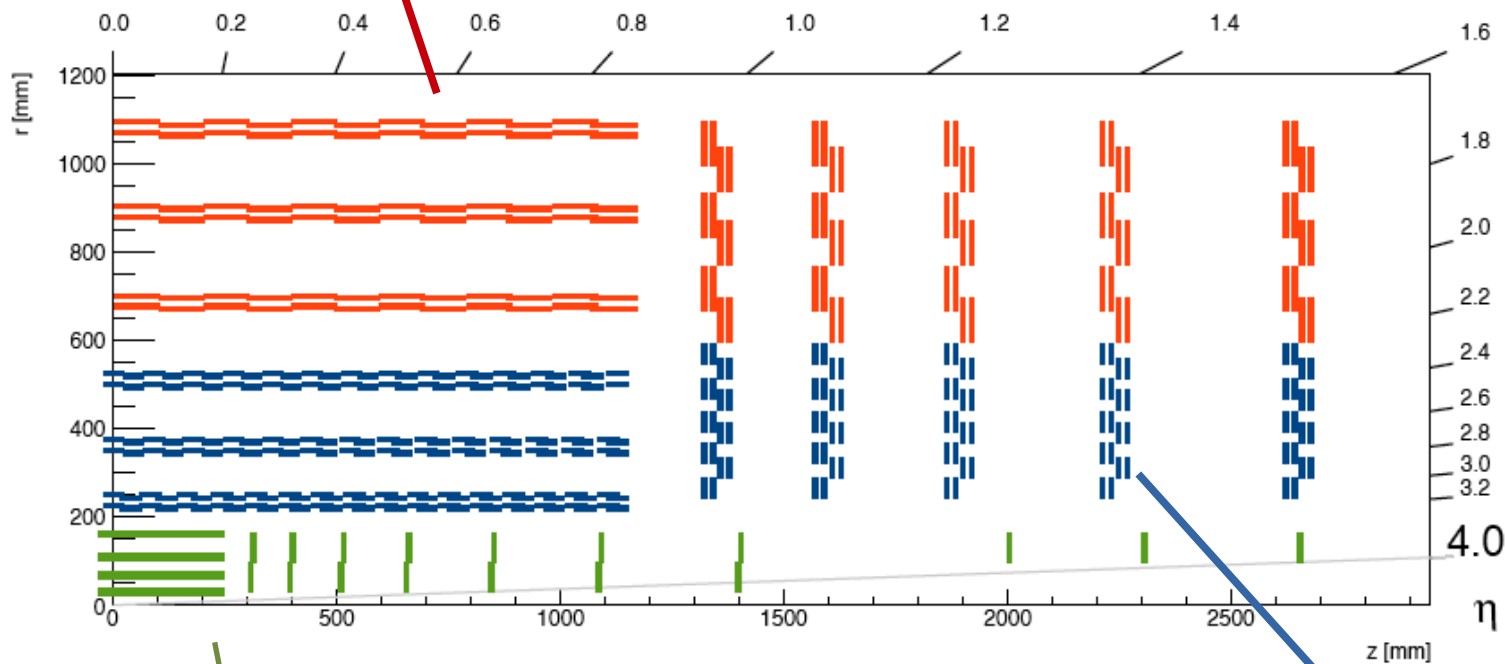
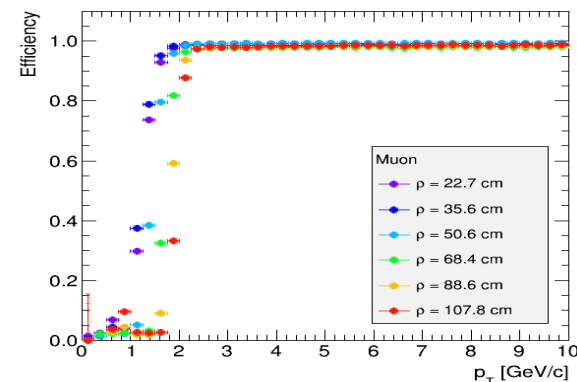
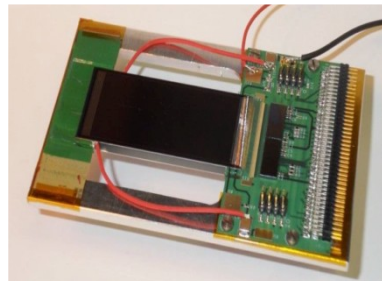
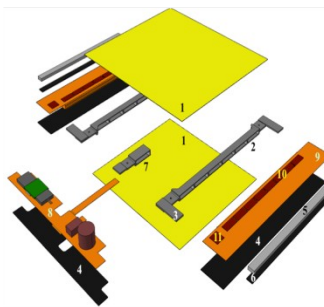




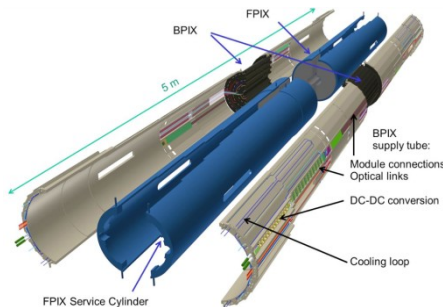
# Tracker Design with Stub Capability



Strip/Strip Modules  
90  $\mu\text{m}$  pitch/5 cm length



Inner Pixel  
Covers up to  $\eta=4.0$



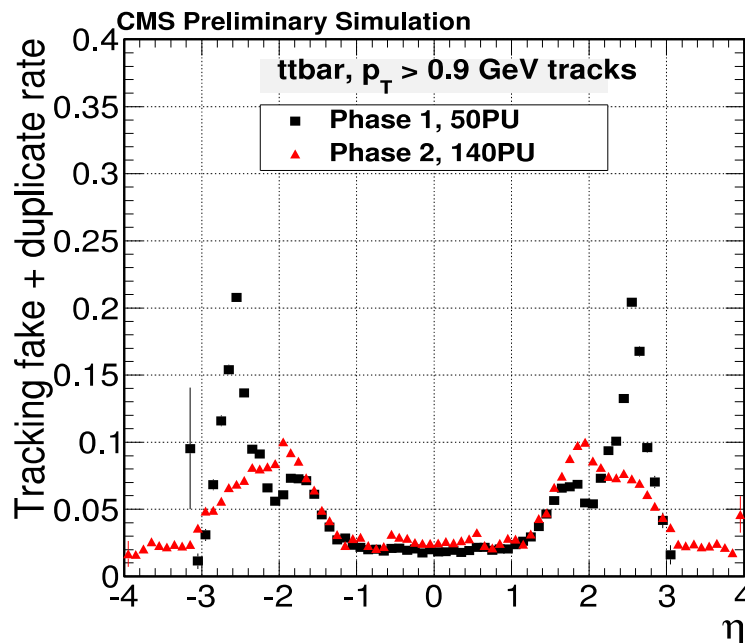
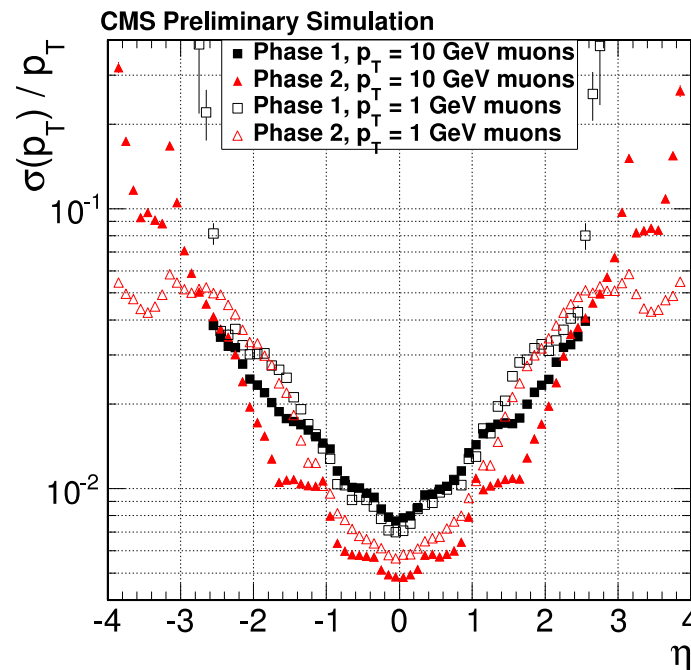
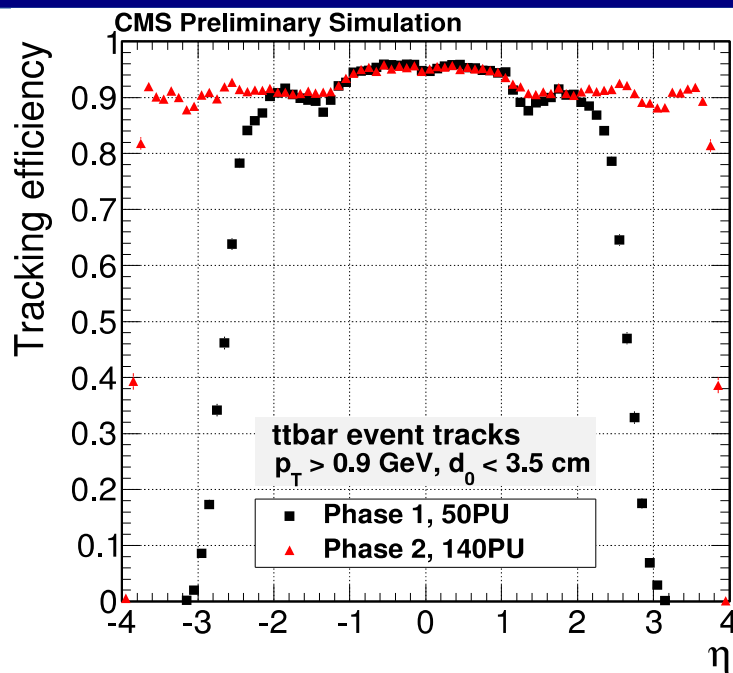
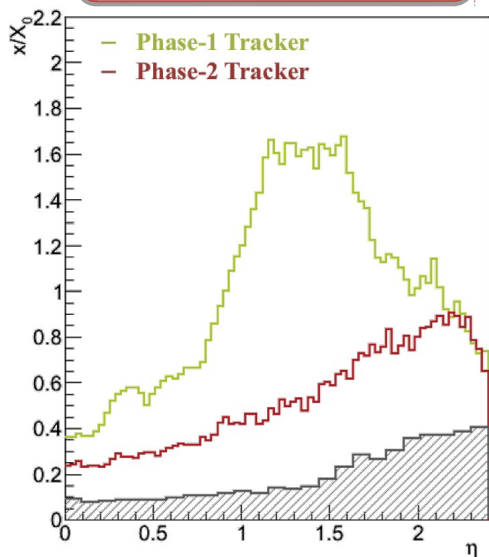
Strip/Pixel Modules  
100  $\mu\text{m}$  pitch/2.5 cm length  
100  $\mu\text{m}$  x 1.5 mm "macropixels"



# Tracker Full Simulation Results



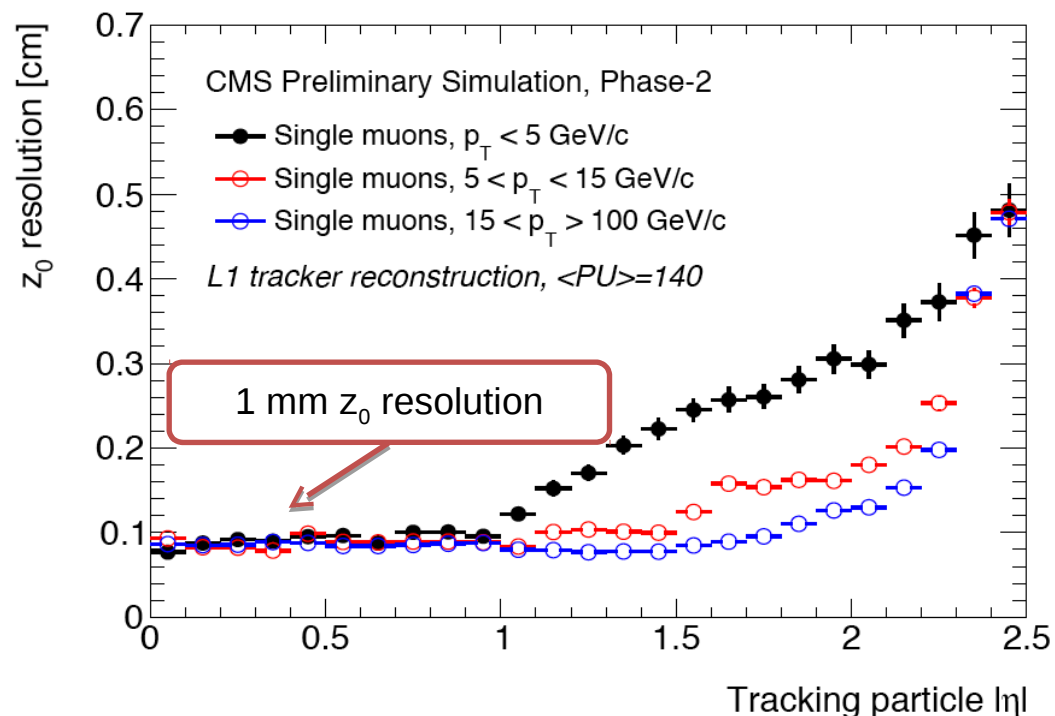
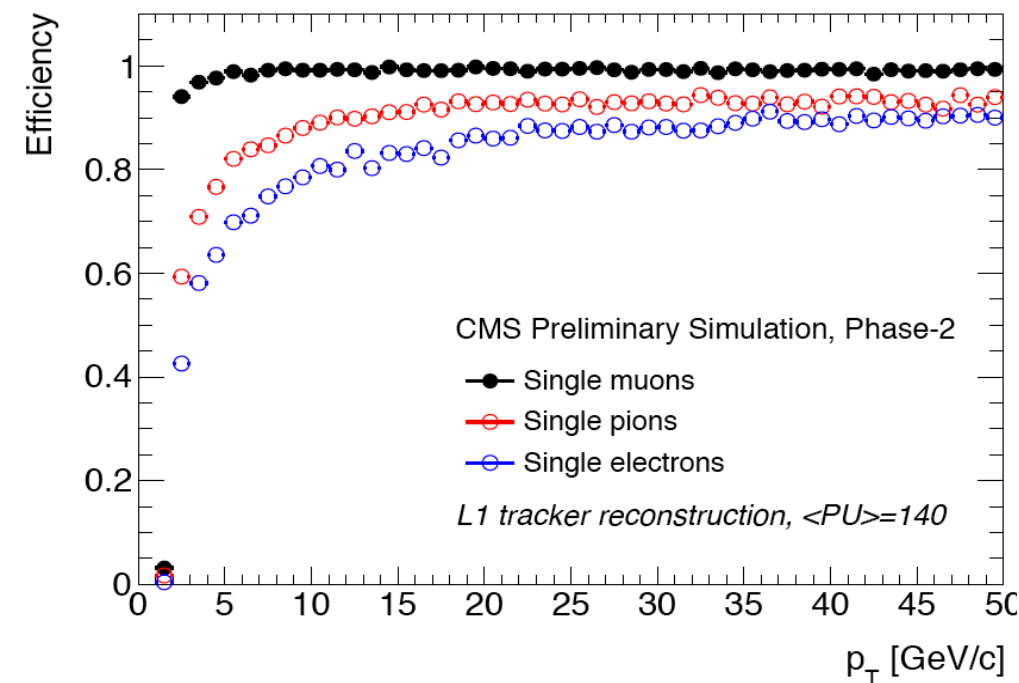
Outer Tracker substantially lighter!



Pixel used in simulation results to date is identical to the Phase 1 Pixel detector with additional forward disks. Further optimization of pixel parameters for b-tagging and forward track parameter resolution is planned



# Tracking Performance at Level 1



- Algorithms validated in digitized simulation
- Two hardware implementations under study
  - Associative memory (use case for 3d IC technology)
  - Tracklets in commercial FPGAs
- Requires a trigger latency of  $\approx 10 \mu\text{s}$  compared with current limit of  $3/6 \mu\text{s}$  in tracker/ECAL electronics

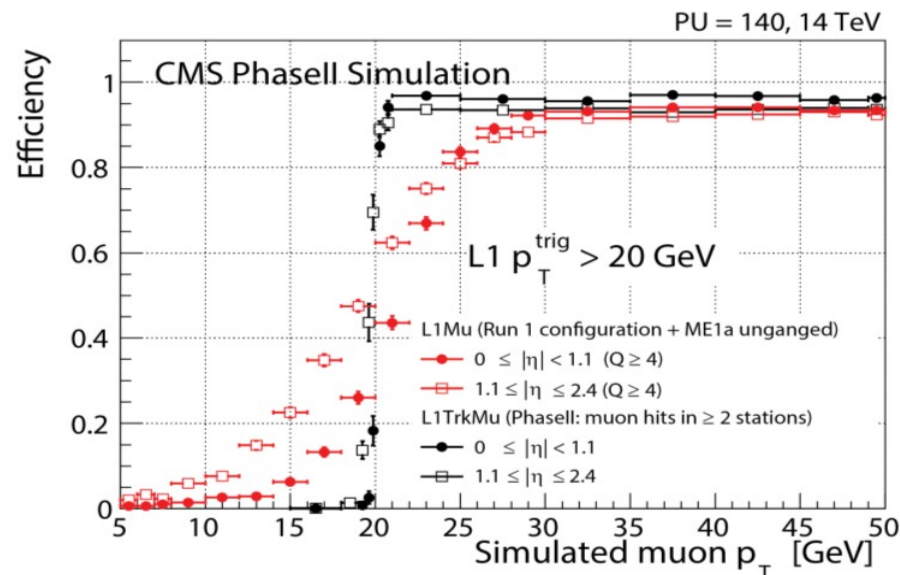
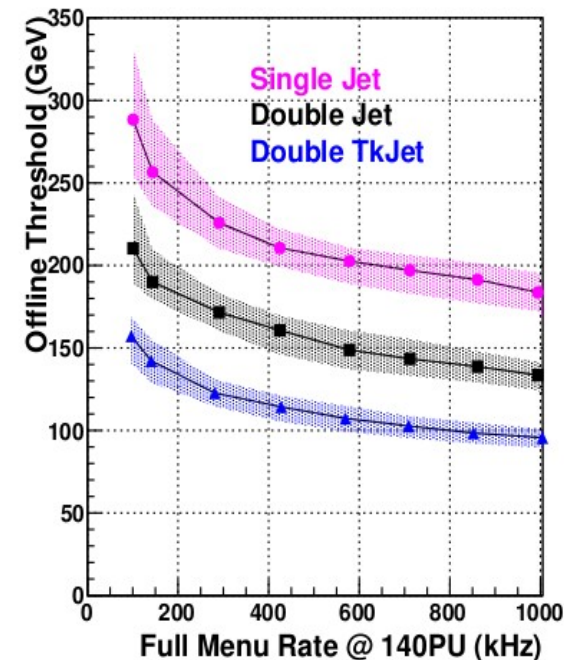
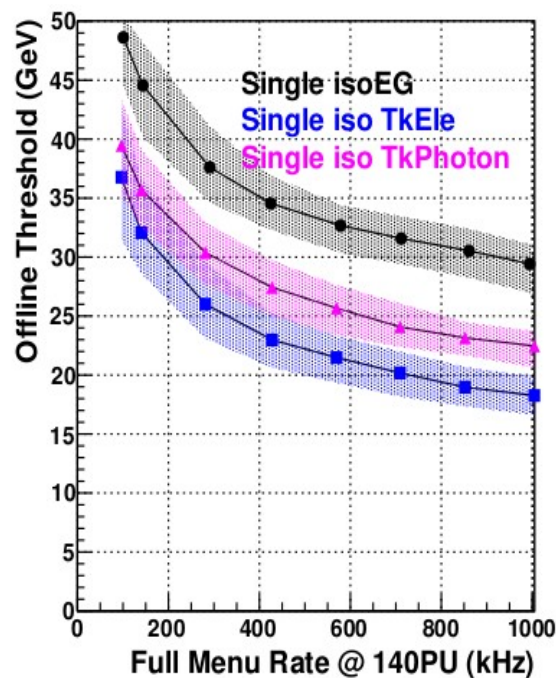




# Trigger Capabilities with Tracking

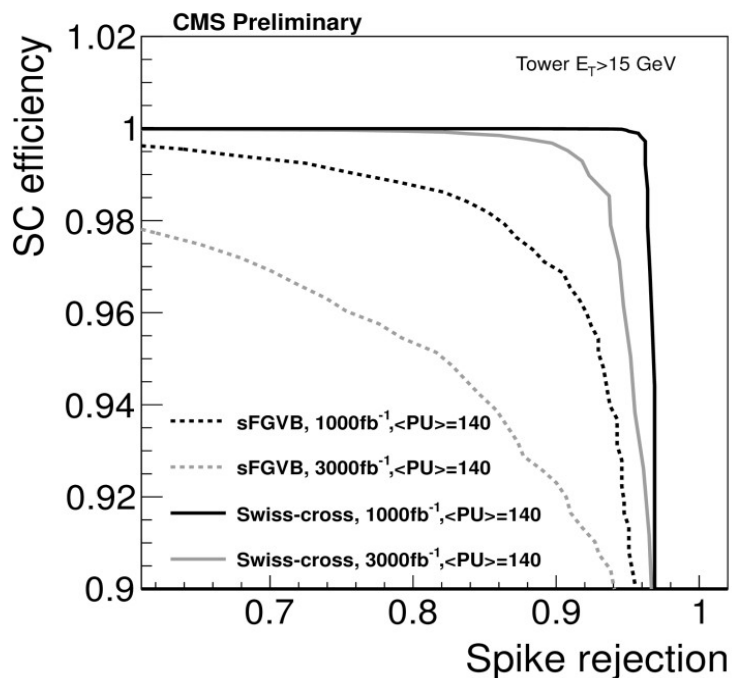
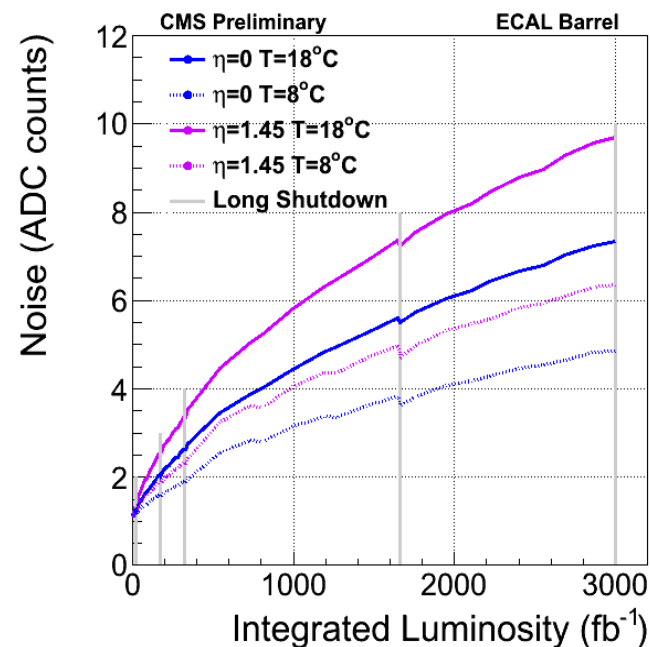
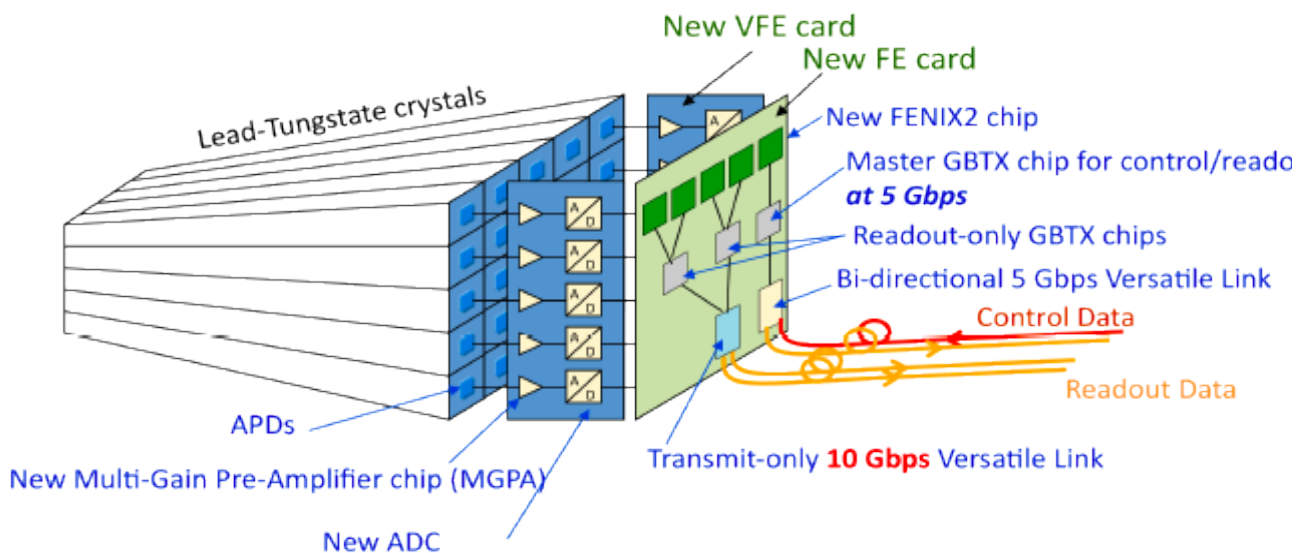


Trigger Algorithm	Level-1 Trigger with L1 Tracks	
	Rate [kHz]	Offline Threshold(s) [GeV]
Single Mu (tk)	14	18
Double Mu (tk)	1.1	14 10
ele (iso tk) + Mu (tk)	0.7	19 10.5
Single Ele (tk)	16	31
Single iso Ele (tk)	13	27
Single $\gamma$ (tk-veto)	31	31
ele (iso tk) + e/ $\gamma$	11	22 16
Double $\gamma$ (tk isol)	17	22 16
Single Tau (tk)	13	88
Tau (tk) + Tau	32	56 56
ele (iso tk) + Tau	7.4	19 50
Tau (tk) + Mu (tk)	5.4	45 14
Single Jet	42	173
Double Jet (tk)	26	2@125
Quad Jet (tk)	12	4@72
Single ele (tk) + Jet (tk)	15	23 66
Single Mu (tk) + Jet (tk)	8.8	16 66
Single ele (tk) + $H_T^{\text{miss}}$ (tk)	10	23 95
Single Mu (tk) + $H_T^{\text{miss}}$ (tk)	2.7	16 95
$H_T$ (tk)	13	350
Rate for above Triggers	180	
<b>Est. Total Level-1 Menu Rate</b>	<b>260</b>	





# Barrel Calorimetry



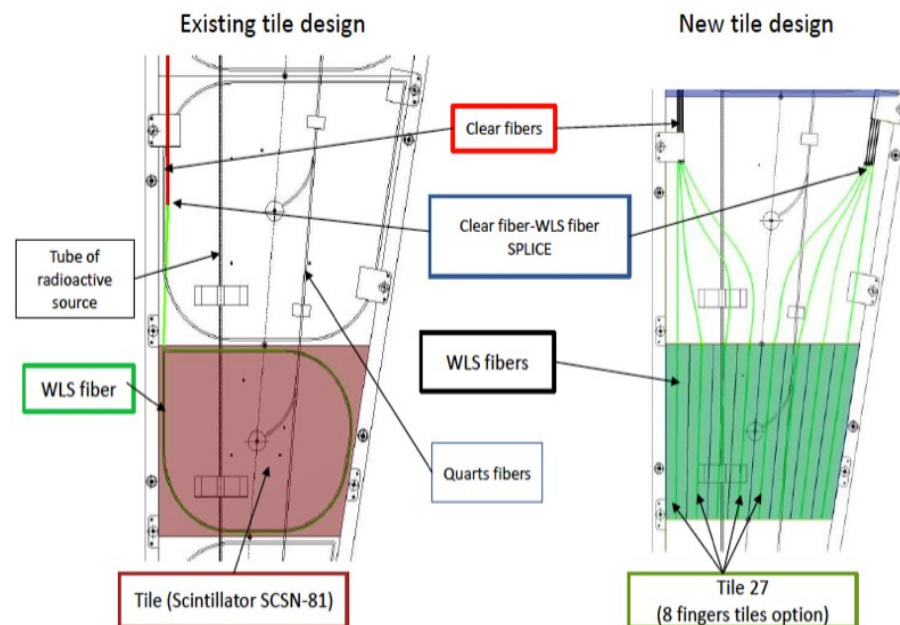
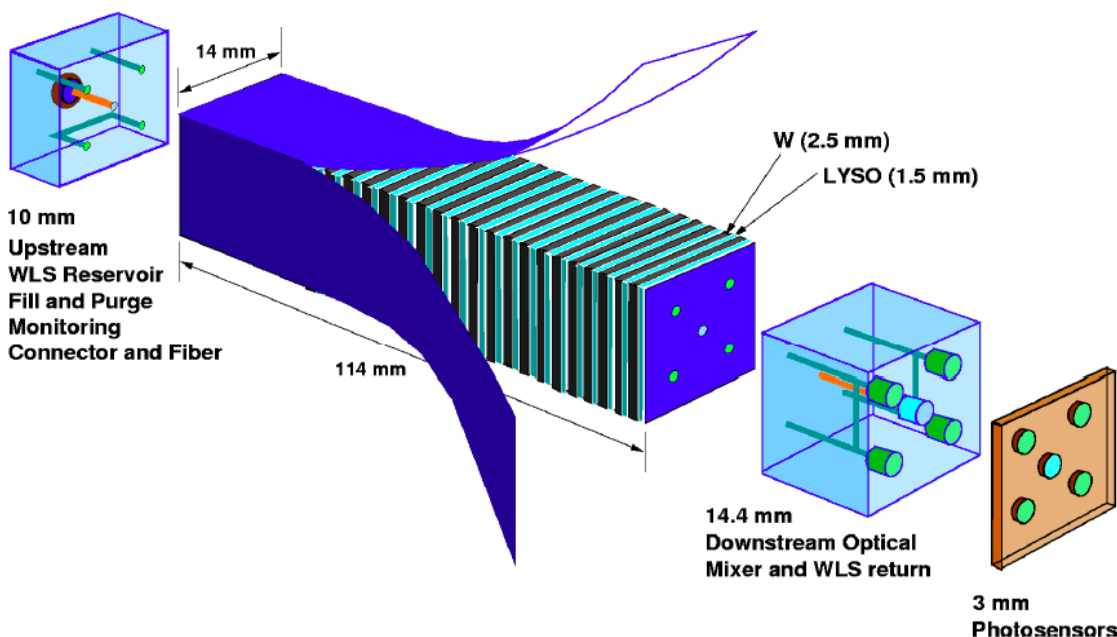
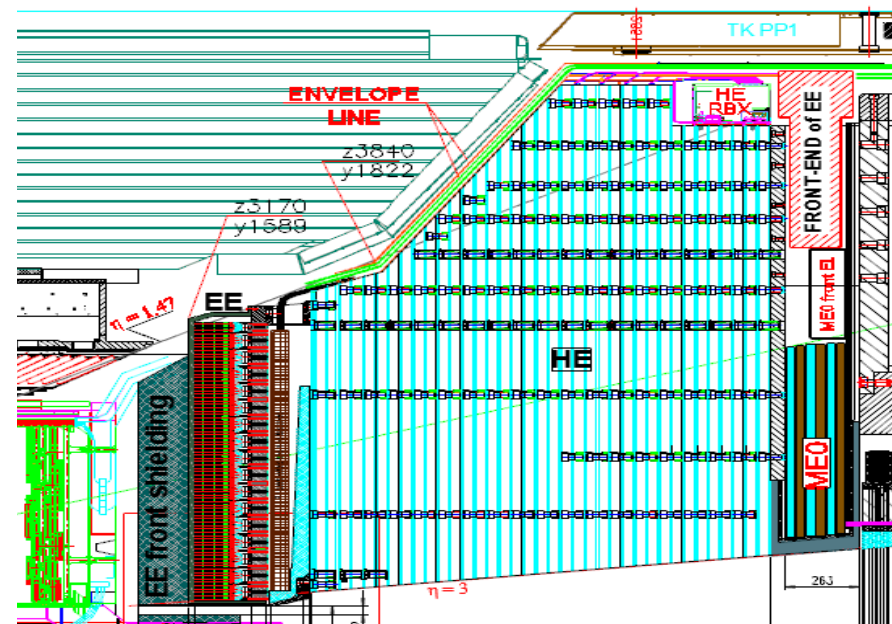
- New on-detector electronics needed to meet requirements for track trigger latency
- Replacement allows trigger-level readout of each crystal and new shaping to reduce impact of out-of-time pileup and increasing APD noise



# Concept 1: Shashlik + Scintillator HE

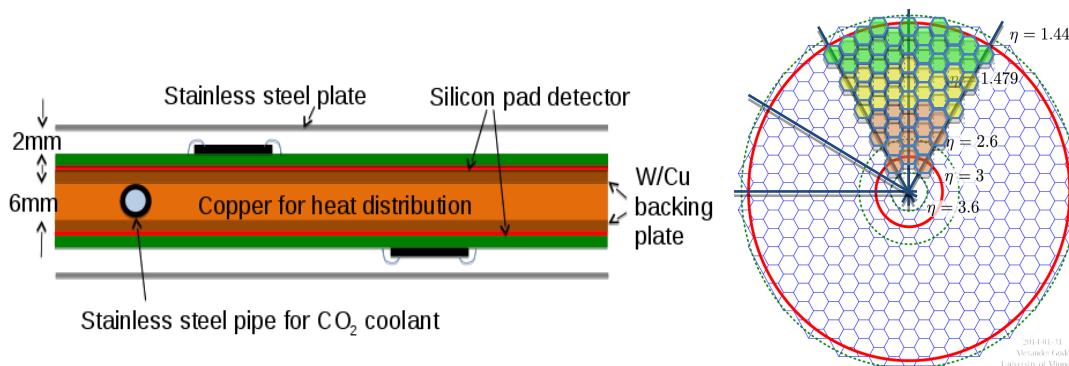
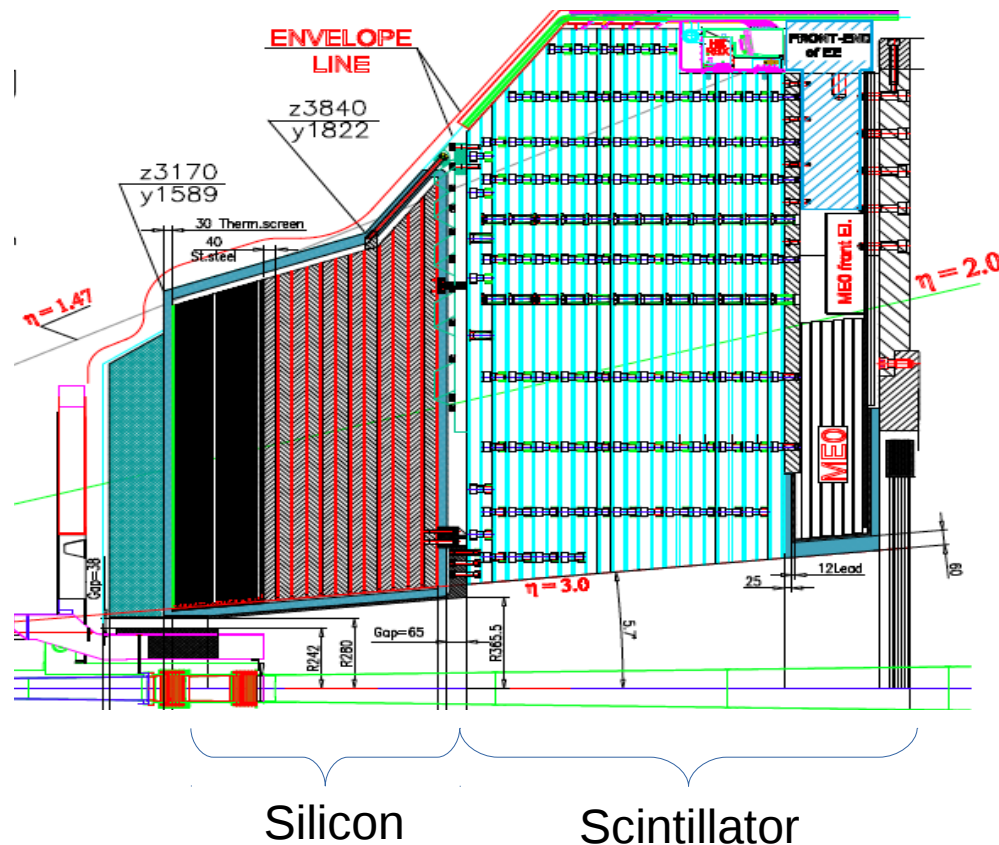


- EM Calorimeter
  - Compact Pb/LYSO Shashlik using WLS based on quartz capillaries and readout using GaInP “SiPMs”
- Hadron Calorimeter
  - Scintillator-based hadron calorimeter with 30% of volume replaced by “finger tiles” and 10% by a solution with higher radiation tolerance





- Silicon readout for front portion of calorimeter
  - Si+tungsten/copper EM calorimeter ( $25 X_0$ ,  $1\lambda$ ), 30 layers
  - Si+brass front hadron ( $3.5 \lambda$ ) calorimeter, 12 layers
  - 8.7 M channels, pad sizes  $0.9 \text{ cm}^2$  or  $0.45 \text{ cm}^2$  depending on  $\eta$
- Scintillator-brass backing calorimeter ( $5.5 \lambda$ )
- Goal is to suppress pileup effects by using information on shower development provided by high level of granularity
  - Informed by experience of ILC R&D

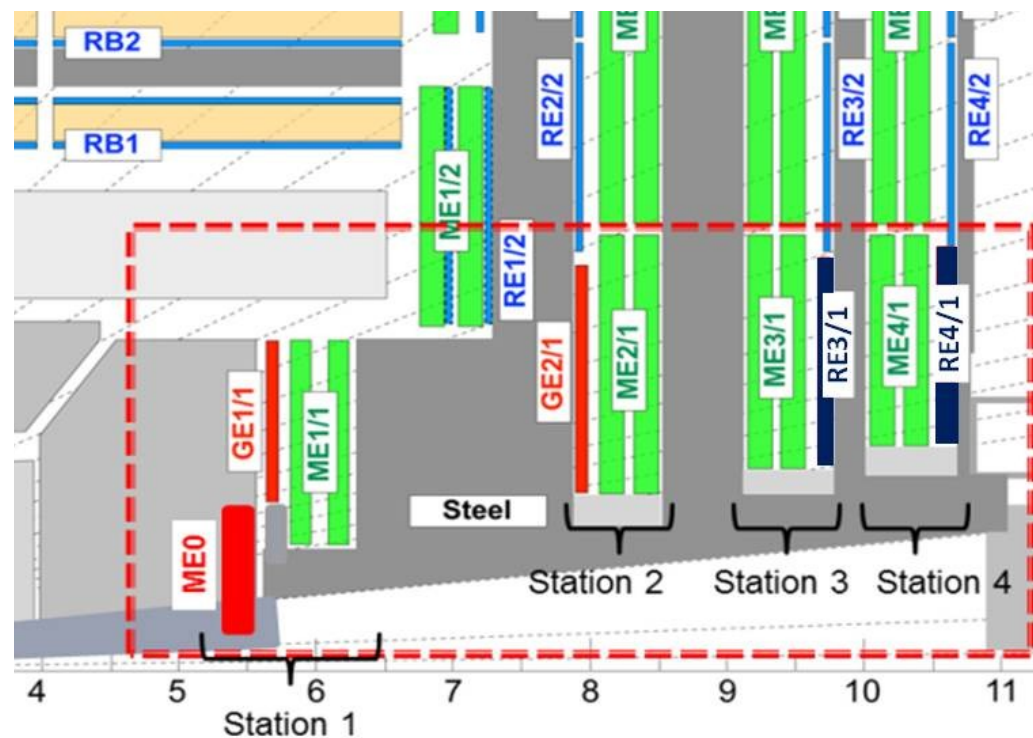




# Muon System Upgrades



- Improvements of existing detectors
  - Electronics: DT minicrates, CSC inner MEx/1 readout
    - Both are needed for compliance with trigger upgrade
- Forward  $1.6 < |\eta| < 2.4$  upgrades
  - L1 trigger rate reduction, enhance redundancy
  - GEMs: GE1/1 and GE2/1
  - iRPCs: RE3/1 and RE4/1
    - Operation in higher rate
    - Technology to be selected
- Very forward extension
  - Extend muon tagging
  - ME0 with GEMs
  - 6 layer stub
  - Baseline  $2.0 < |\eta| < 3.0$ 
    - Depends on calorimetry



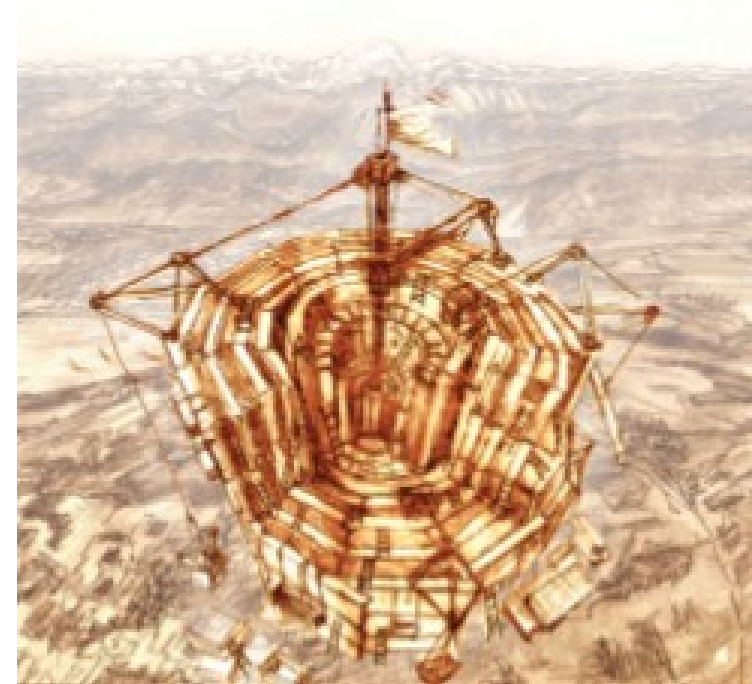


# Moving forward



Calendar Year											
2014	2015	2016	2017	2018	2019	2220	2021	2222	2023	2024	2025
	TP										
Technology R&D											
		TDRs									
Design and Prototyping											
			Engineering Design								
			Pre-Production								
				Production / Construction							
									Install / Commission		

- CMS is preparing a Technical Proposal including physics performance studies, to be completed by March 2014
  - Decision on endcap calorimeter technology planned for early 2015





# Conclusion



- Run 2 and Run 3 of LHC will open a new energy regime, hopefully leading to major new discoveries
  - The Phase 1 Upgrades of CMS will support the physics program of these LHC runs and are moving to construction: Pixels, HCAL, L1 Trigger
  - Major US leadership in all three upgrade efforts
- The HL-LHC will allow for precision studies of the Higgs as well as allowing the identification and characterization of discoveries made in Run 2 and 3.
  - CMS is preparing a technical proposal detailing the plans for upgrades allowing the same physics performance for 140 pileup and  $3000 \text{ fb}^{-1}$  as CMS had in Run 1
  - US scientific and technical efforts will be critical to the success of the HL-LHC physics program