“Fast” Readout Electronics (high resolution, fast throughput)

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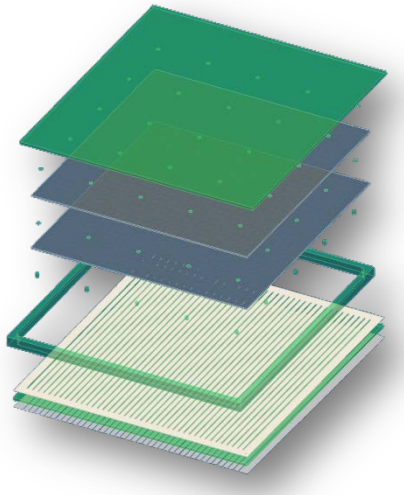
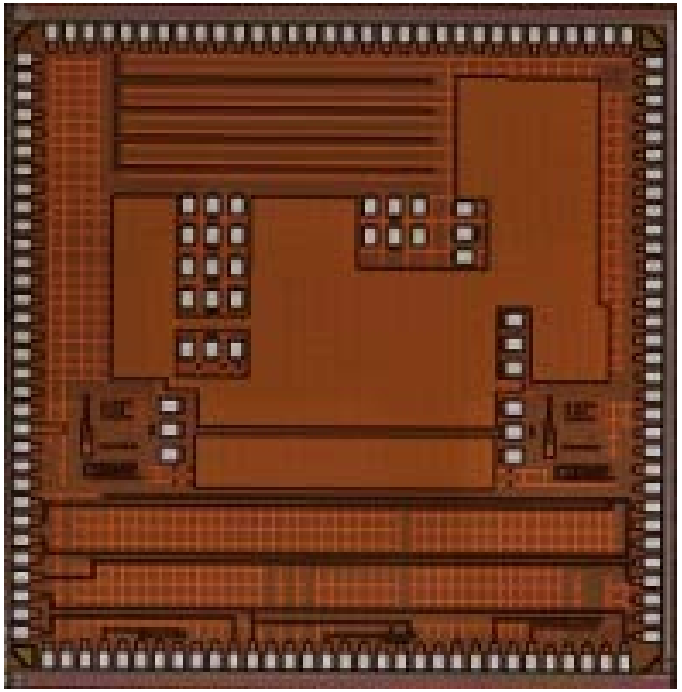
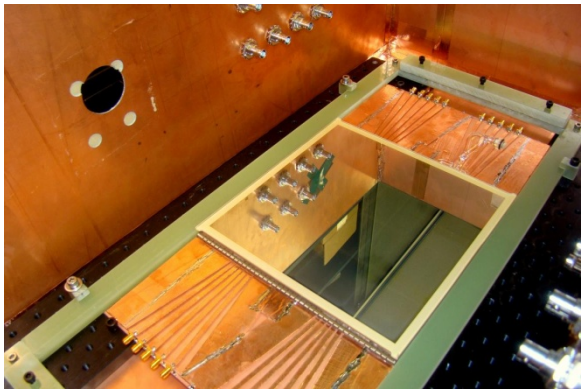
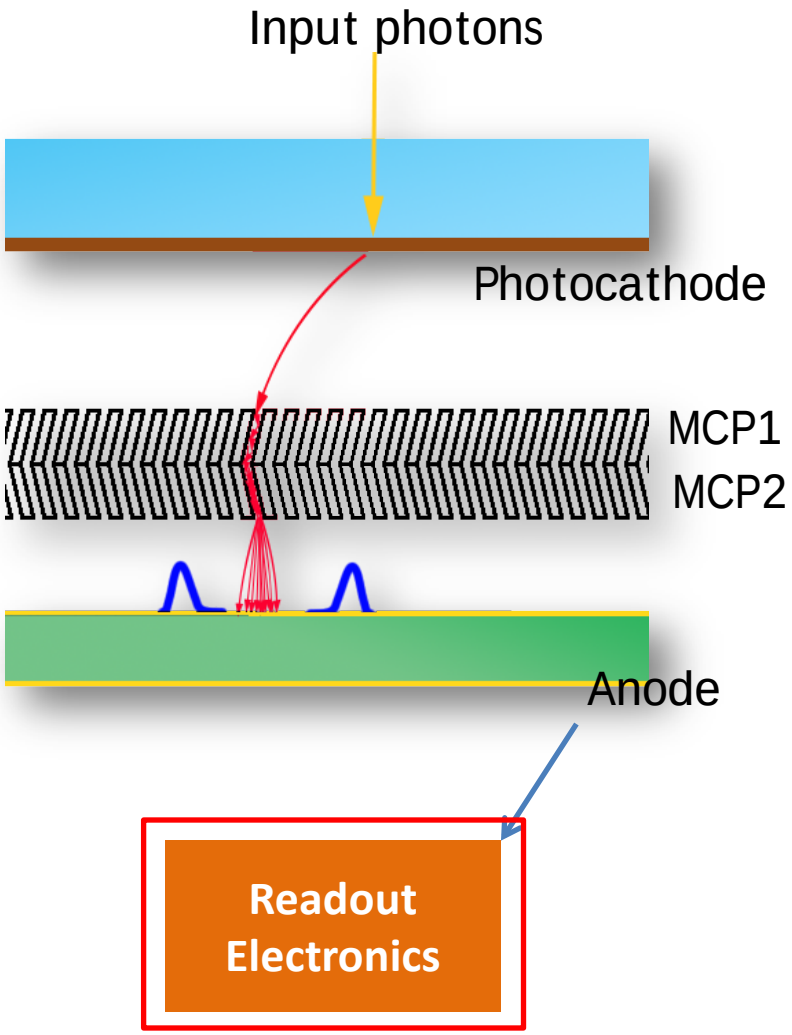






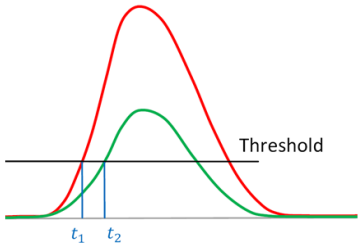
Elements of an MCP-PMT



- Photocathode
- Micro-channel plates
- Collection anode
- **Readout electronics**
- Mechanical design / tile assembly.

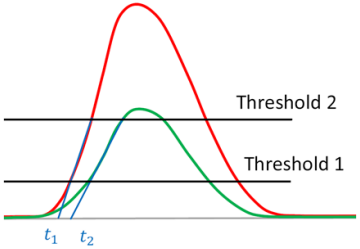
Timing Methods

Single threshold



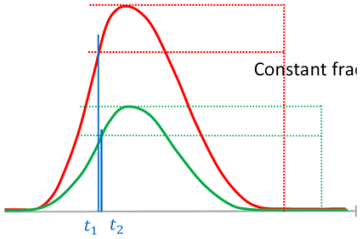
The single threshold is the least precise time extraction measurement. It has the advantage of simplicity.

Multiple threshold



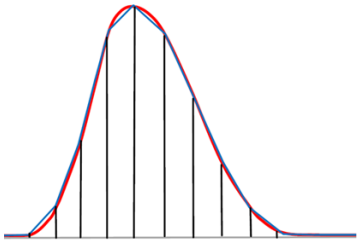
The multiple threshold method takes into account the finite slope of the signals. It is still easy to implement.

Constant fraction



The constant fraction algorithm is very often used due to its relatively good performance and its simplicity.

Waveform sampling



Waveform sampling above the Nyquist frequency is the best algorithm since it is preserves the signal integrity.

In principle, sampling above the Nyquist-Shannon frequency and fully reconstructing the signal attains the best timing information.

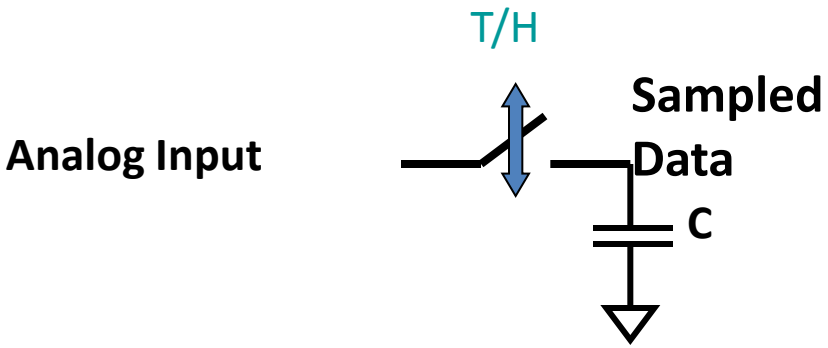
Attrib. Jean-Francois Genat

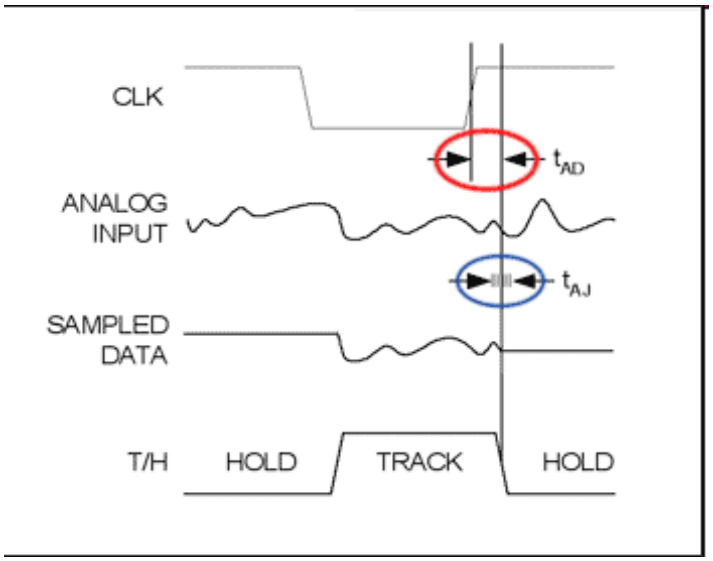
Continued Evolution

- CFD + TDC or Discrim. + TDC + Q/Vpeak are well established techniques
  - Next generation HPTDC @ CERN
  - NINO and other front-ends
- Recent years has seen explosive growth in evolution of Switched Capacitor Array waveform samplers
- Best choice can be application-specific
- Will review results/projections
- Interesting convergence of technologies

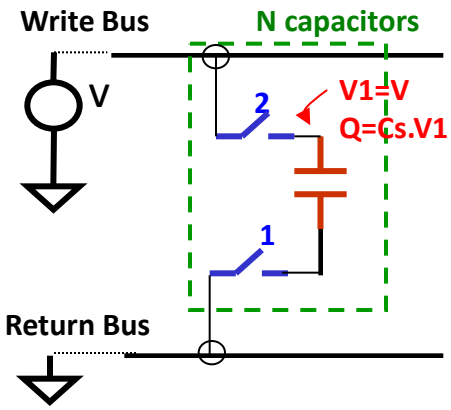
SCA Underlying Technology

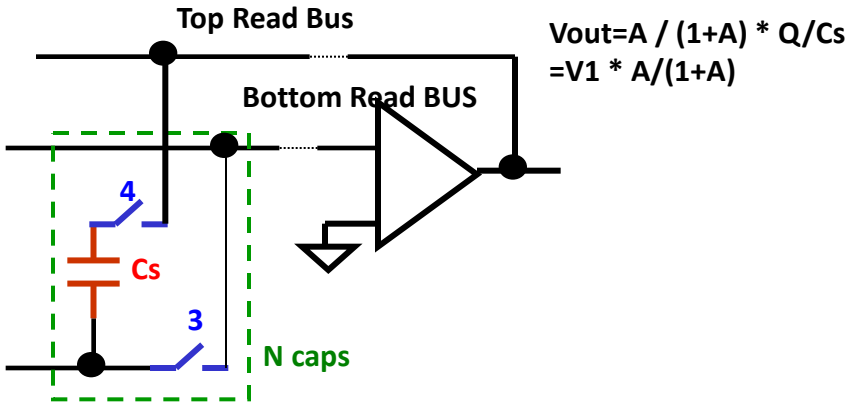
- Track and Hold (T/H)





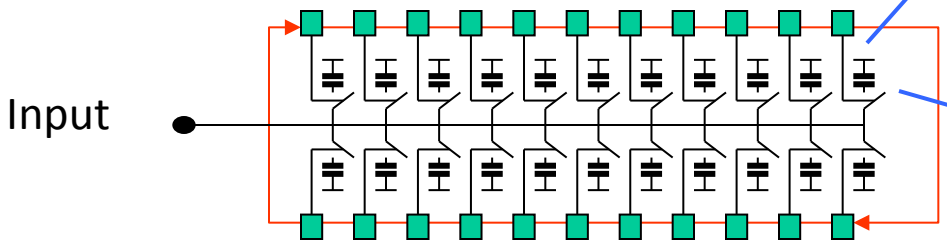
- Pipelined storage = array of T/H elements, with output buffering

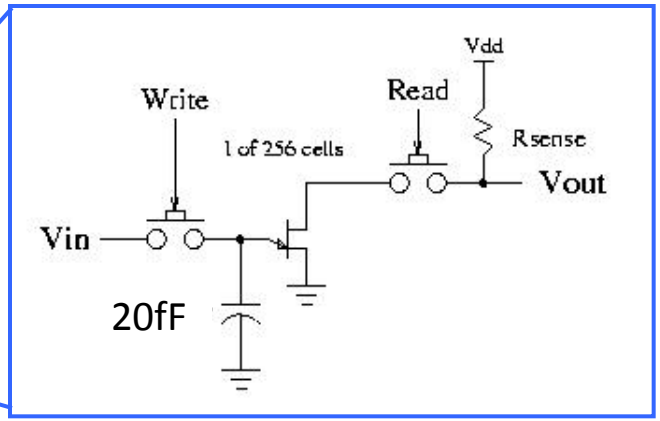




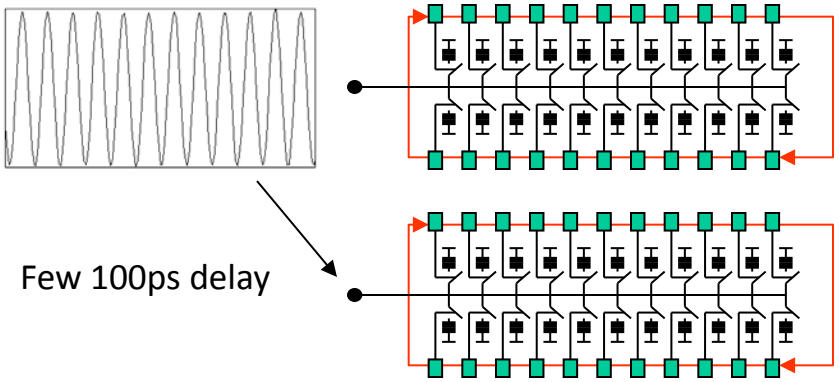
Switched Capacitor Array Sampling

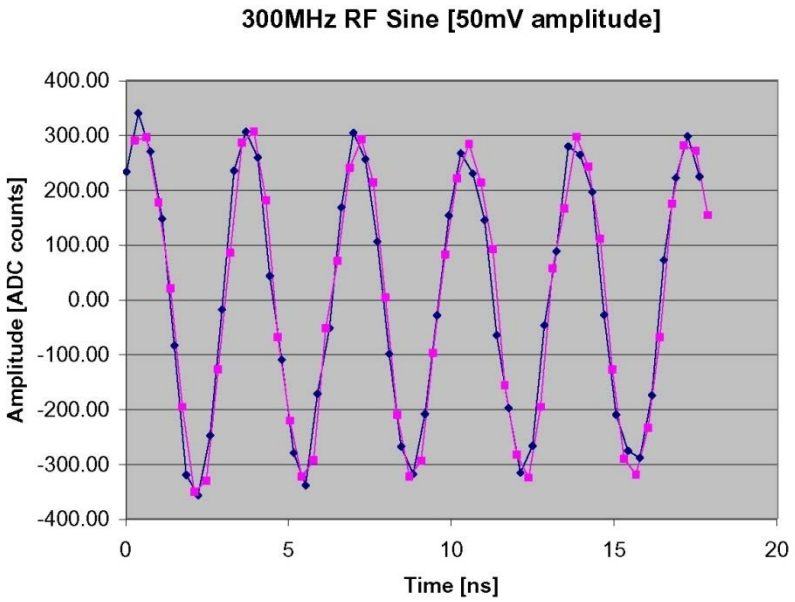
- Write pointer is ~few switches closed @ once



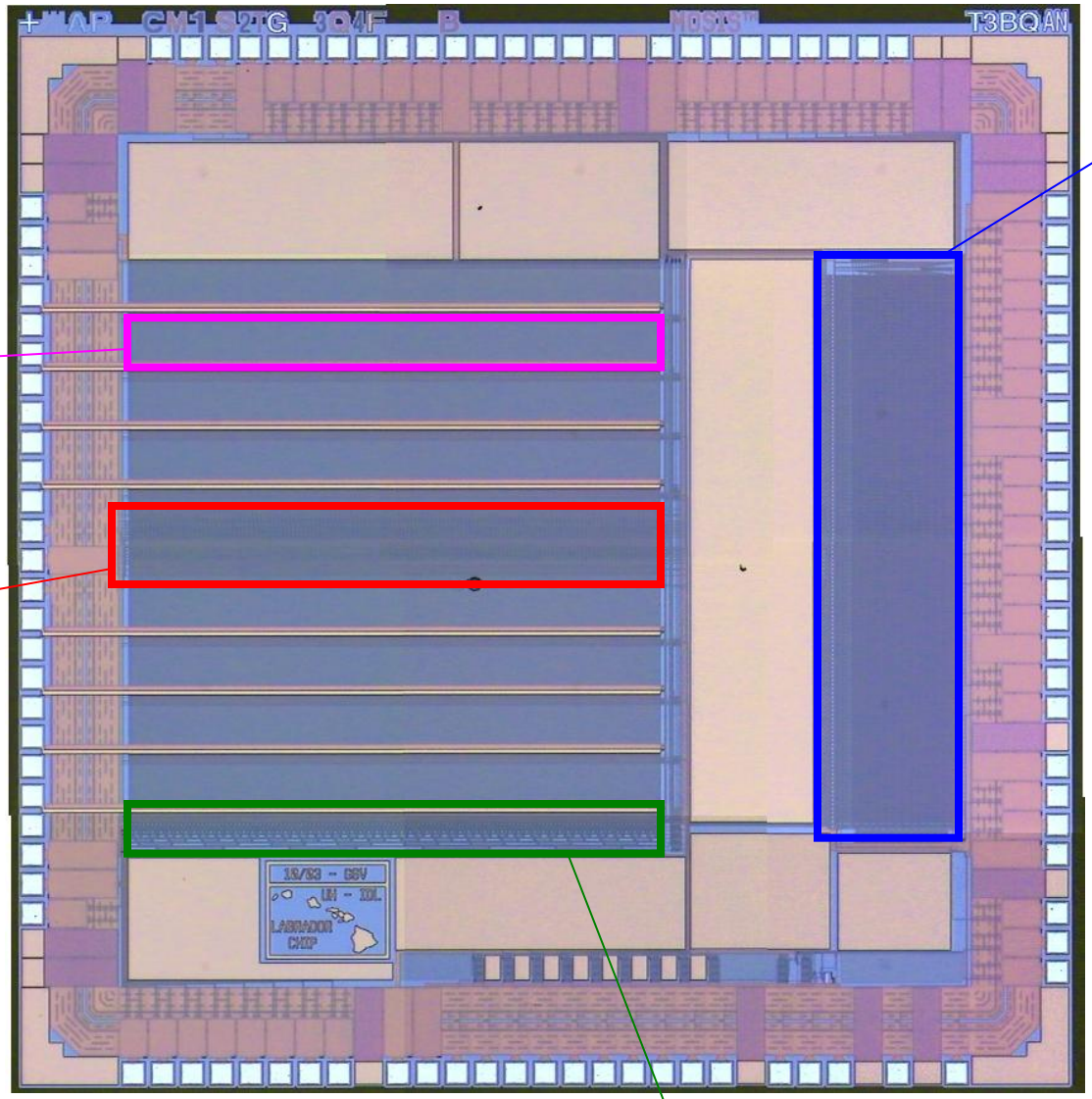


Tiny charge: 1mV ~ 100e$^-$





Basic Functional components

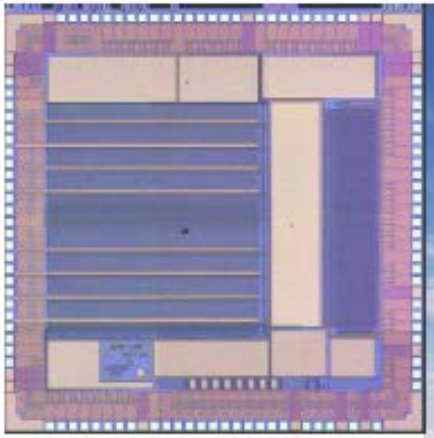


A Portfolio of Waveform samplers

ASIC	Amplification?	# chan	Depth/chan	Sampling [GSa/s]	Vendor	Size [nm]	Ext ADC?
DRS4	no.	8	1024	1-5	IBM	250	yes.
SAM	no.	2	1024	1-3	AMS	350	yes.
IRSX	no.	8	32536	1-4	TSMC	250	no.
BLAB3A	yes.	8	32536	1-4	TSMC	250	no.
TARGET	no.	16	4192	1-2.5	TSMC	250	no.
TARGET2	yes.	16	16384	1-2.5	TSMC	250	no.
TARGETX	no.	16	16384	1-2.5	TSMC	250	no.
RITC	no.	3	Continuous	1-3.7	IBM	130	no.
PSEC4	no.	6	256	1-16	IBM	130	no.

Gen 2 Enabling Technology (ATWD Gen 1)

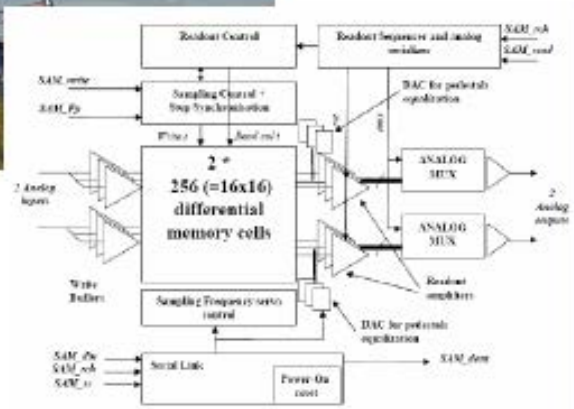
- Already in use in many experiments…

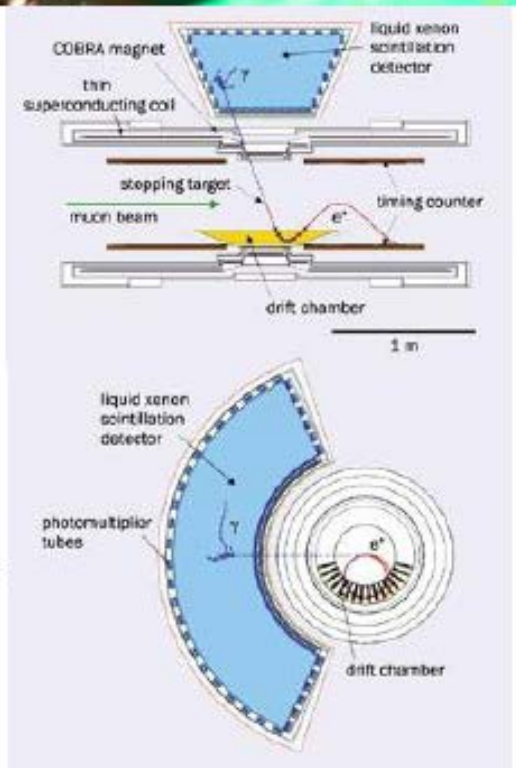


LABRADOR3,
ANITA Experiment

DRS4,
MEG Experiment

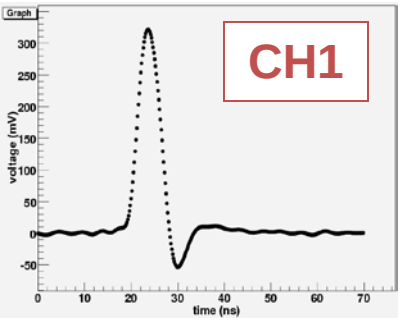
SAM,
H.E.S.S.-II

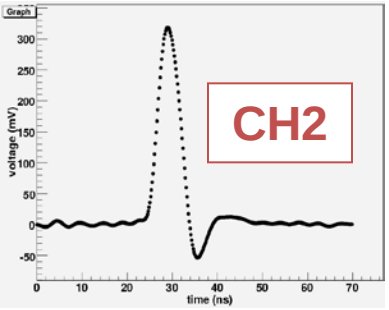


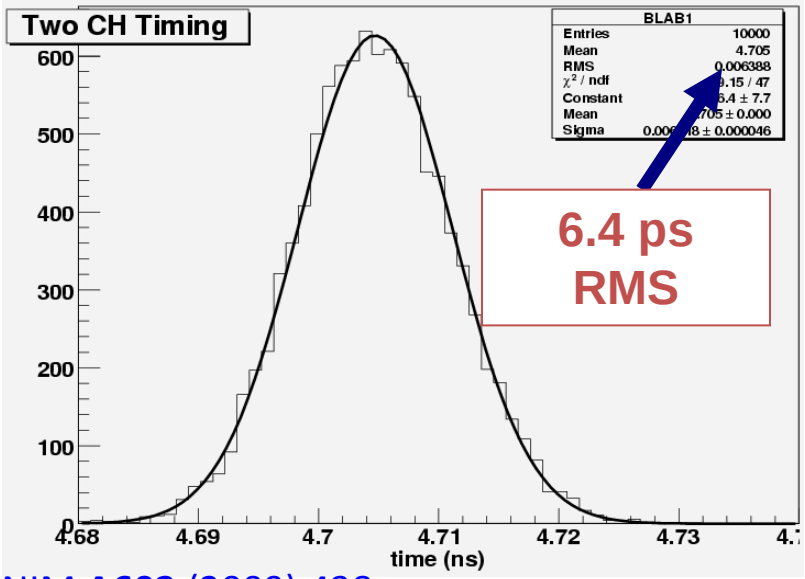


Integrating Readout Electronics

- Detectors and Readout electronics keep pushing each other
  - Readout based on waveform sampling
  - Requirements of the readout vary significantly by application

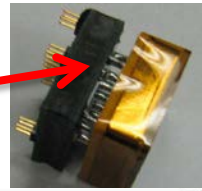


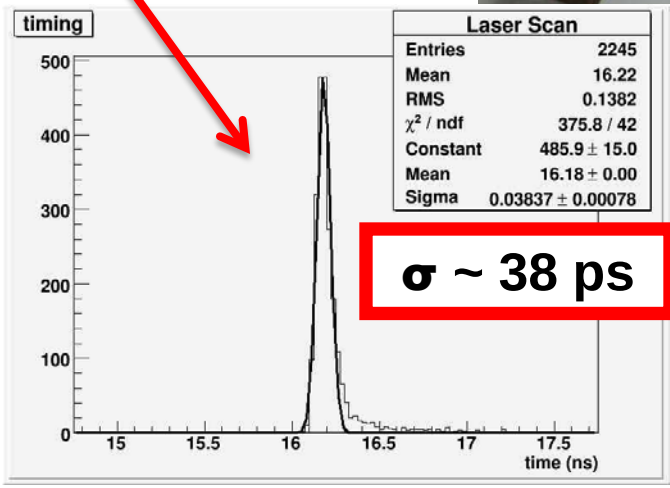




NIM **A602** (2009) 438

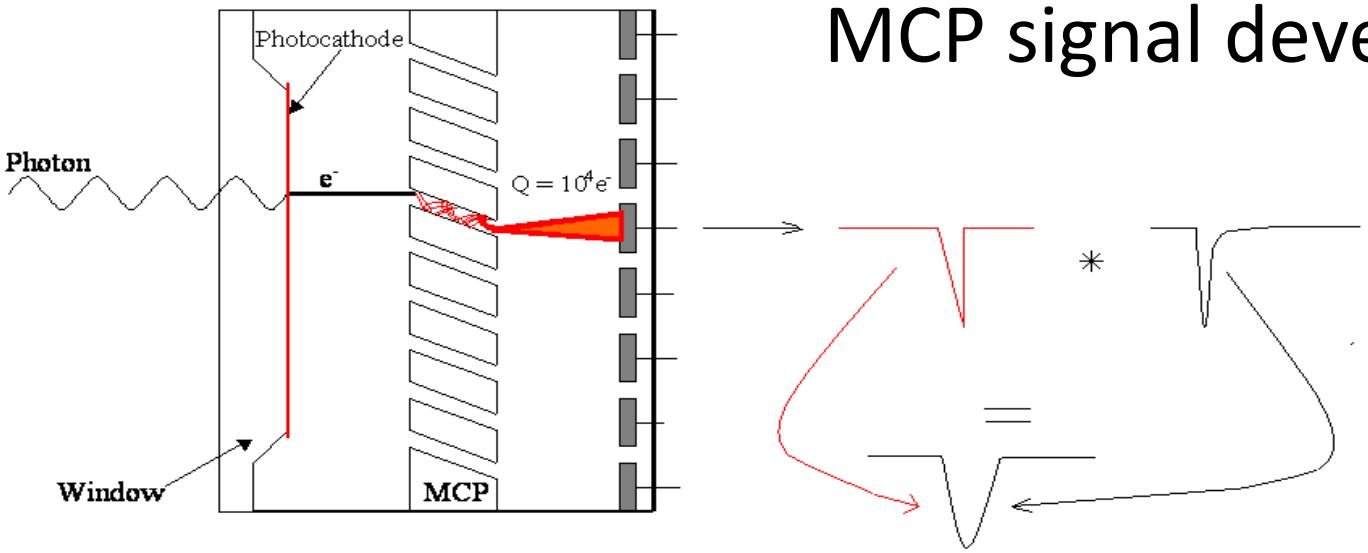
4x4 anode "1 inch"
MCP-PMT (HPK SL-10)





Single p.e. resolution

MCP signal development



MCP signal rising edge: qE = ma $tr = l\sqrt{2m/qV}$

l = 1mm, E=100V/mm, tr=250ps

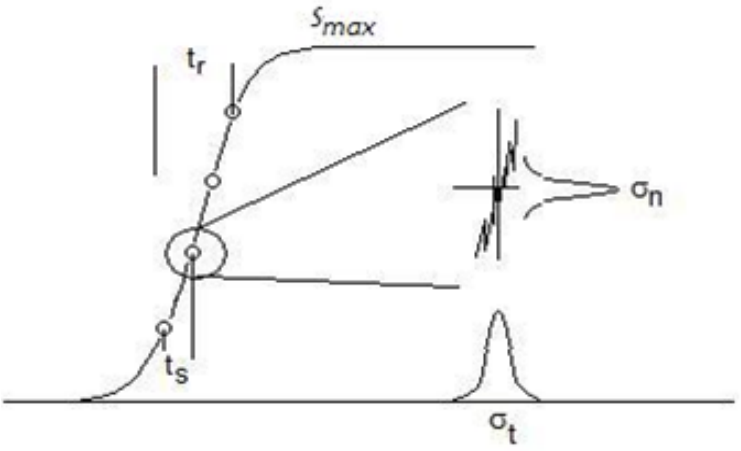
- First gap: 10ps
- Assume 2-stage pores TTS of 20ps
- Anode gap: 10ps
- Noise: 20ps

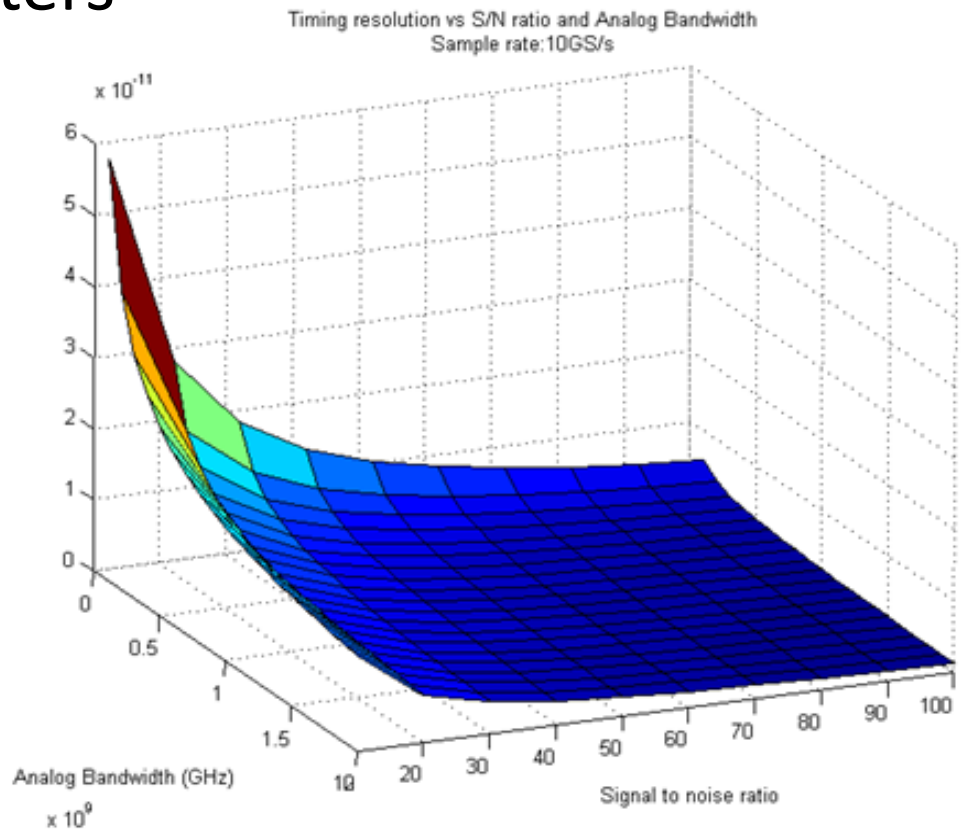
Total is 32ps

(Measured Burle-Photonis 2'' x 2'' is 30ps)

Understanding what matters

Transit Time
Noise$_{detector}$
Rise time
Gain (Signal/noise)





Electronics:
Noise$_{elec}$
Sample rate
Analog bandwidth

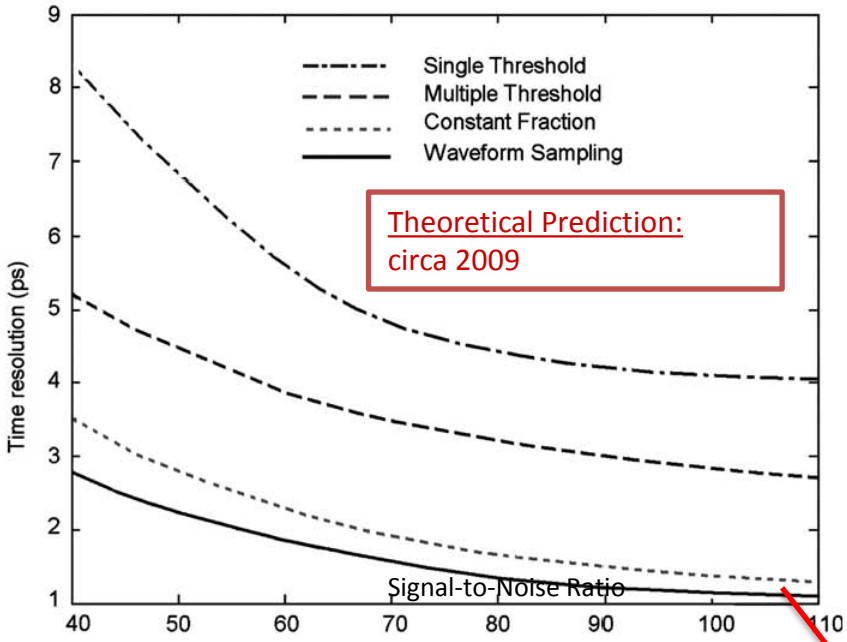
$$SN = S_{max}/\sigma_n \qquad \sigma_{t,n} = \frac{\sigma_n}{\sqrt{n}}$$

$$\sigma_{t,n} = \frac{\sqrt{t_r t_s}}{SN} = \frac{1}{SN}\sqrt{0.35 t_s \, abw}$$

$\sigma_n = \sigma_{n\,det} + \sigma_{n\,elec}$

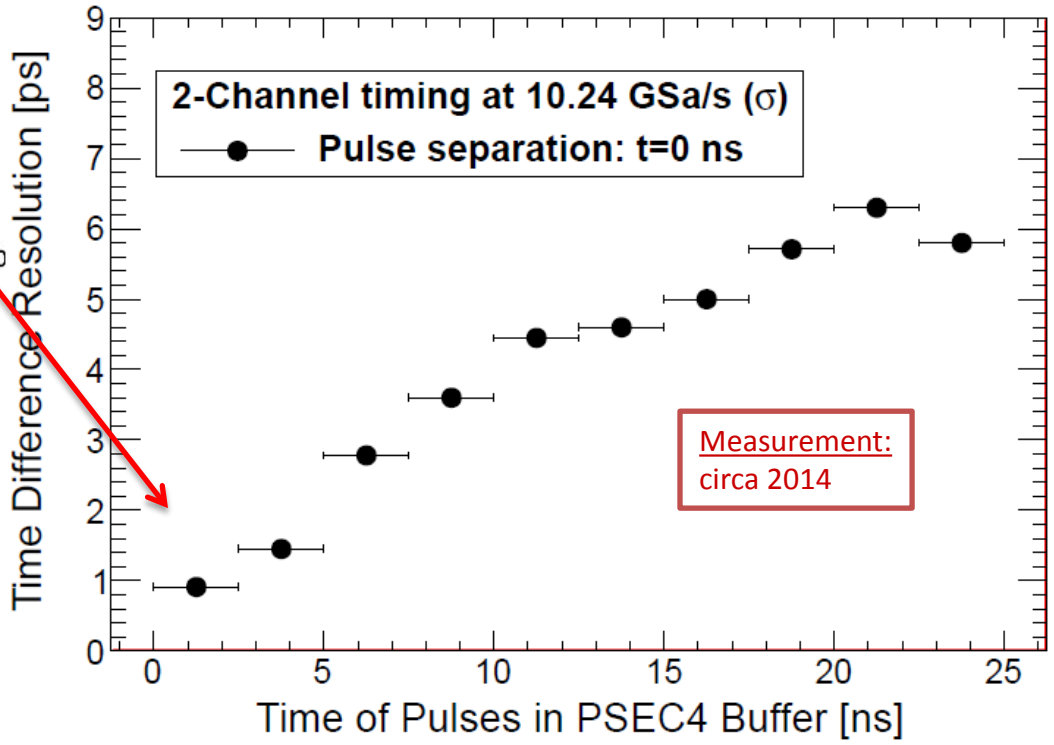
$$S = G\ Npe$$

ps Timing Resolution



Theoretical Prediction:
circa 2009

Extending to 1ps and lower, with advanced calibration techniques



Measurement:
circa 2014

The “no free lunch” Theorem

- Excellent results obtained

  1. Has made ANITA and other projects possible & highly successful

  2. Similar architectures being studied for new and upgraded experiments

  3. Minimize costs for large systems

- Not a magic solution
  - Significant/important constraints
  - Technology in its adolescence – will continue to improve

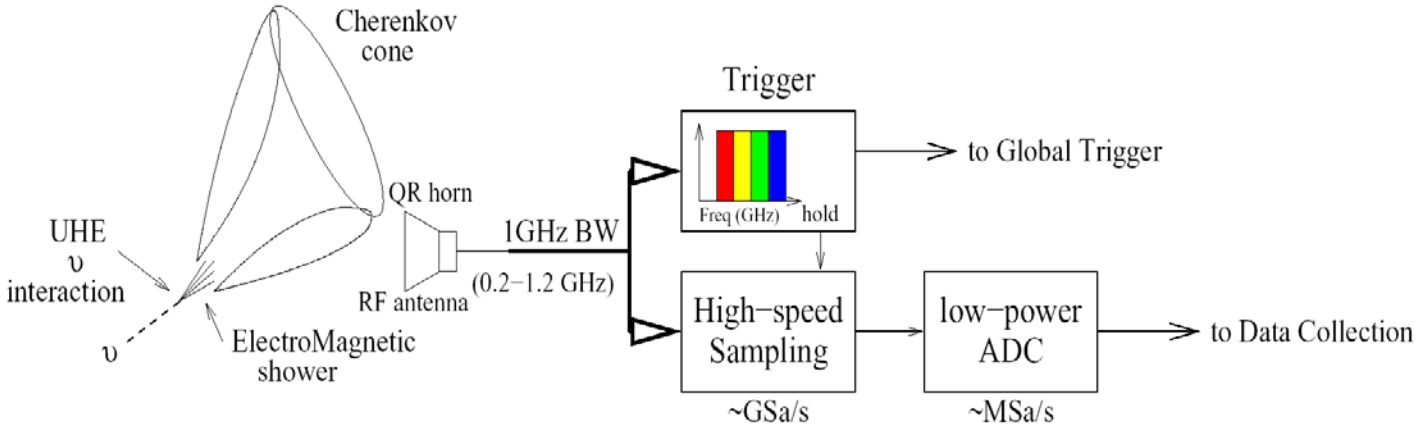
- Limits and future directions

First, the current limitations, in a bit more detail

Constraint 0: An Intrinsic Limitation

No power (performance savings) for continuous digitization

Won't displace Flash ADCs

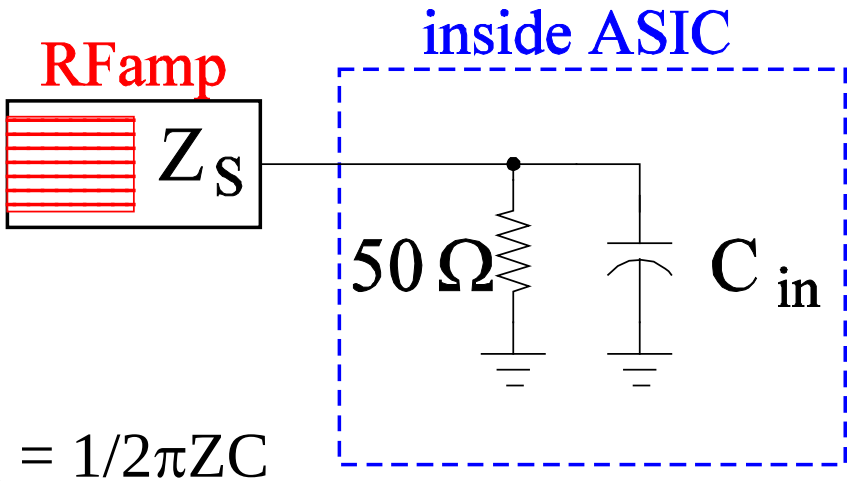


"down conversion"

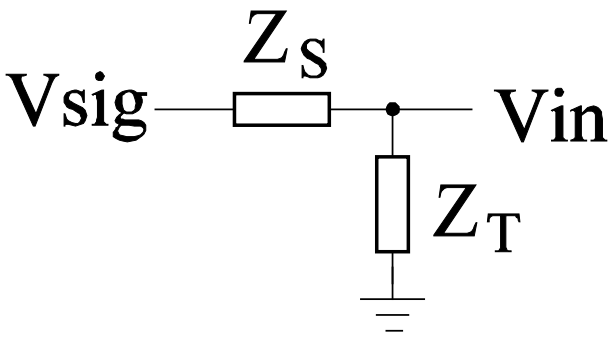
→ For most "triggered" 'event' applications, *not a serious drawback*

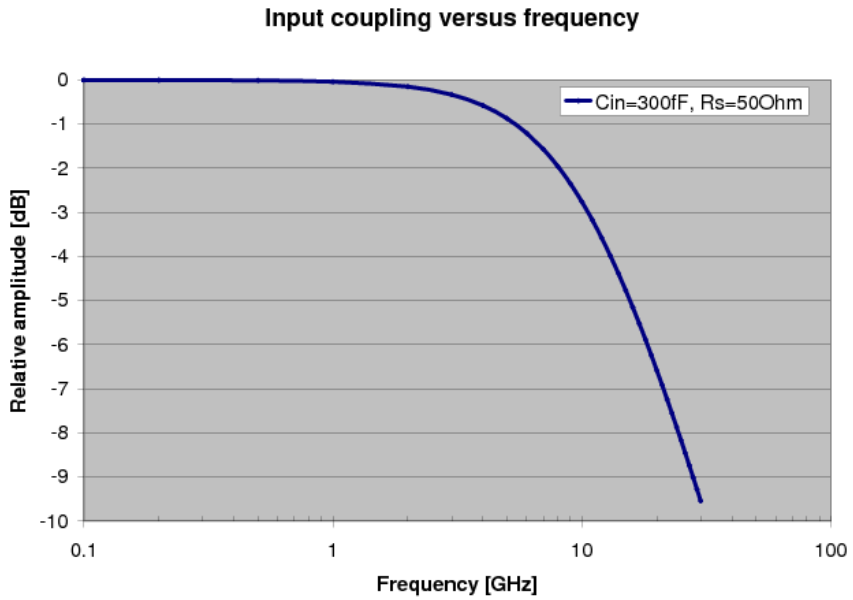
Constraint 1: Analog Bandwidth

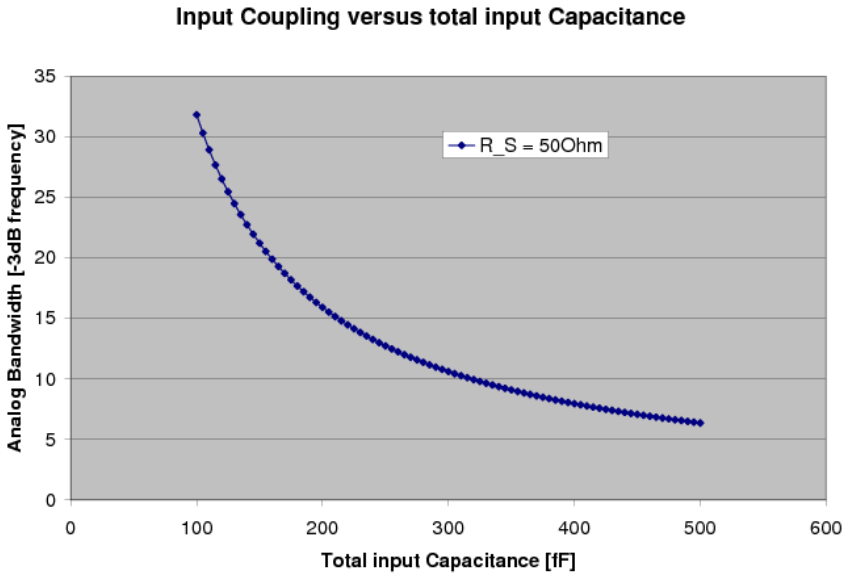
Difficult to couple in Large BW (C is deadly)



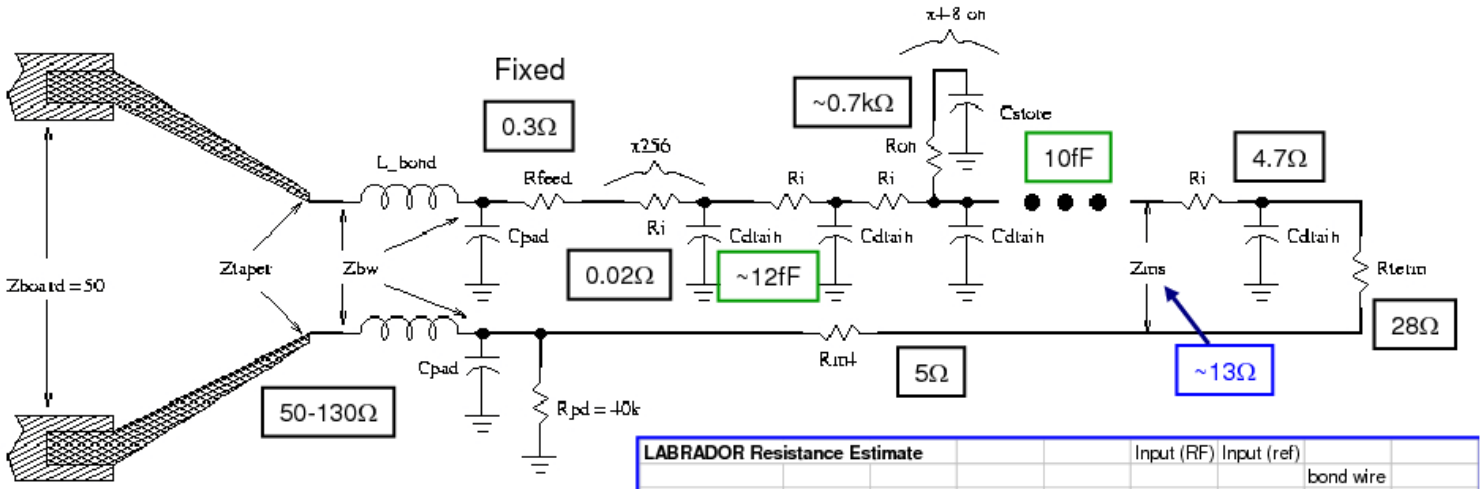
$f_{3dB} = 1/2\pi ZC$

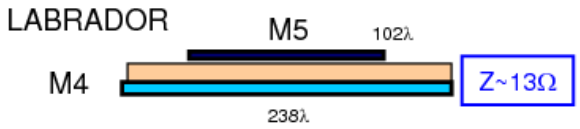






Constraint 2: Storage Depth





LABRADOR Resistance Estimate					Input (RF)	Input (ref)	
							bond wire
Length	17000	λ			0.0	0.1	pad
			70			0.2	M5-M4
Metal 4(sheet) =	0.07	Ohm/sq		71.42857		5.0	typ length (sq.)
Metal 5(sheet) =	0.03	Ohm/sq	166.6667		5.0		typ length (sq.)
Poly contact =	5.1	Ohm	6	6	0.9	0.9	
via 1=	2.7	Ohm	6	3	0.5	0.9	
via 2=	5.35	Ohm	6	3	0.9	1.8	
via 3=	8.26	Ohm	6	3	1.4	2.8	
via 4=	11.34	Ohm	6		1.9		
					10.5	11.5	Total per feed
						28	Rterminator
		Measured:		Ohm		**50.0**	Grand Total

(LAB1 example)

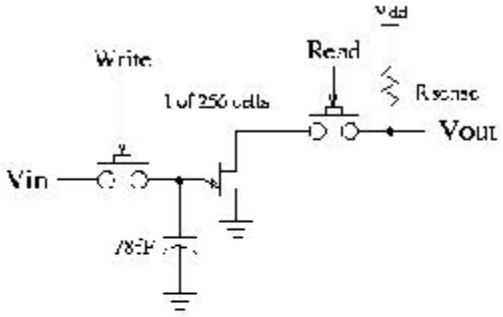
$$f_{3dB} = 1/2\pi ZC$$

Would like smallest possible Cstore

- For 1.2GHz, C <~ 2pF (NB input protection diode ~10pF)
- Minimize C, (C_{drain} not negligible x260)

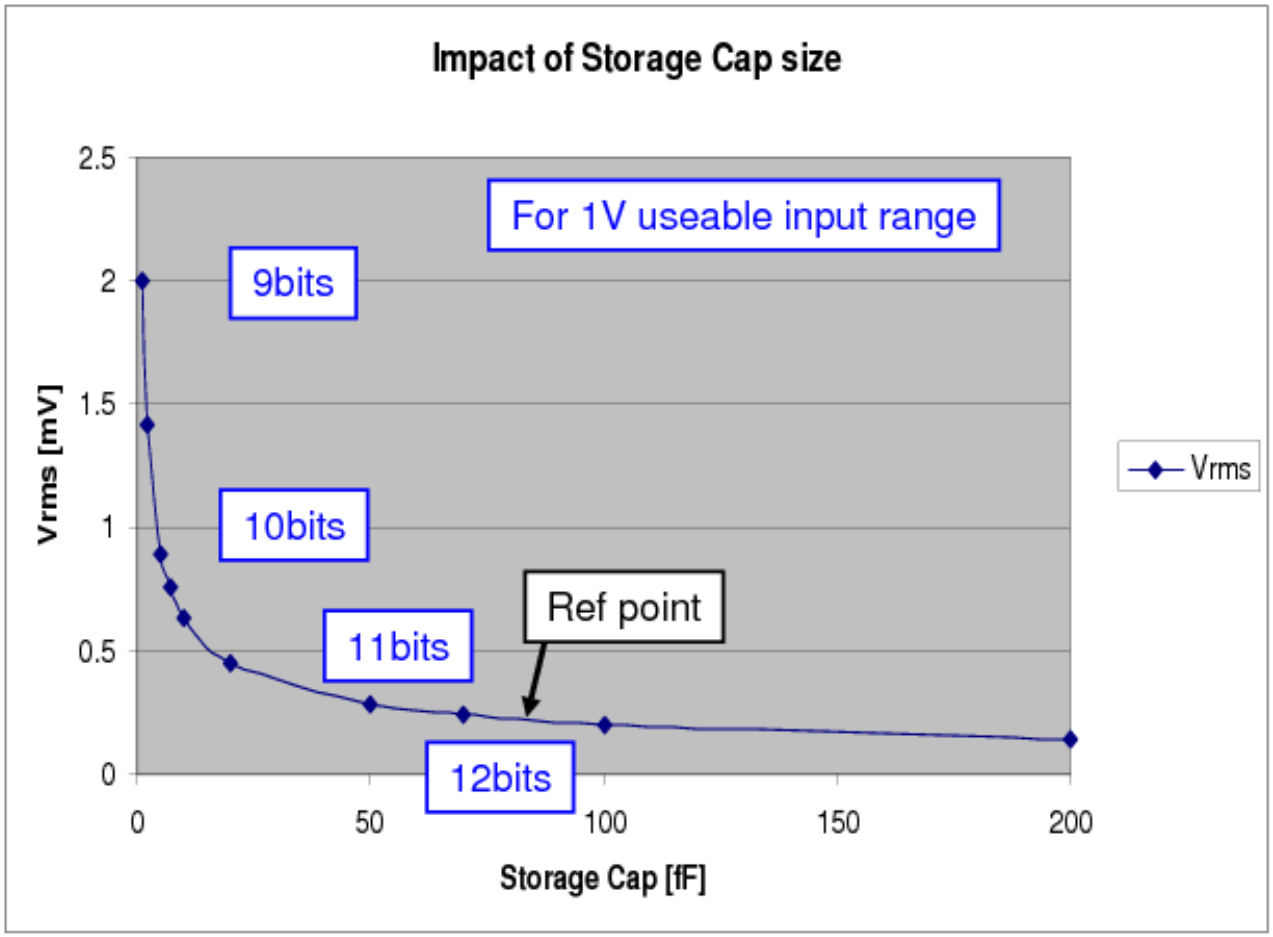
Constraint 3: kTC Noise

Want small storage C, but…



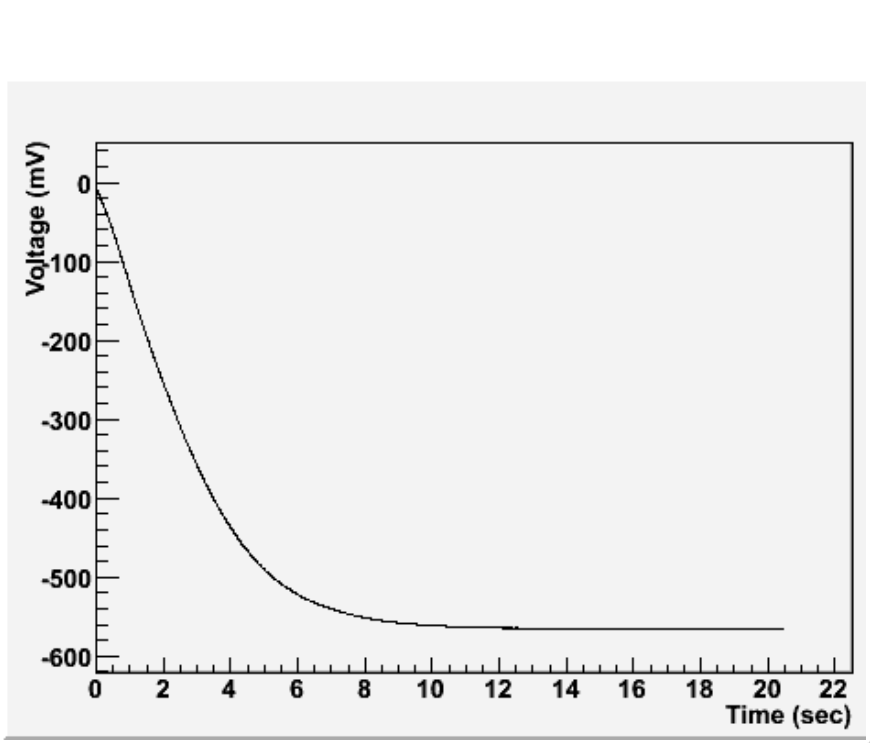
$$v_{rms} = \sqrt{\frac{kT}{C_{store}}} = 0.23mV$$

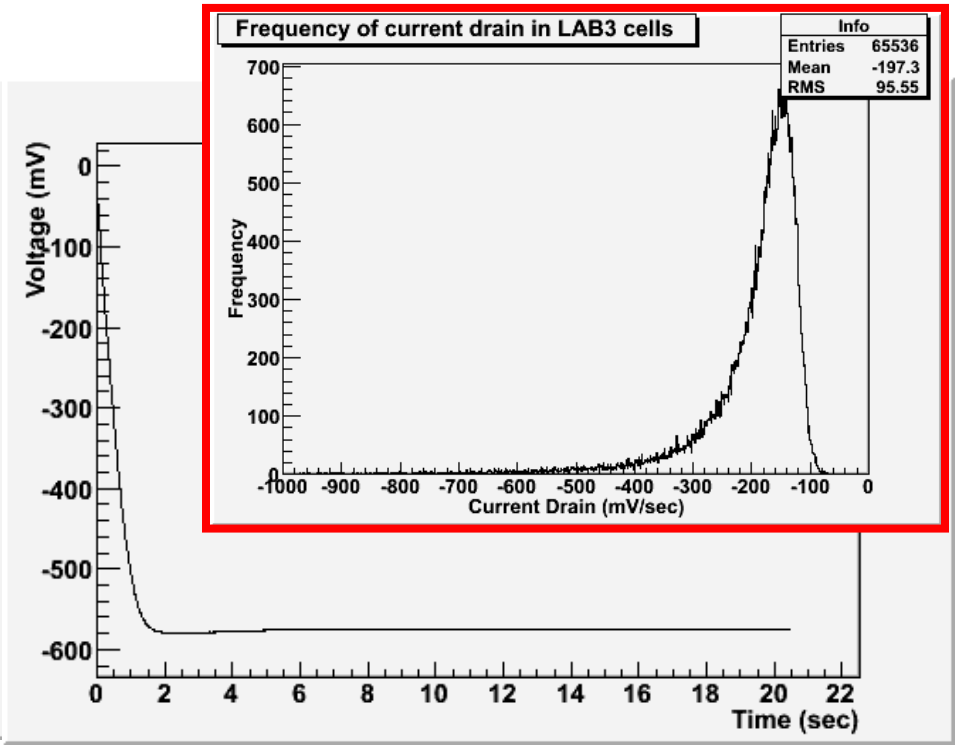
C_{store} = 78fF



Similar Constraint 3b: Leakage Current

Increase C or reduce conversion time << 1mV

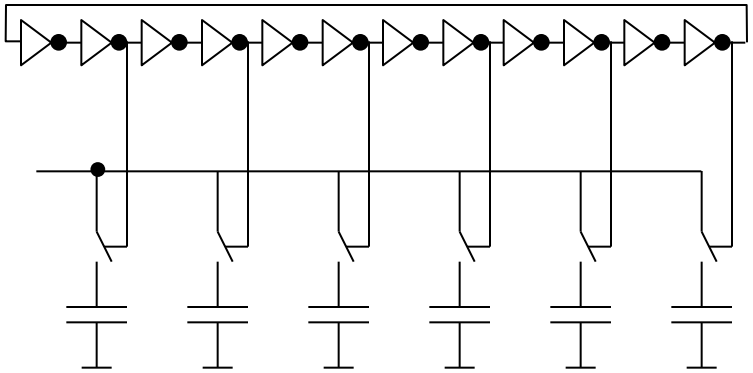


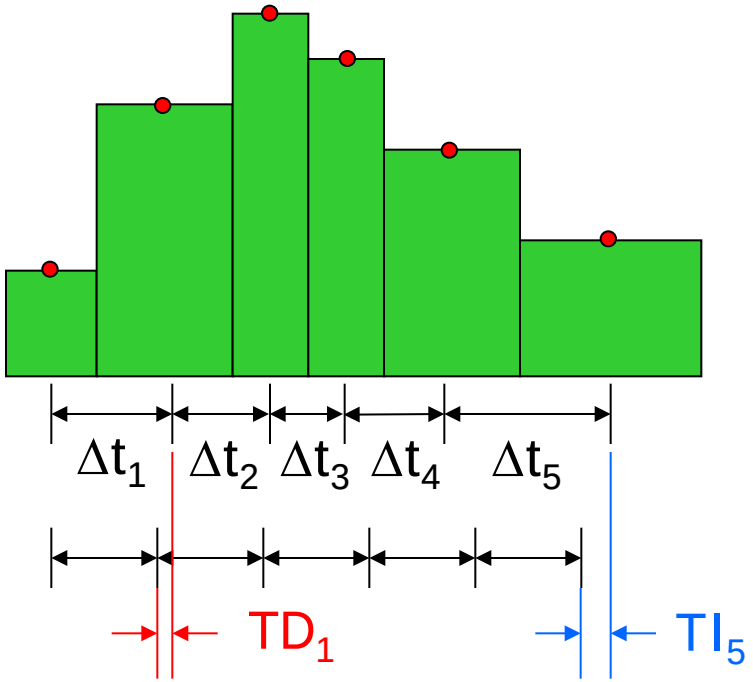


Sample channel-channel variation **~ fA**
leakage typically (0.25um process)

Becomes much worse in faster (digital) processes

Constraint 4: Sample Aperture Variance

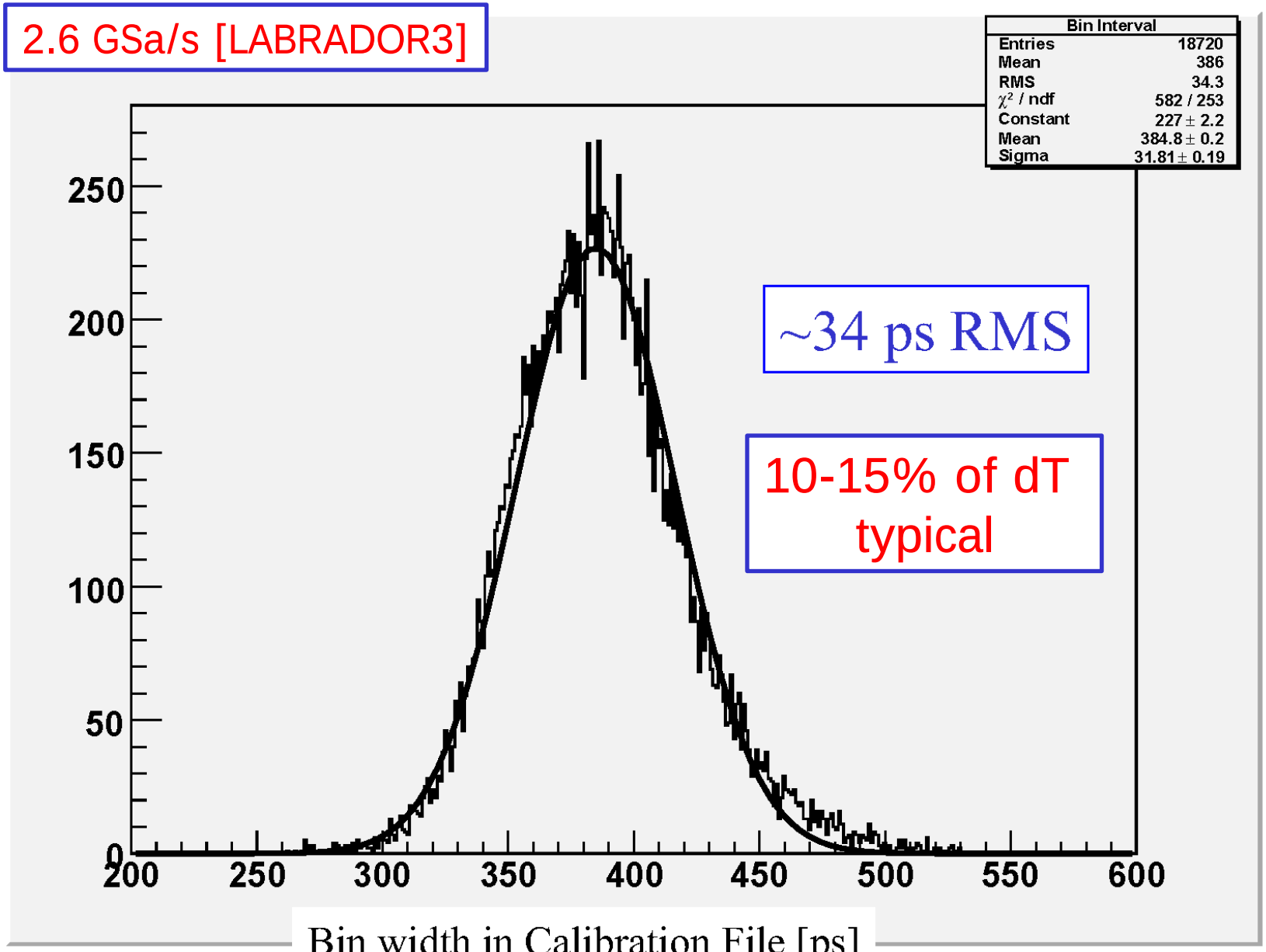




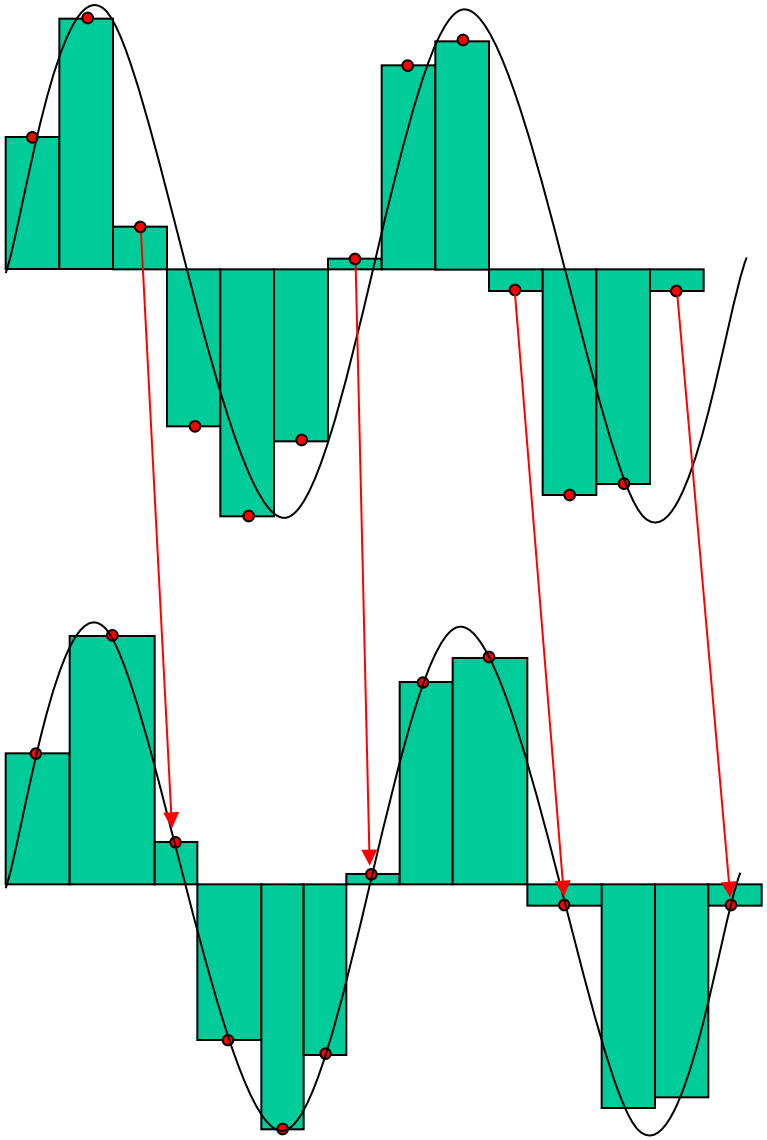
- Inverter chain has transistor variations
  → Δt_i between samples differ
  → "Fixed pattern aperture jitter"
- "Differential temporal nonlinearity"
  $TD_i = \Delta t_i - \Delta t_{nominal}$
- "Integral temporal nonlinearity"
  $TI_i = \Sigma\Delta t_i - i\cdot\Delta t_{nominal}$
- "Random aperture jitter" = variation of Δt_i between measurements

Sample-sample timing “dT” Spread

2.6 GSa/s [LABRADOR3]



Average aperture calibration



- Fixed aperature offsets are constant over time, can be measured and corrected
- Several methods are commonly used (sine fit [left], zero-crossing)
- Most use sine wave with random phase and correct for TD_i on a statistical basis

Great progress in improved algorithms:

http://arxiv.org/abs/1405.4975

However still computationally expensive (e.g. resampling for FFTs)

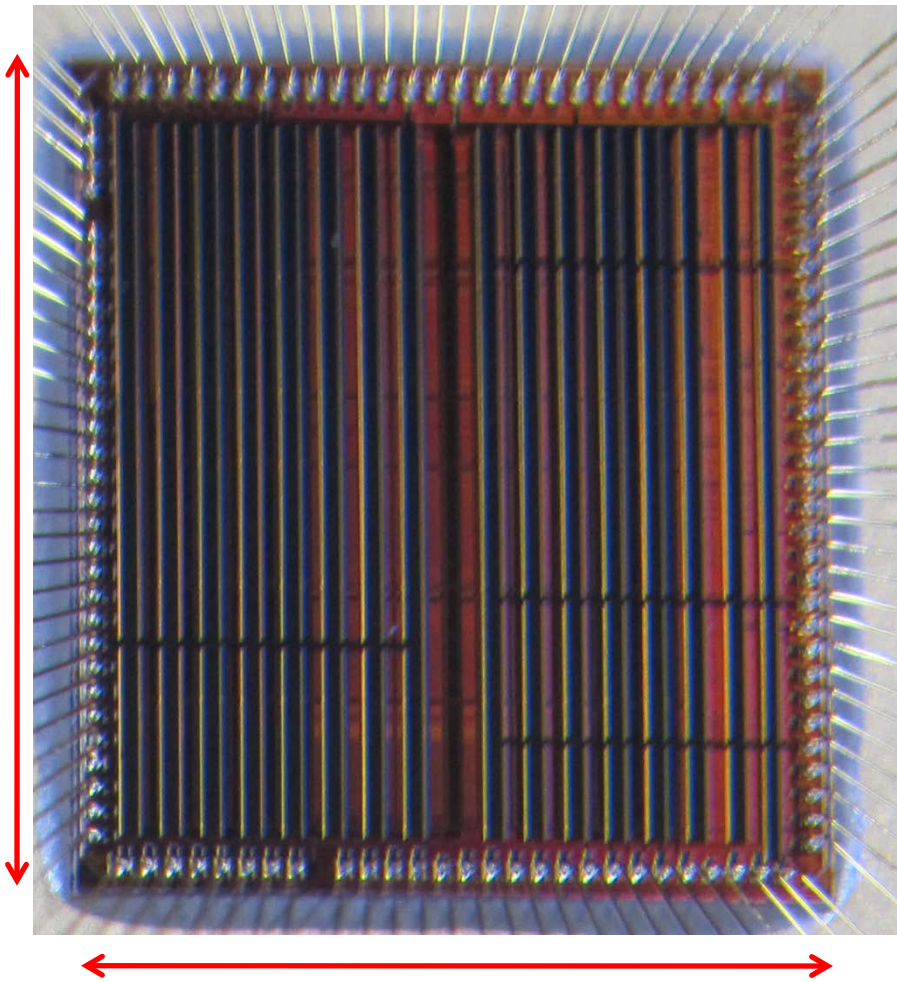
"3rd Generation" (arbitrary)

- Raw performance of 2nd Generation devices
  - Have proven themselves
  - Somewhat general purpose – therefore each adopter wants to change something
- Next generation addressing these constraints
  1. Analog bandwidth
  2. Storage depth
  3. System requirements (clock, flow control, multi-hit, etc.)
  4. Calibration overhead
- Merely a snapshot:
  1. This talk is a moving target
  2. Highly dynamic field
  3. A lot of cross-pollination

1) Analog bandwidth
(sampling, readout speed)

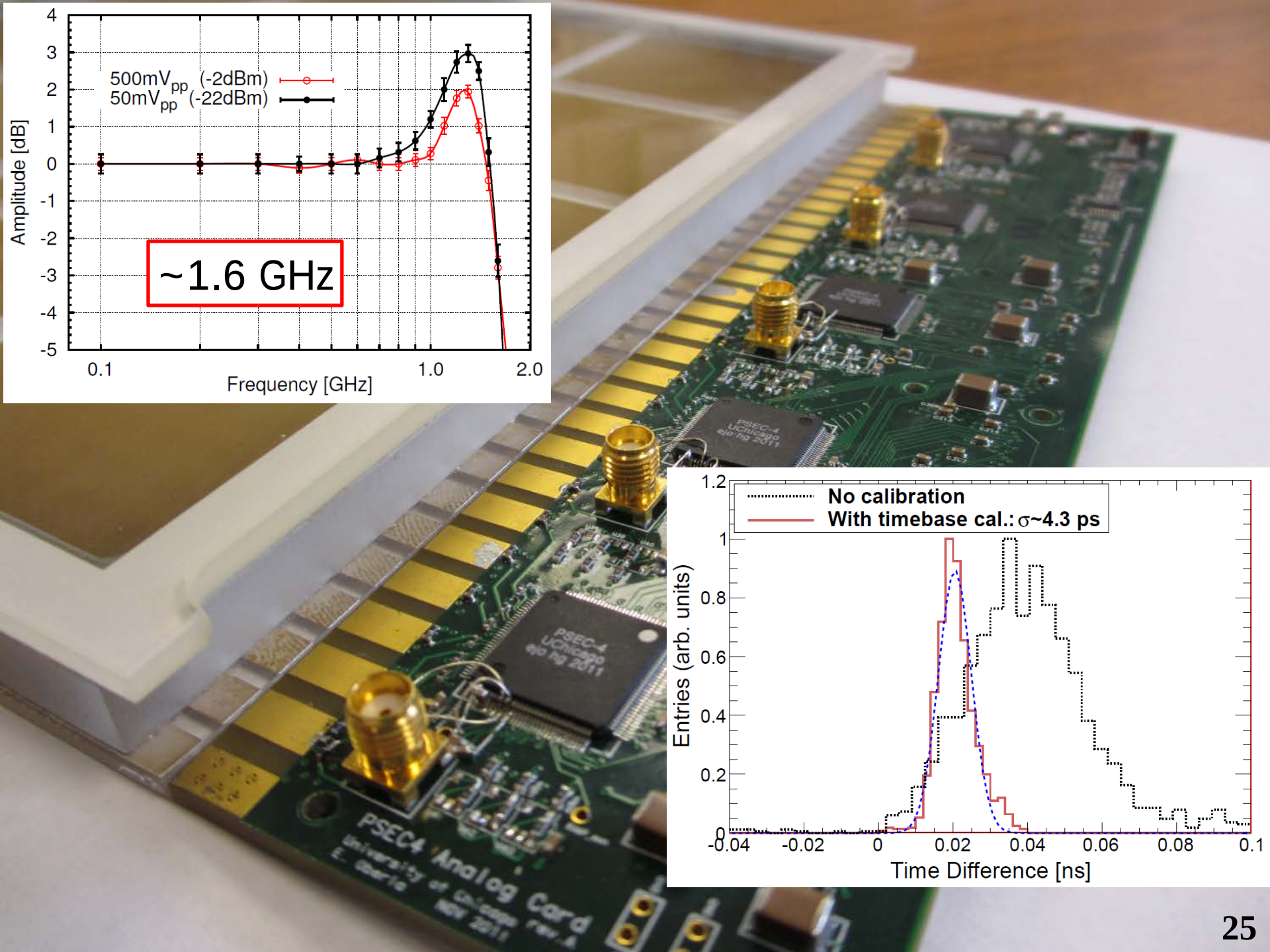
PSEC-4 ASIC

Sampling Rate	2.5 GSa/s-17GS/s
# Channels	6 (or 2)
Sampling Depth	256 (or 768) points
Sampling Window	Depth*(Sampling Rate)$^{-1}$
Input Noise	<1 mV RMS
Analog Bandwidth	1.6 GHz
ADC conversion	Up to 12 bit @ 2GHz
Latency	2 µs (min) – 16 µs (max)
Internal Trigger	yes



130nm process – sampling speed, Conversion rate

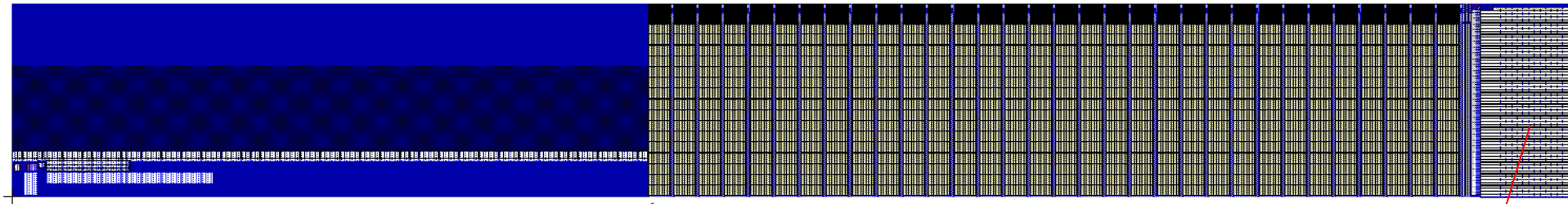
[E. Oberla, U. Chicago]

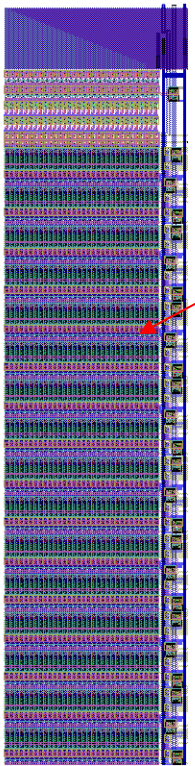

500mV$_{pp}$ (-2dBm)
50mV$_{pp}$ (-22dBm)
~1.6 GHz
Amplitude [dB]
Frequency [GHz]
4
3
2
1
0
-1
-2
-3
-4
-5
0.1
1.0
2.0
No calibration
With timebase cal.: σ~4.3 ps
Entries (arb. units)
Time Difference [ns]
1.2
1
0.8
0.6
0.4
0.2
0
-0.04
-0.02
0
0.02
0.04
0.06
0.08
0.1
PSEC4 Analog Card

2) Storage Depth

- Sampling: 128 (2x 64) separate transfer lanes

Recording in one set 64, transferring other (“ping-pong”)





- Concurrent Writing/Reading
- Only 128 timing constants
- Storage: 64 x 512 (8 ch. IRS)

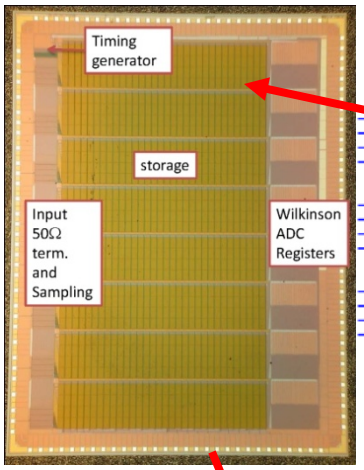
(32x512 16 ch. [TARGET – CTA])

- Wilkinson (64x1): was (32x2)
- 64 conv/channel

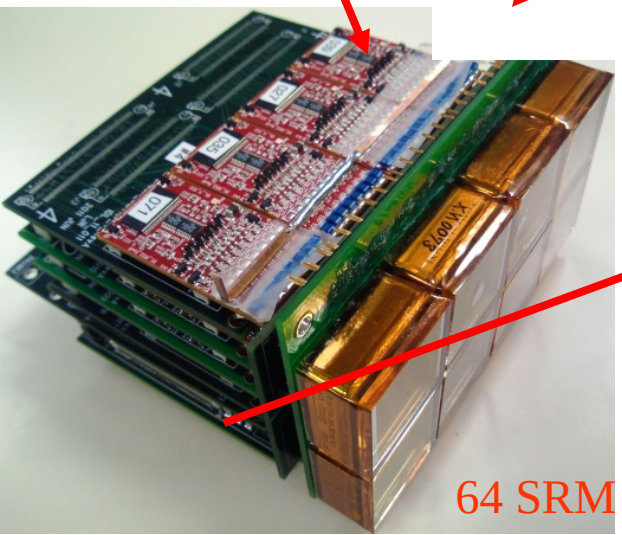
3a) Ex. Belle II TOP Readout Architecture

16 COPPER

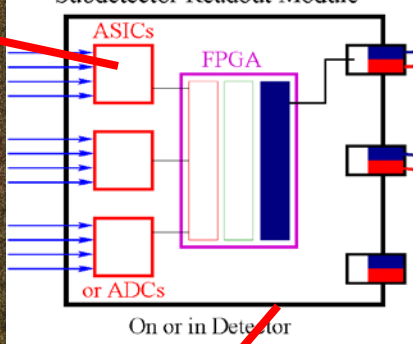
Waveform sampling ASIC



8k channels
1k 8-ch. ASICs



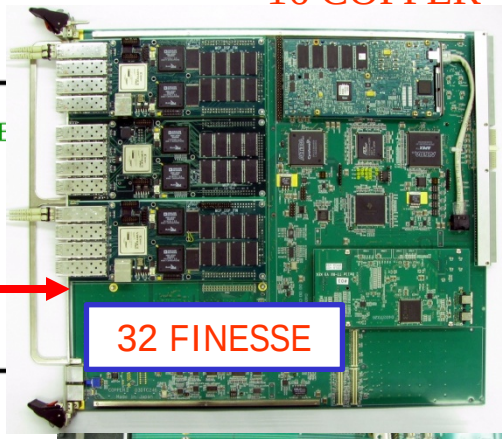
64 SRM



FPGA firmware consists of 3 parts:
1) ASIC/ADC driver (common)
2) Trigger feature extract (subdet. specific)
3) Unified DAQ transport protocol

Giga-bit Fiber Transceiver Links

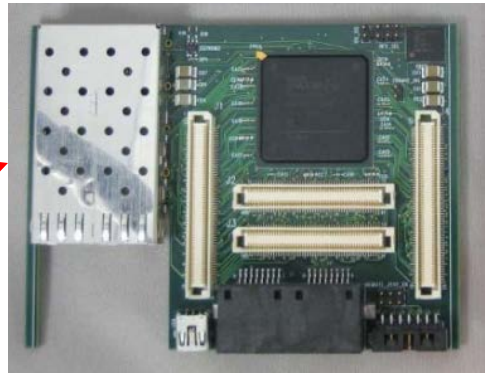
COPPER
FINESSE



Global Decision Logic

Clock/Event Timing Distribution

Clock jitter cleaners

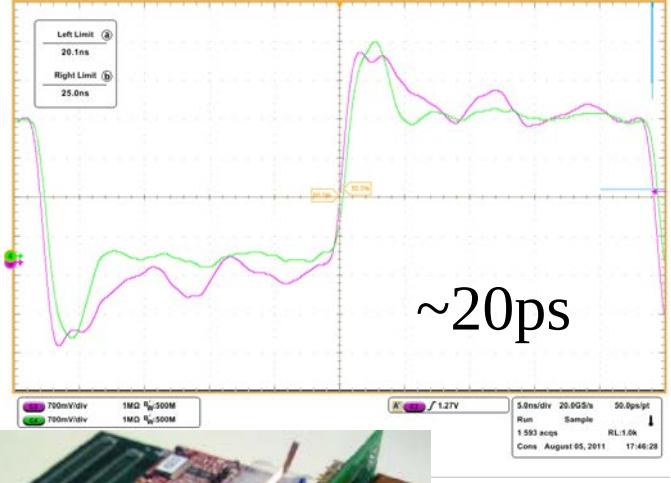


SRM Control "SCROD"

FTSW clock, trigger, programming

16 FTSW

System Synchronization

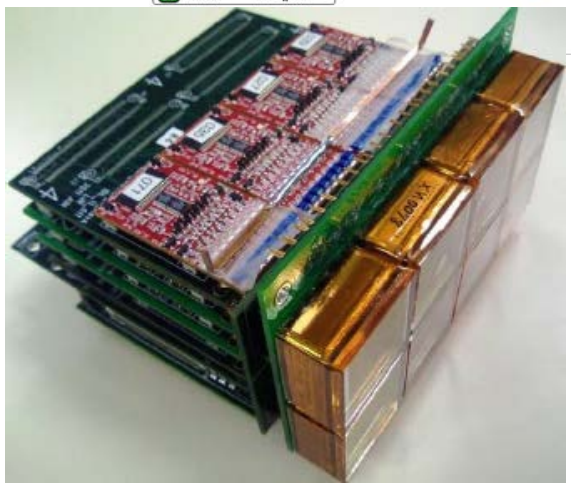


Crucial to obtain required performance

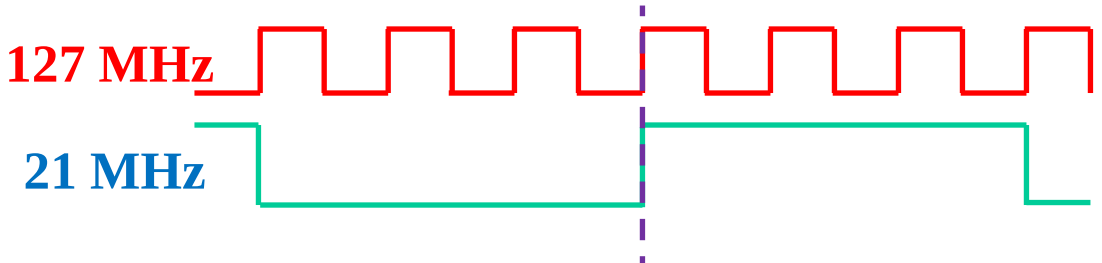
FTSW (Timing & Trigger Distribution board)

127 MHz clock

Serial data (trigger & synchronization)



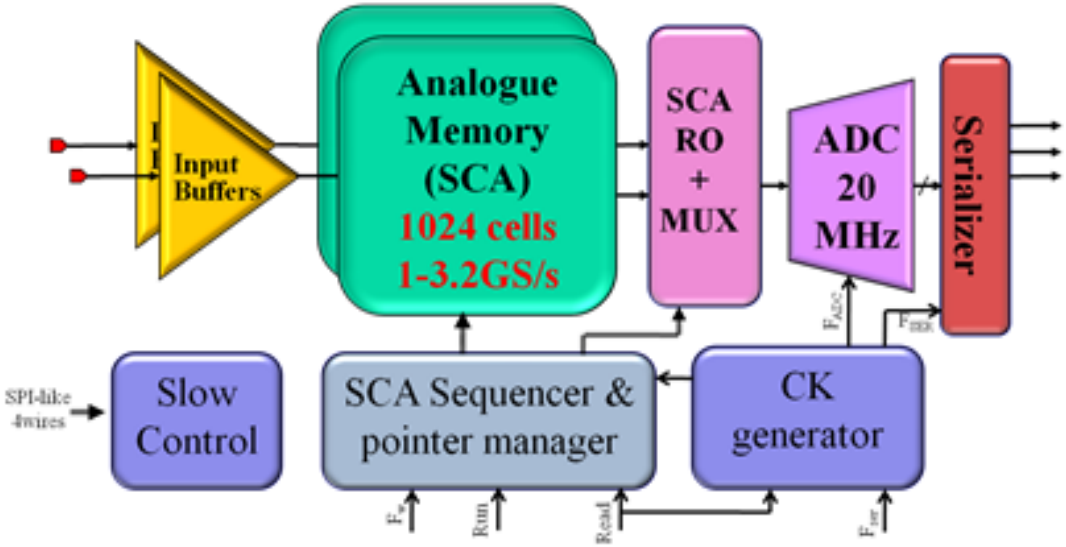
- **127 MHz clock is divided by 6 on front-end module to ~21 MHz**
  - **This corresponds to sampling rate of ~2.7 GSa/s**
  - **FPGA uses serial data stream to determine clock phase**

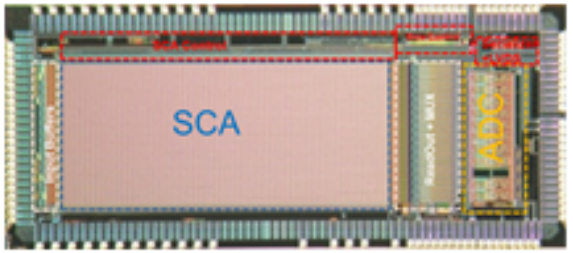


3b/4) Multiple TeV-gamma telescopes

The NECTAR chip for the Cerenkov Telescope Array

[E. Delange]

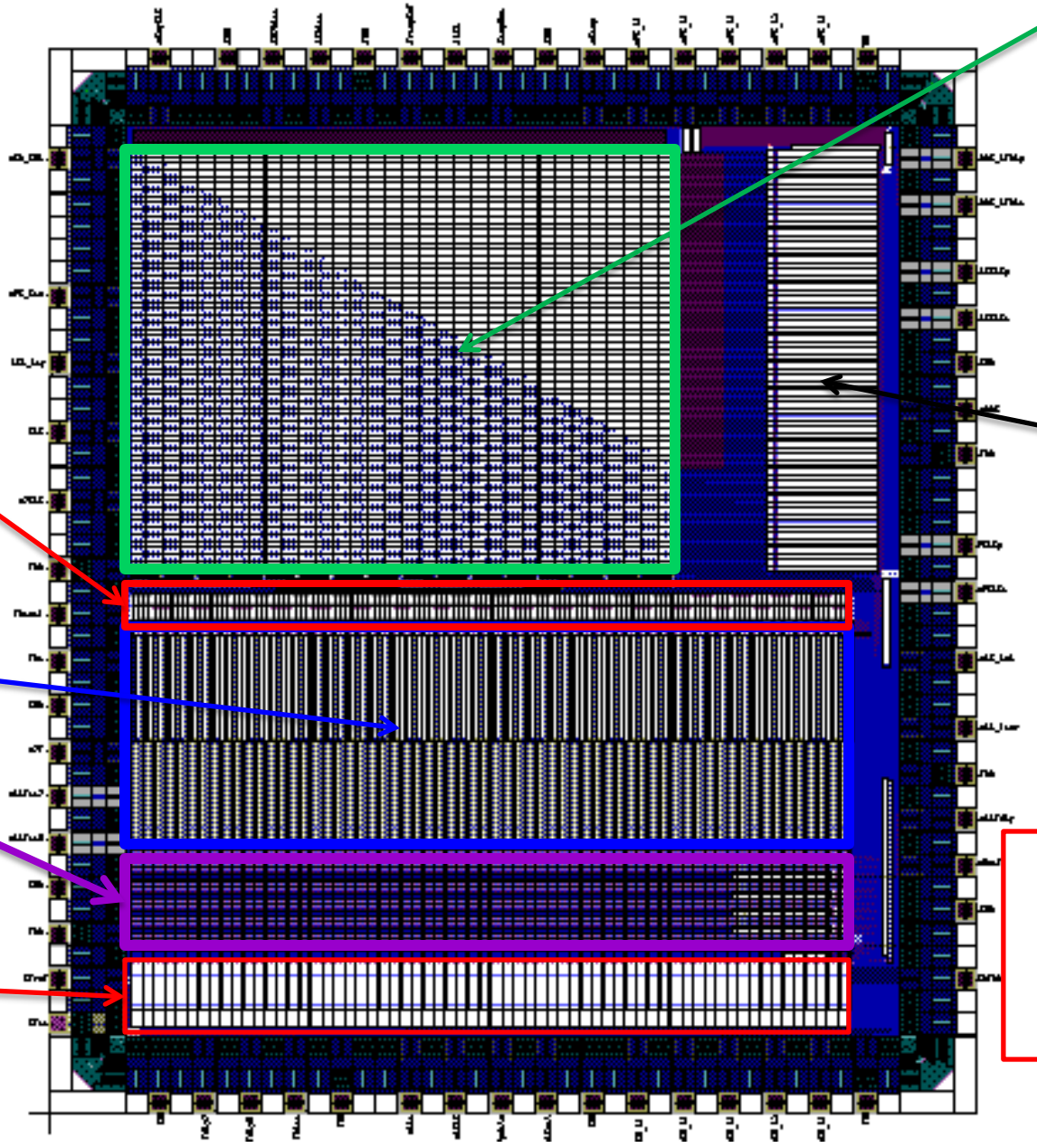




3mm x 7mm
AMS CMOS 0.35µm

- Evolution of the SAM(LONG) chip (HESS-2 telescope)
- 4 SCA channels => 2 fully differential channels
- 1024 cells/SCA channel (64 x 16 matrix)
- 0.5 to 3.2 GSPS => 1µs max latency @ 1GSPS, 0.5µs @ 2GSPS
- On chip 12 bit pipeline 20MSPS ADC
- Output data directly usable for calculation (without need for pedestal or gain spread correction)
- Low input capacitance < 4pF including package thanks to input buffers
- 4000 chips used for the upgrade of the HESS experiment (Namibia)

4) Hardware Timebase correction



Storage Array

2nd stage transfer

Wilkinson Registers

dT trim DACs

Timing Generator

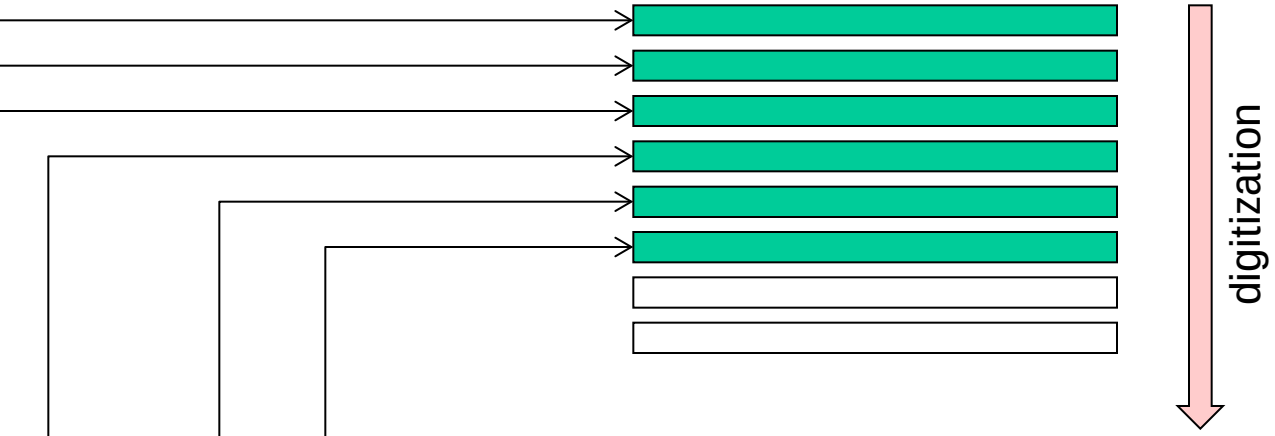
Sampling array

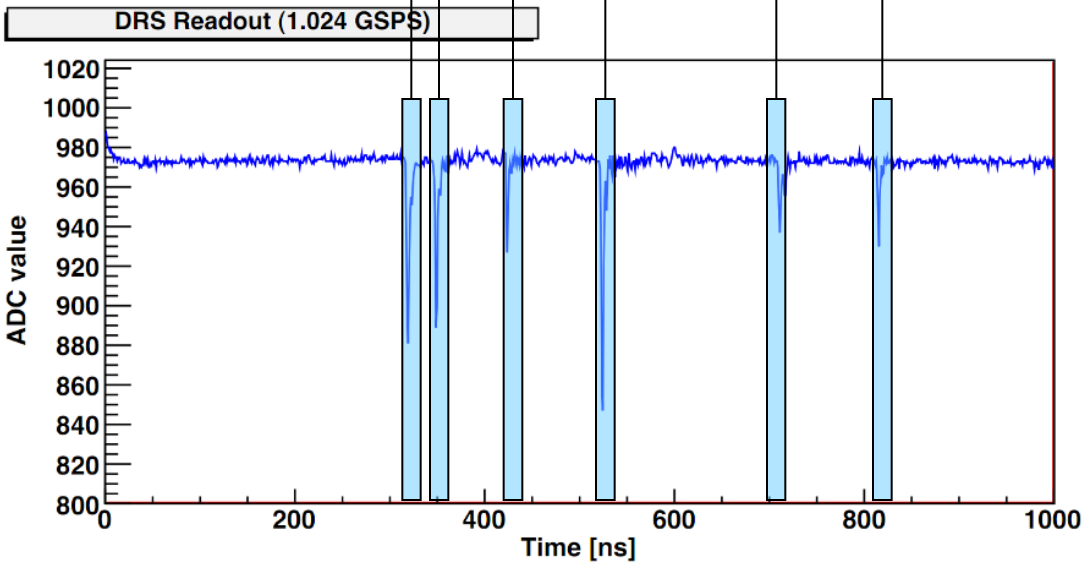
3.6 x 4.2mm

LAB4 for ANITA 4th flight

FIFO-type analog sampler

"TDC" with benefits?

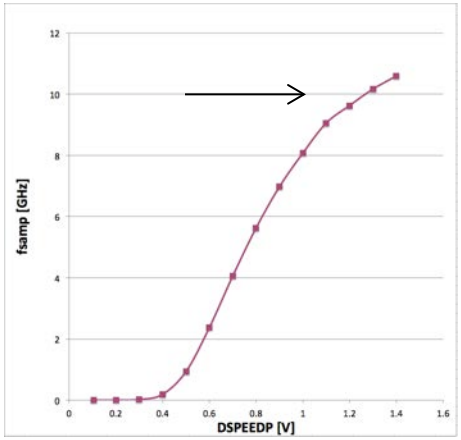


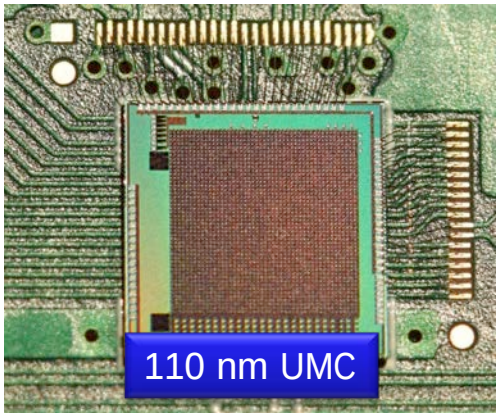


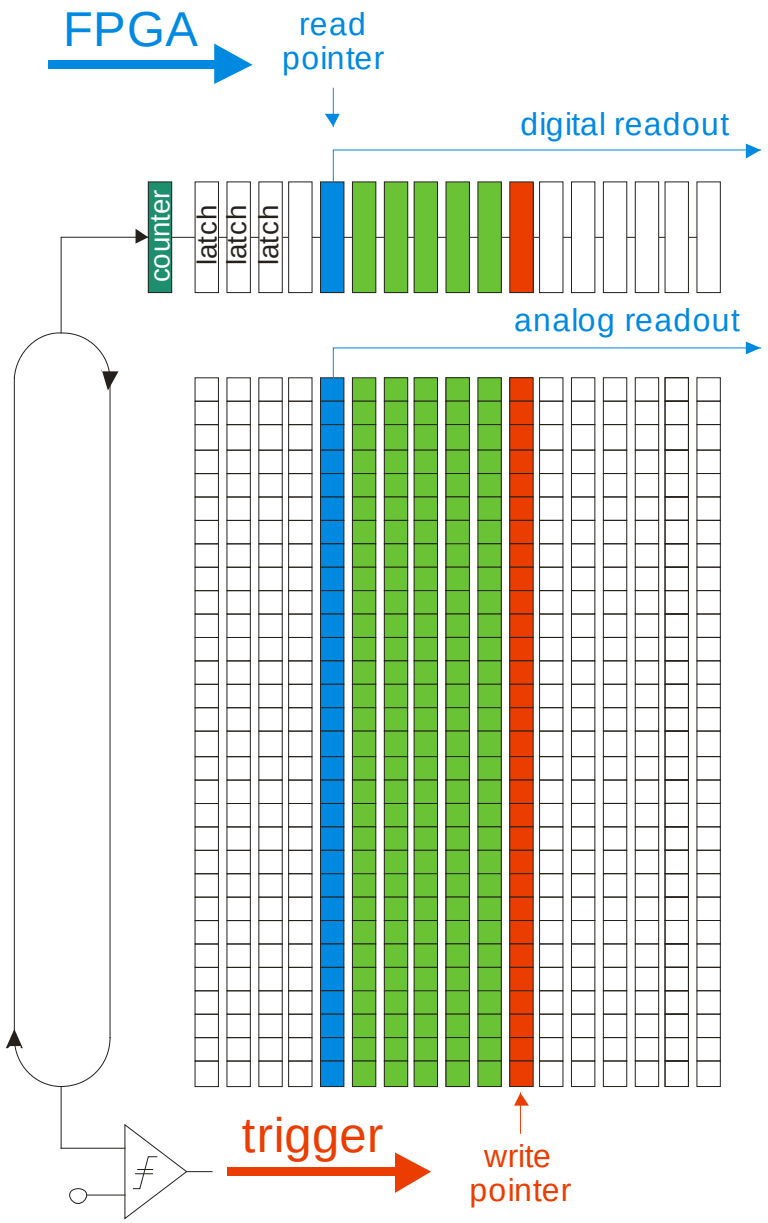
- FIFO sampler becomes immediately active after hit
- Samples are digitized asynchronously
- "De-randomization" of data
- Can work **dead-time less** up to average rate = 1/(window size * TSR)
- Example: 2 GSPS, 10 ns window size, TSR = 60 → rate up to **1.6 MHz**

DRS5, for example (100ps/sqrt(12))

- Self-trigger writing of 128 short 32-bin segments (4096 bins total, 3 GHz analog bandwidth)
- Storage of 128 events
  - Accommodate long trigger latencies
  - Quasi dead time-free up to a few MHz,
  - Possibility to skip segments
    → second level trigger
- Attractive replacement for CFD+TDC
- First tests: > 10 GSPS @ 4 mA, first full version planned for 2014



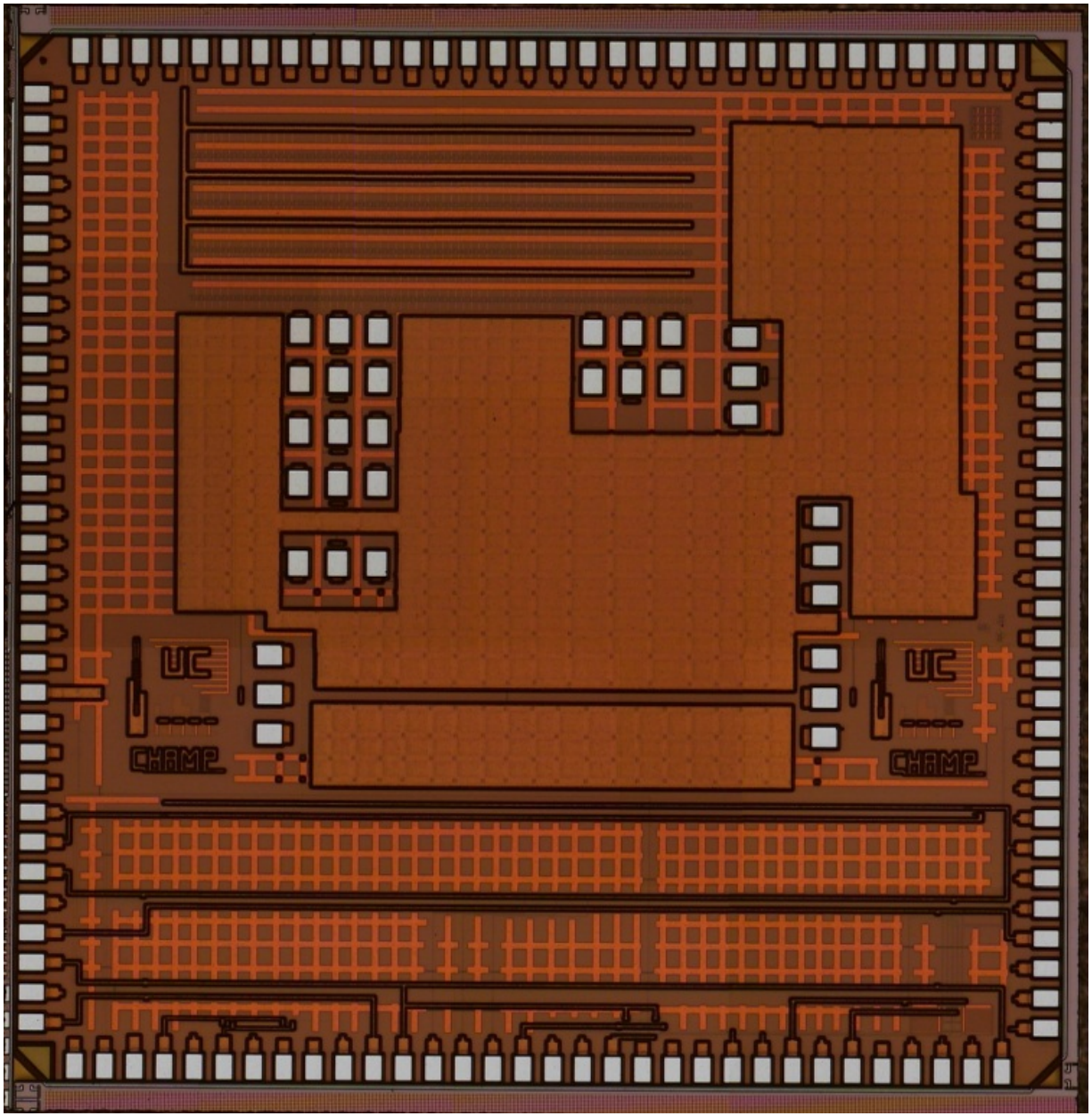




Summary

- Options for integrated, high-performance photodetector readout will continue to increase
- Next generation SCA-based readout:
  - Higher analog bandwidth
  - Faster sampling rate
  - Deeper storage depth
  - Easier calibration
  - Higher throughput
- For higher-rate applications, distinction between WFS and traditional TDC becoming blurred

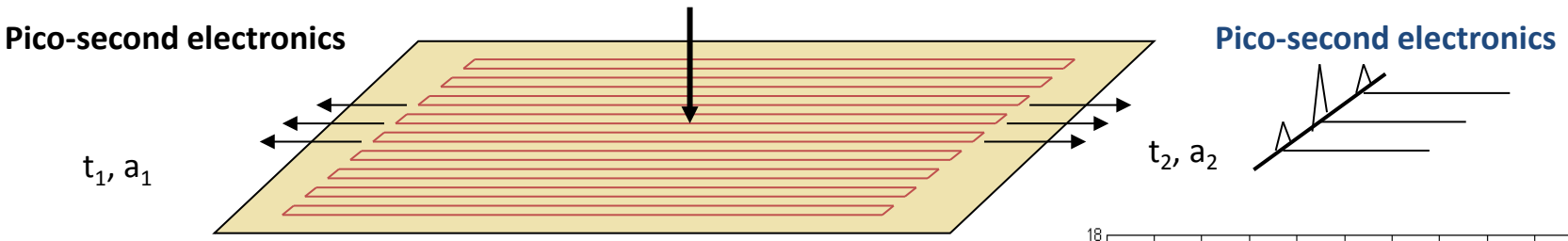
Back-up Slides



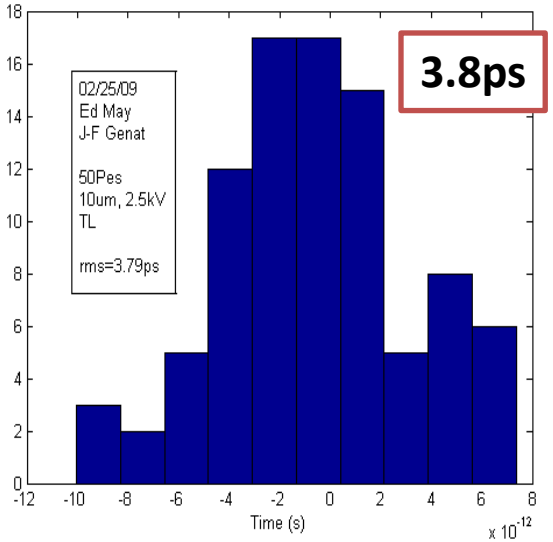
Picosecond timing and 2D position for large area detectors: delay lines and Waveform Sampling

Delay line readout and pulse sampling provide fast timing (2-10ps).
→ Delay lines should have a signal bandwidth matched to the detector

Fewer electronics channels for large area sensors



3.8 ps translates in 190 μm position resolution with 50 photo-electrons



$\frac{1}{2}(t_1 + t_2)$ = time
$v(t_1 - t_2)$ = longitudinal position
$\Sigma \alpha_i a_i / \Sigma \alpha_i$ = transverse position

The electronics contribution to spead is small:
3.8ps / sqrt(2) = 2.7ps,
For 50PEs, MCP is 30ps / sqrt(50) = 4.2ps, equal at 100 PEs

How is timing resolution affected?

$$\Delta t = \frac{\Delta u}{U} \cdot \frac{1}{\sqrt{3 f_s \cdot f_{3dB}}}$$

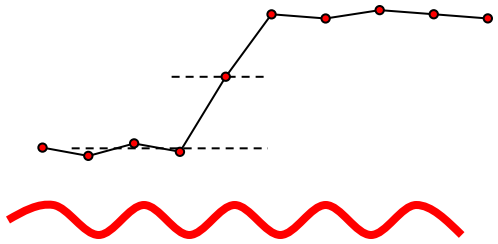
•Assumes zero aperture jitter

	U	Δu	f_s	f_{3db}	Δt
•today:	100 mV	1 mV	2 GSPS	300 MHz	~10 ps
•optimized SNR:	1 V	1 mV	2 GSPS	300 MHz	1 ps
•next generation:	100 mV	1 mV	20 GSPS	3 GHz	0.7 ps
•next generation •optimized SNR:	1V	1 mV	10 GSPS	3 GHz	0.1 ps

•How to achieve this?

•includes detector noise
in the frequency region of the rise time

•and aperture jitter

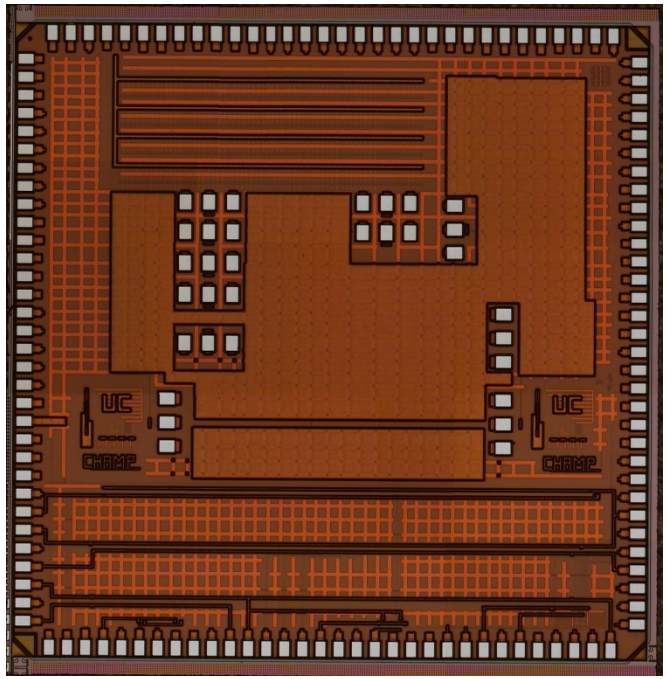


Stefan Ritt slide

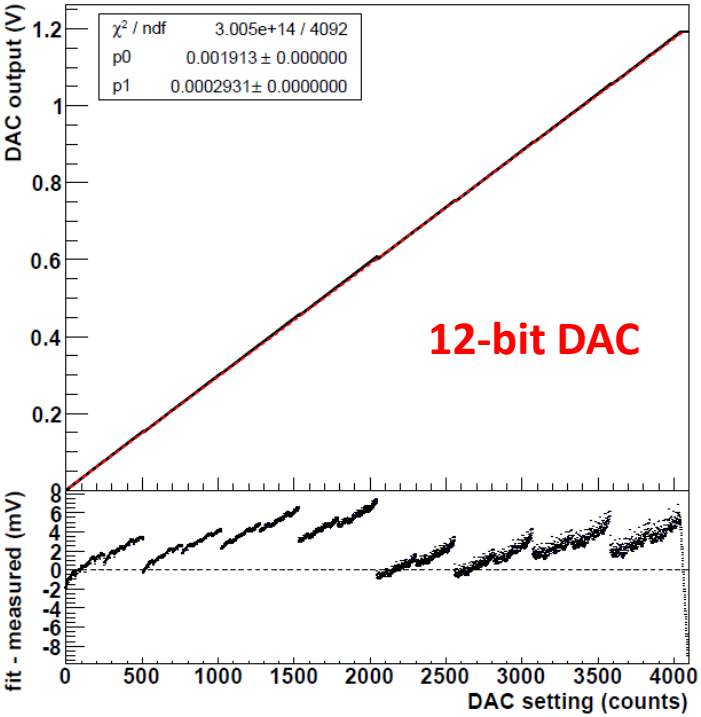
UC workshop 4/11

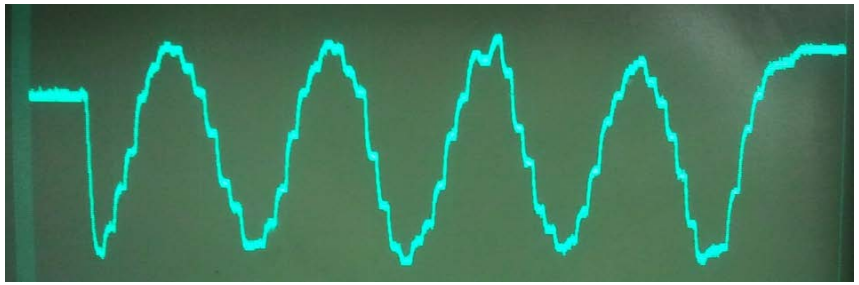
Chicago Hawaii ASIC, Multi-Purpose (CHAMP)

- Develop new circuit elements, train additional students in the IBM 130nm process

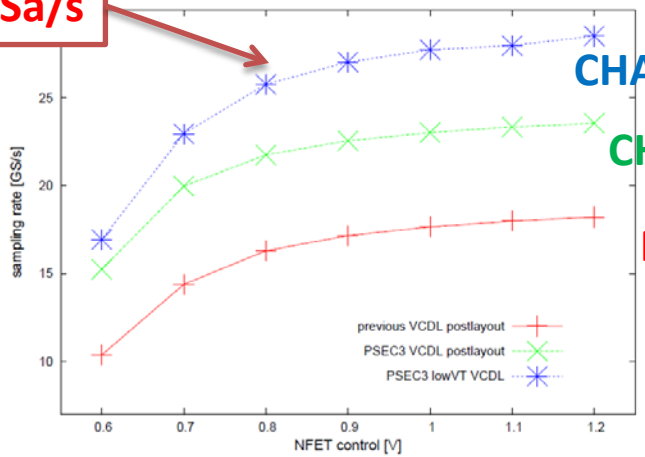


Many useful building blocks, will allow increased functionality, more compact implementation





25GSa/s

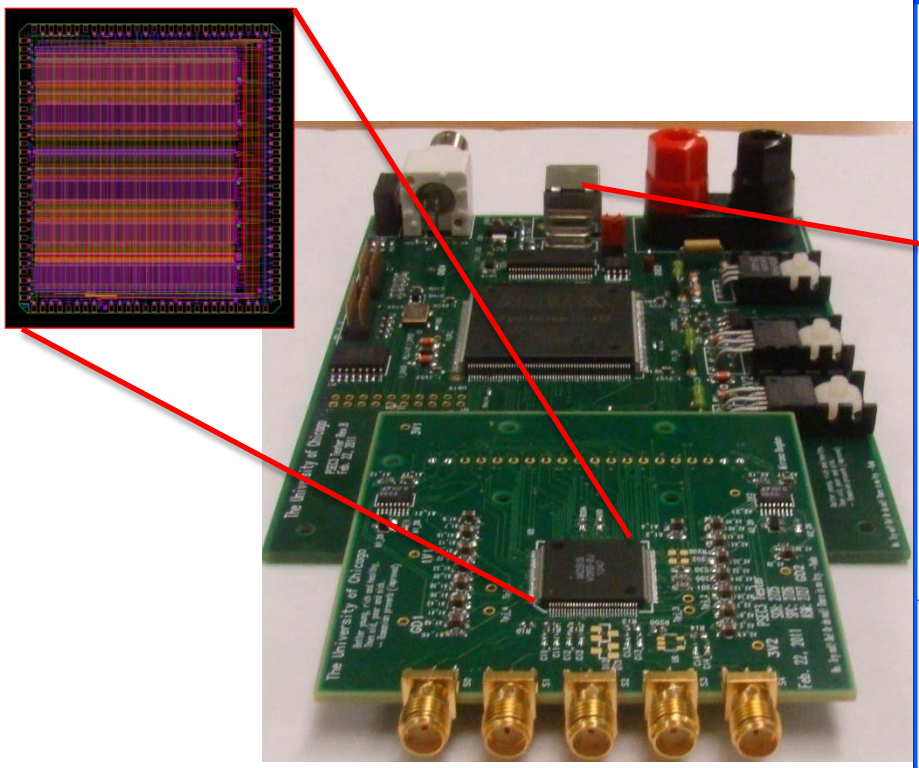


CHAMP low V_t VCDL

CHAMP VCDL

PSEC3 VCDL

Oscilloscope on a chip? ➔ Calibration



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