CPAD Instrumentation Frontier Meeting, UTA, October 5-7, 2025

Data Acquisition & Triggering

SLAC Advanced Instrumentation For Research Division (AIR)

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U.S. DEPARTMENT OF ENERGY
Office of Science

SLAC NATIONAL ACCELERATOR LABORATORY

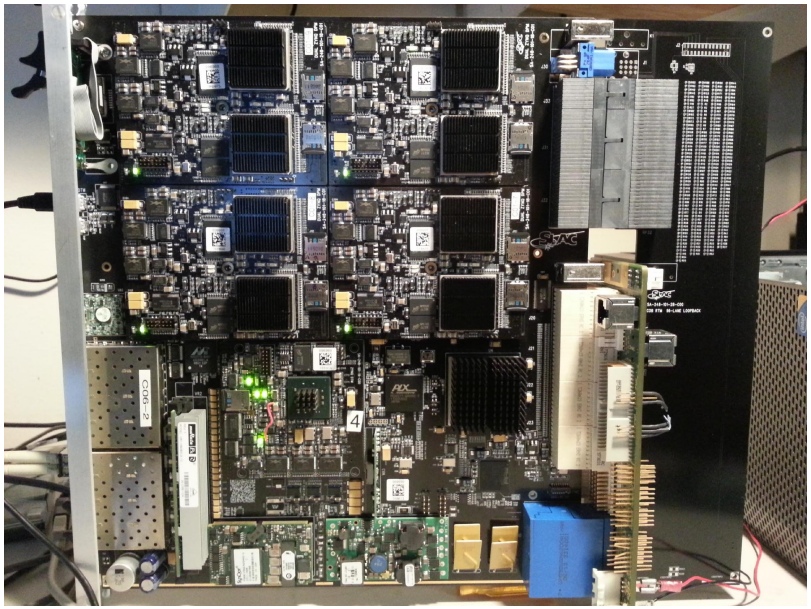
Overview

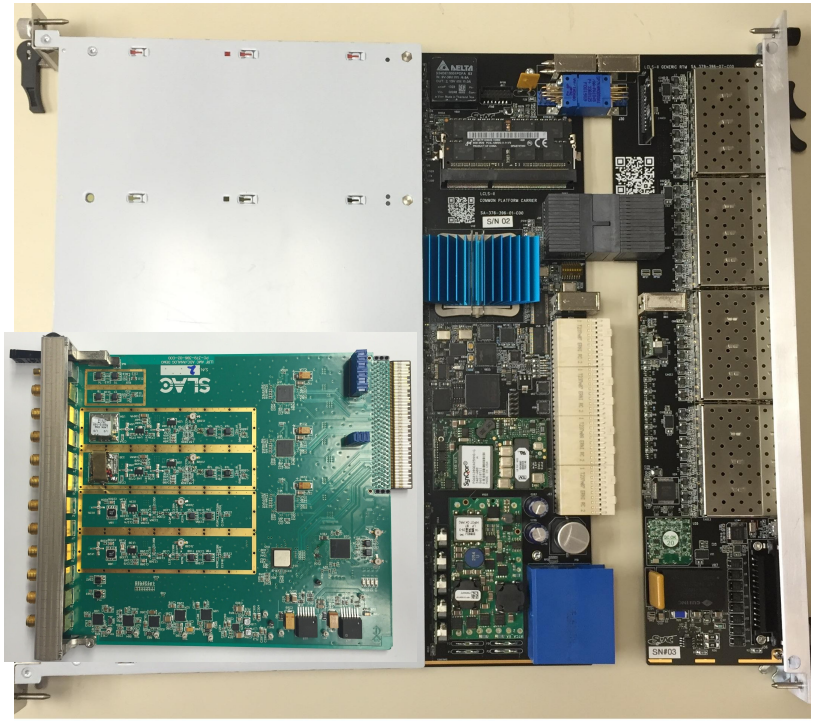
- Current Developments
- Data Acquisition Hierarchies
  - Data Path
  - Trigger
  - Event Building
- Development Challenges
  - Sandbox Approach
  - Shared Libraries & Open Source
- Roadmap
- Conclusion

Current Developments

Current Detector Development

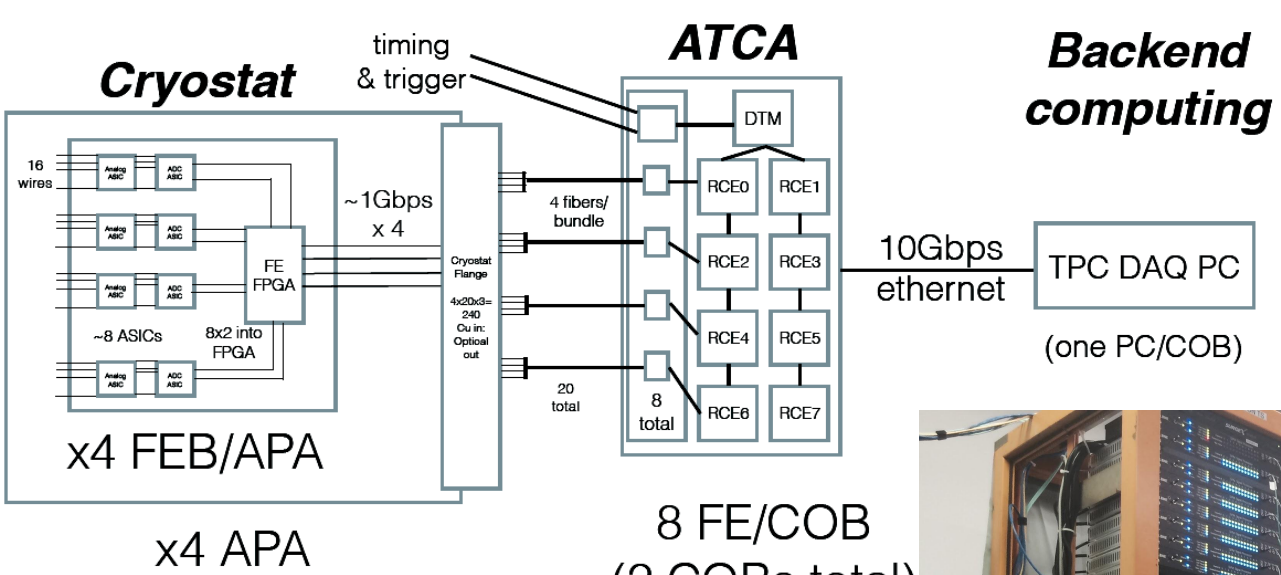
- SLAC has been focused on ATCA based data acquisition and control systems
- RCE (Reconfigurable Cluster Element) platform is a full meshed distributed architecture, based upon network based “system on chip” elements
  - “Plug in” architecture for applications
  - Firmware and software development kits
  - Based upon Xilinx Zynq platform
  - Full mesh 10G network
  - 96 high speed back end links





- ATCA based general purpose analog & RF board
- Digital back end is based on Xilinx Ultrascale FPGA
- Supports two double wide dual-height AMC cards for analog and RF processing
- LCLS-1 LLRF upgrade
- LCLS-2 BPM, MPS and timing system
- SSRL RF booster upgrade
- CMB
- TES (transition edge sensor) photon detector

RCE @ DUNE

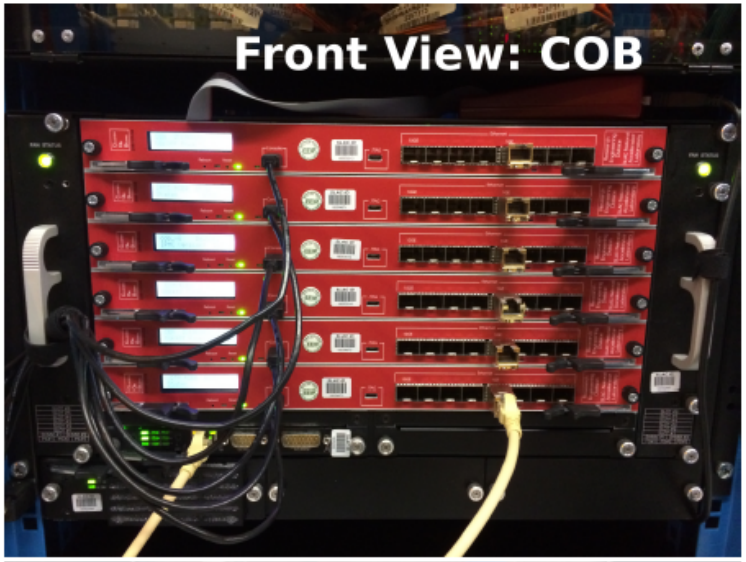


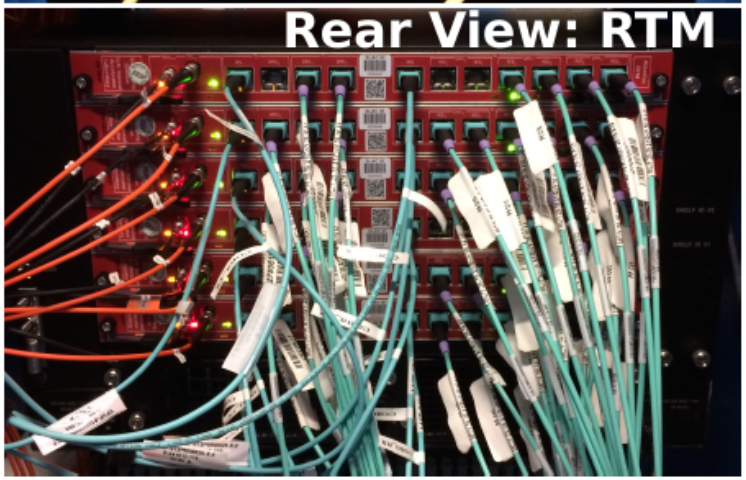
FE configuration & control done over same high-speed connections as signal, with dedicated I2C links as a backup

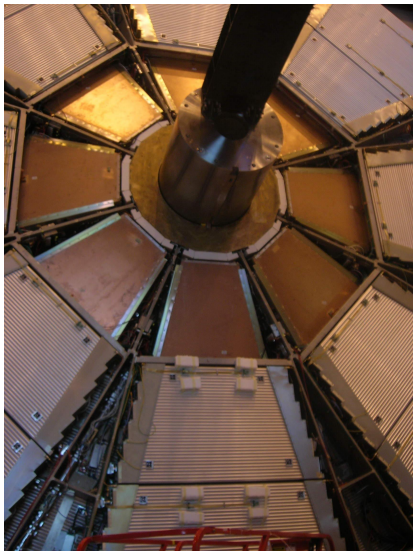
- Readout for 35Ton detector
- Integrated with NOVA timing system
- Integrated with ARTDAQ backend system
- Supports three modes of operation
  - Externally triggered
  - Scope mode for selected channels
  - Burst mode for large raw snapshots of full detector

RCE @ ATLAS CSC

- Replaced previous RODs which limited trigger rate < 70Khz
- Integrated with ATLAS timing and trigger system
- Integrated into ATLAS data acquisition
- Successful demonstration of 100Khz trigger rate @ 13% occupancy







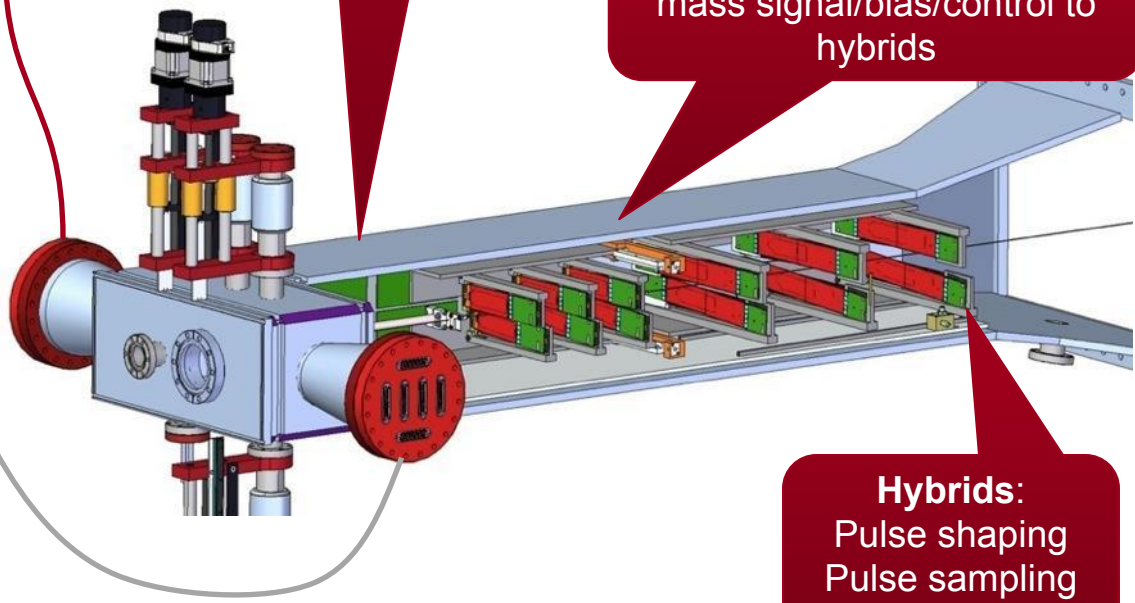
RCE @ Heavy Photon Search

DAQ Platform
SLAC RCE (ATCA blade)

Power supplies
Low voltage
Sensor bias

FE boards:
Amplification
Analog to digital
Hybrid control/power

Flex cables:
Impedance controlled, low mass signal/bias/control to hybrids



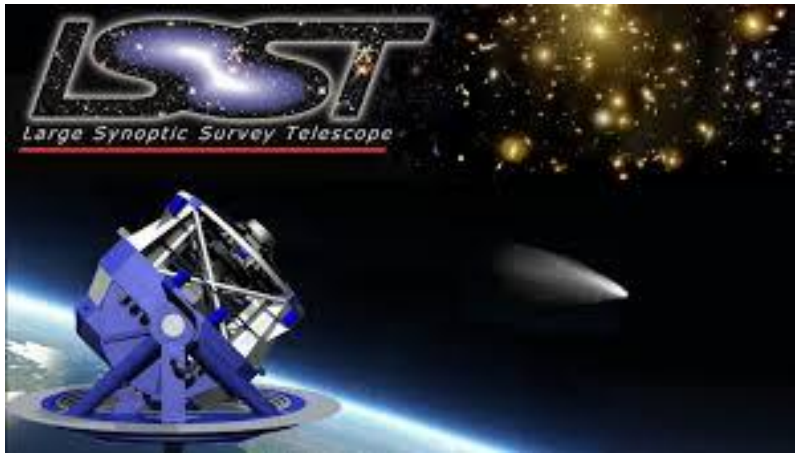
Hybrids:
Pulse shaping
Pulse sampling
Buffering

JLab DAQ

- Integrated with JLAB's timing and back end DAQ system (CODA)
- Took data at beginning of 2015
- Expect more data runs in 2015/2016

Upcoming and Potential Experiments

- LSST
  - Data acquisition and data cache
- ATLAS Inner Tracker (ITK) upgrade development
- nEXO
  - 2nd generation to EXO 200
- LCLS-1 accelerator controls upgrade
  - Beam Position Monitor (BPM) upgrade
  - Low Level RF (LLRF) upgrade
- LCLS-2 high performance accelerator controls
  - Timing distribution
  - Beam position monitoring (BPM)
  - Bunch charge and bunch length monitoring
  - Machine protection system
- LCLS-2 detectors and data acquisition

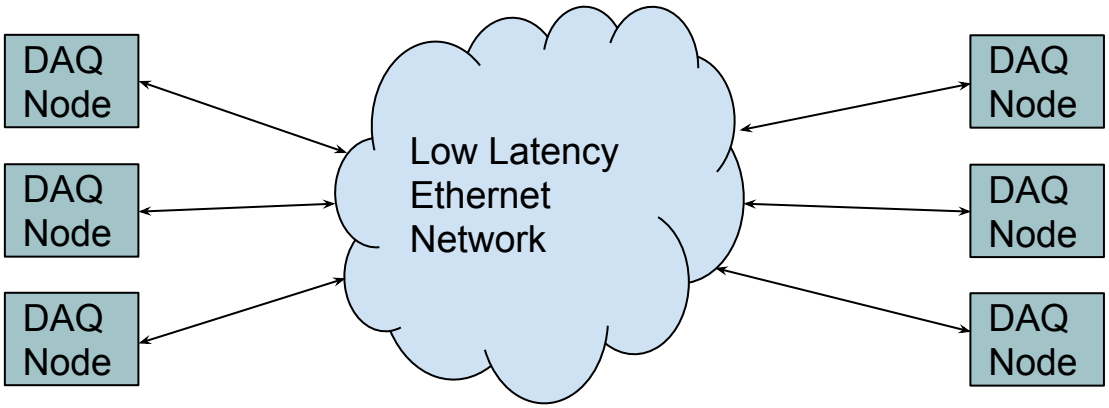


Enriched Xenon Observatory
for double beta decay

Data Acquisition Hierarchies

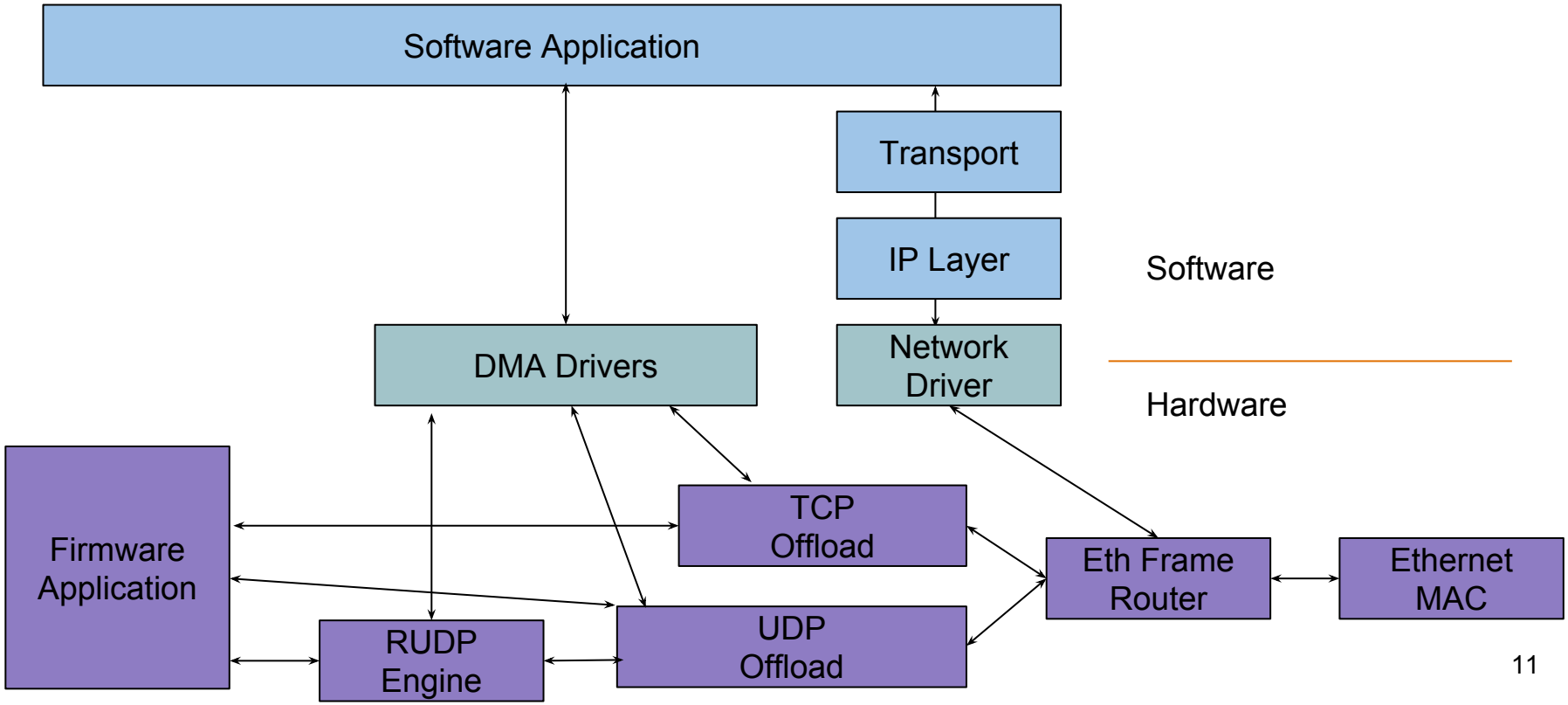
Data Acquisition Interconnects

- Data reduction, triggering and event building have similar interconnect requirements
  - Scalable low latency interconnect
  - Accessible to both low level firmware and high level software
- Need for flexible architectures for interconnect between nodes
  - Low latency switched networks allow for design flexibility
  - Best to leverage commercial networks
- VC money invested heavily in switch technology R&D in 2000 - 2005
  - Ethernet, Infiniband & PCI-Express won out
- Ethernet may be the best approach for inter-FPGA communication
  - Proven roadmap in scalability in larger systems
  - PCI-Express is optimized for short reach within the server
  - Ethernet is most efficient to implement in FPGAs
  - 10G & 40G proven on standard backplanes and optical fibers, roadmap to 100G
  - Congestion management and end to end flow control is still a challenge



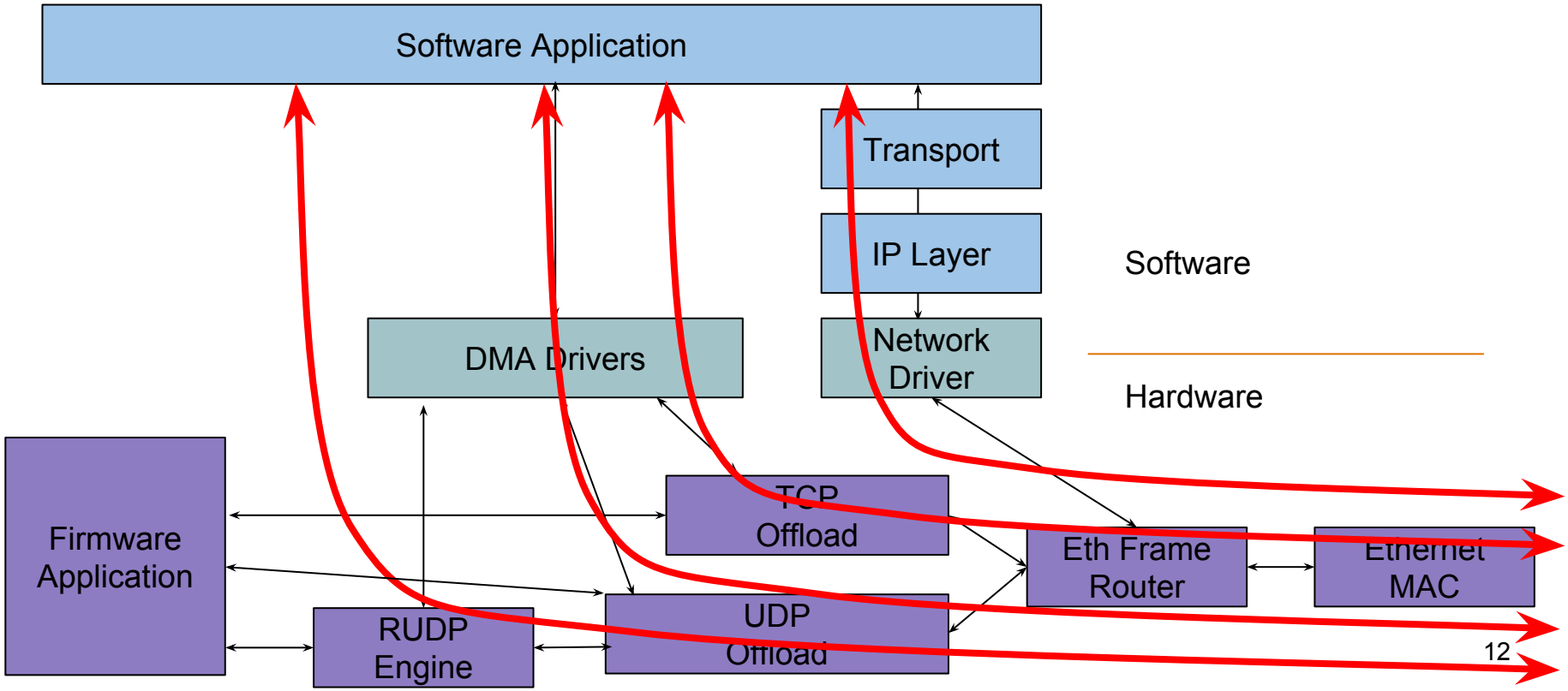
Data Acquisition Interconnects

- Firmware can assist in reducing the point to point latency for inter-node data movement
  - TCP/UDP/RUDP offload for software (RUDP is RFC908/RFC1151/Cisco)
  - Direct memory to network transactions
  - Firmware driven communication
- Multiple possibilities for data path
  - Varying levels of hardware/software involvement
  - Depends on application and latency requirement



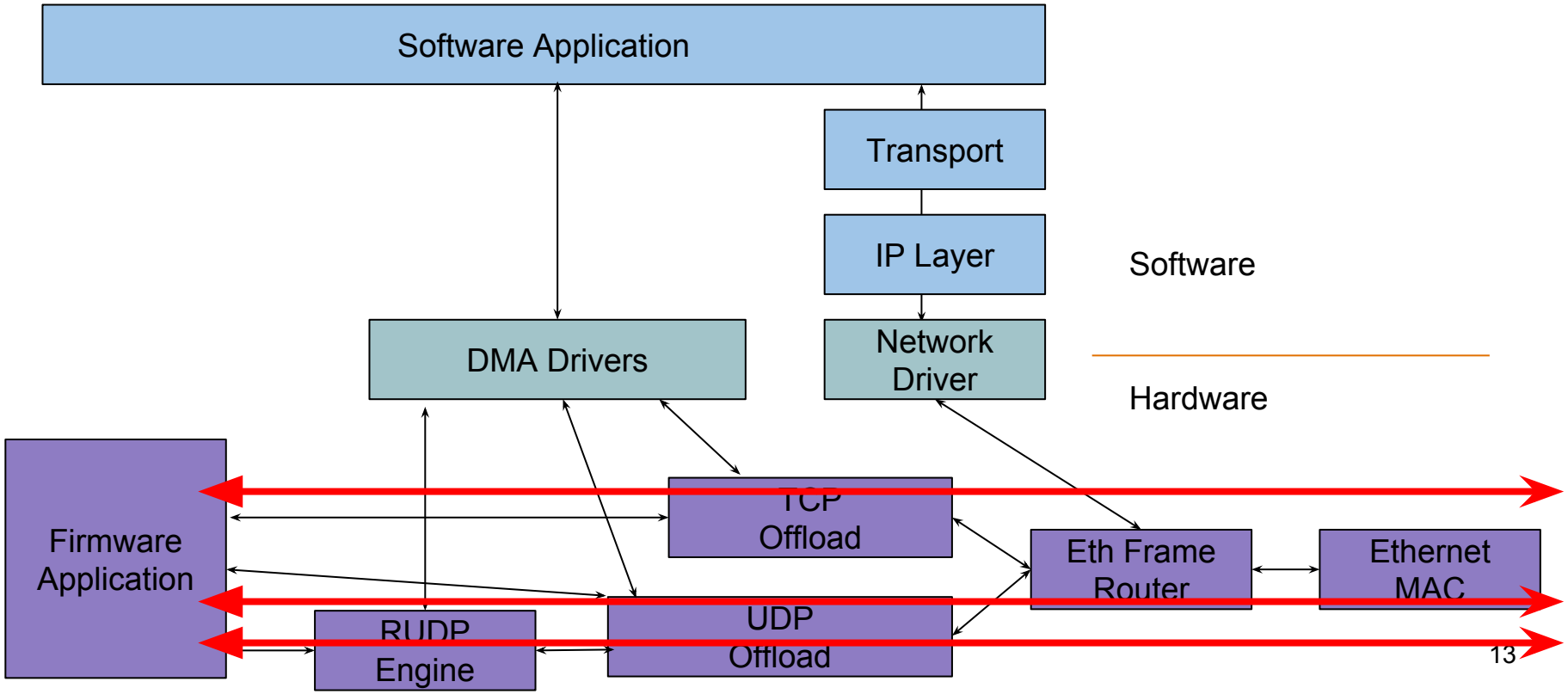
Software Communication

- Possible software data paths include:
  - Classical network access through standard network layers
  - TCP offload (FPGA resource heavy)
  - UDP offload (Minimal FPGA resources)
  - RUDP (Medium FPGA resources)



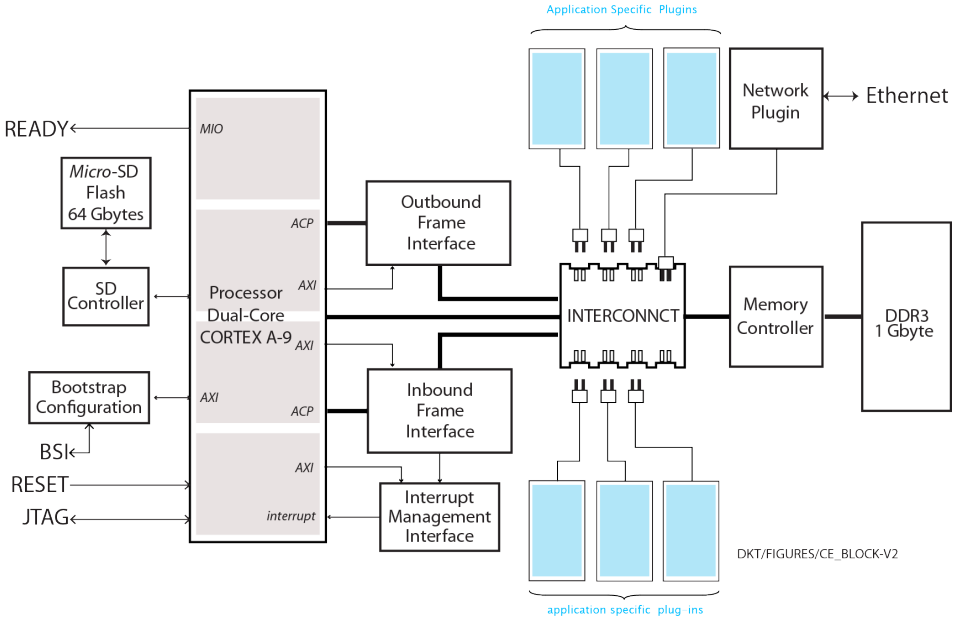
Firmware Communication

- Possible hardware paths are similar to software:
  - TCP offload (FPGA resource heavy)
  - UDP offload (Minimal FPGA resources)
  - RUDP (Medium FPGA resources)
    RUDP provides end to end flow control and buffer management
- All hardware & software modes can coexist for full flexibility



Data Processing

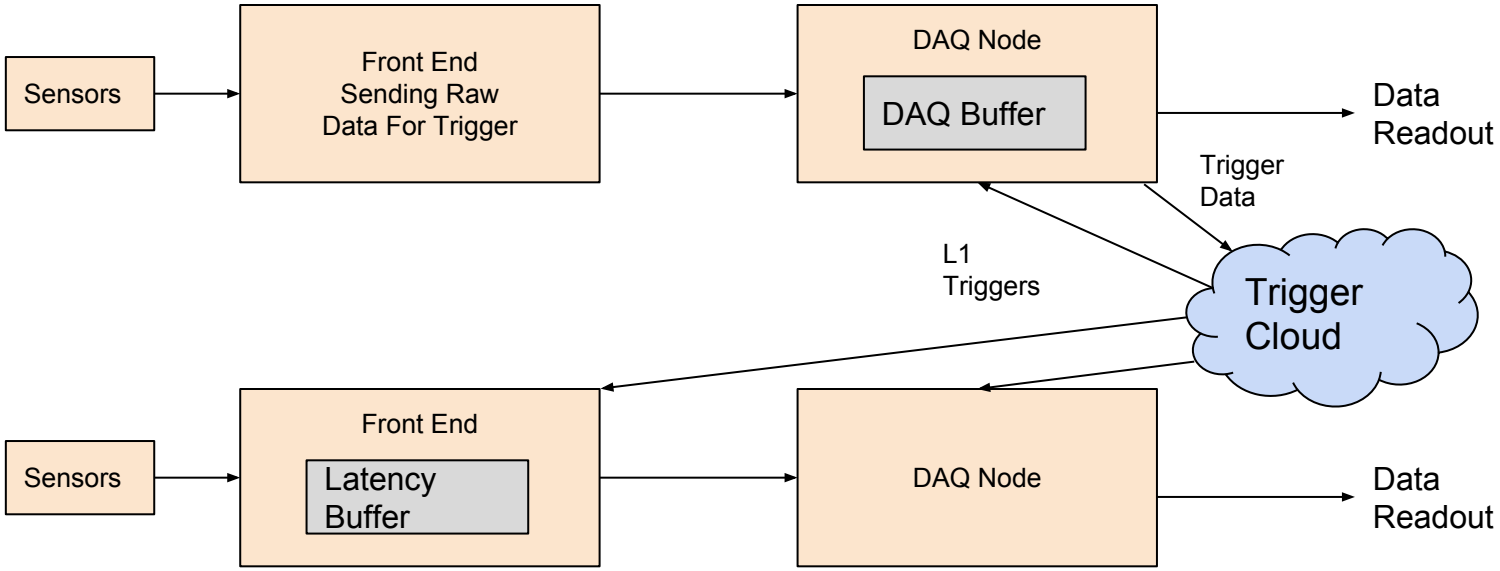
- System on chip (SOC) based designs allow tight coupling of software and firmware for online data processing
- Algorithms typically involved baseline subtraction, waveform fitting and cluster finding
- Larger detectors may have neighboring channels which interface to different data acquisition nodes
  - Inter-node communication facilitates cluster finding and proper charge calculations
- Challenge is to find the correct balance of firmware and software processing
  - Tight coupling allows the boundary to adjust to shifting requirements
  - Early development can be proven in software and then ported to firmware
- Firmware pre-processing can organize data into a format best suited for software access
  - Feature tagging to reduce software searching within memory
  - Direct to user space DMA



SLAC RCE SOC Architecture

Triggering

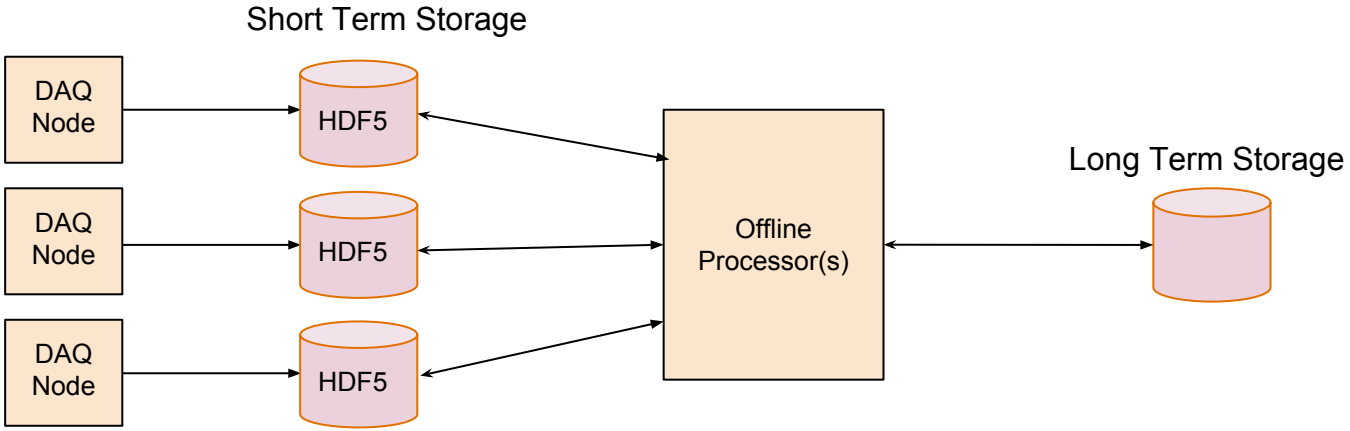
- Trigger systems can utilize Ethernet based interconnect
  - Trigger nodes must communicate with each to coordinate trigger decisions
  - Supports central node model as well as distributed trigger processing
- Varying levels of data sharing requirements
  - Some systems allow meta-data to be passed for trigger decisions, reducing bandwidth
  - Complex systems must pass raw data over interconnect
- Latency requirements depend on buffer and bandwidth capabilities of the front end
  - Small buffers in front end reduce the available time, squeezing the latency requirement
  - Front end with high bandwidth interconnects can utilize deeper buffers in the daq nodes
  - Front ends which contribute to trigger must send at least some raw data



Event Building

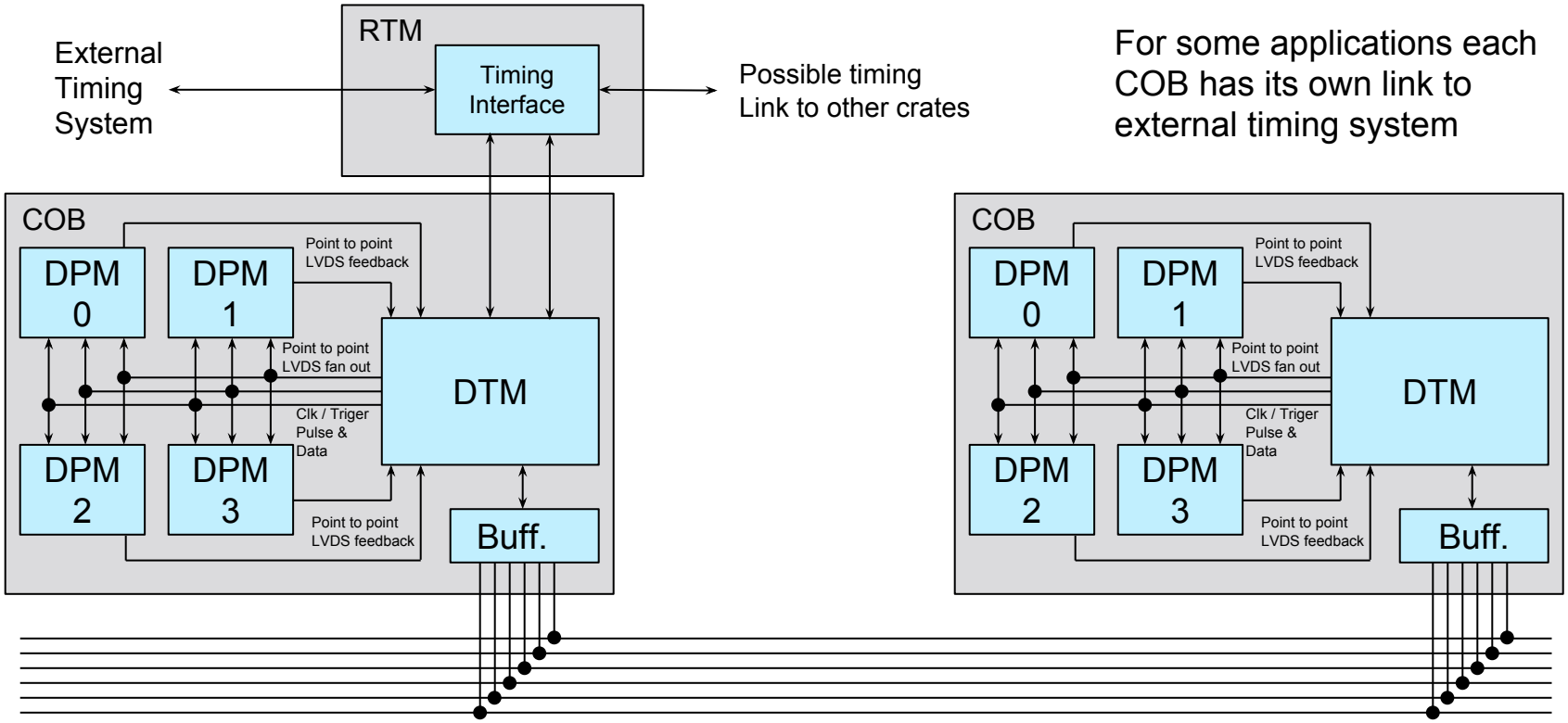
- Similar network requirements for event building
  - Central event building
  - Distributed event building with dedicated nodes
  - Distributed event building utilizing existing DAQ nodes
- Event building is utilized for systems that required higher level (L3) triggers
  - Reduces data storage requirements with additional filtering

- For some systems higher level trigger is not utilized
  - This systems may rely on post processing or even “offline” data filtering
  - Often utilized in photon science where post processing is very experiment specific
  - HDF5 allows for timestamped data storage for later event building



RCE Platform Timing Distribution

- Crate based systems allow for a single point of entry for timing
- Clock, trigger and timestamp information is decoded at the point of entry
  - Single place where timing system specific logic needs to reside
  - Eases interfacing to foreign timing and trigger distribution systems
- Timing information is distributed locally within the card and across the backplane
  - ATCA provides timing busses which meet telecom standards
  - Used to forward clock, trigger pulses and timestamp data



For some applications each COB has its own link to external timing system

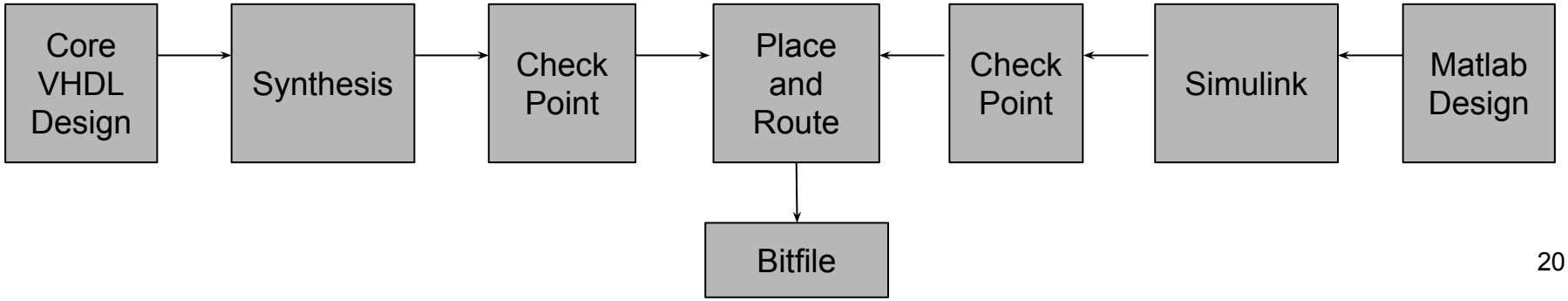
Development Challenges

Development Challenges

- Organizations face challenges developing for high performance systems
  - Not everyone is a highly skilled firmware engineer
  - Most are not familiar with real time programming
- As we transition to firmware based systems, skill sets have to evolve as well
  - Need to bridge the gap and smooth the transition
  - Advanced RF developments are transitioning to FPGAs
  - A high performing DAQ platform is not attractive if “experts” are required for development and maintenance
  - Can create a manpower bottleneck
  - Learning curve encourages dirty alternative approaches which are hard to maintain
- FPGA vendors address this problem with higher level synthesis tools and Matlab integration
  - Examples and development flow assume the entire FPGA
  - Does not bridge the gap to larger complex designs
  - Results are often difficult to debug
  - Revision tracking requirements are not met
  - Difficult path to native VHDL/verilog conversion
  - Not easy to integrate a complex base platform

Creating The Sandbox

- SLAC employs a partnership between the low level firmware designer and the application designer
- Leverages tools provided by vendors with an organized design flow
  - Well defined example designs
  - Make based build system which utilizes vendor API (Xilinx Vivado TCL API)
- Creating a well defined “sandbox” in which the application developer can work
  - Well defined interfaces for application developers
  - Data in and out delivered via AXI-Stream interfaces
- Core design is created and synthesized with the application as a black box
  - Design checkpoint containing the synthesized core and associated constraints is created
- Application is developed using one of the higher level development tools from vendors
  - Matlab Simulink
  - Vivado HLS
  - Registers for configuration and status can be created in HLS tool
  - Output of higher level development tool is a design checkpoint of synthesized design
- Build scripts combine the two checkpoint files into Xilinx project and perform place and route
- Partial reconfiguration provides additional isolation but the licensing is still costly



Shrinking The Sandbox

- Some limitations and irritations have been identified with this approach
  - Sometimes simulink can generate problematic RF blocks
  - RF block parameters are not always matched to expectations
  - Concerns about revision tracking and readability have been raised
- SLAC has been addressing similar problems in native VHDL/Verilog designs
  - Identify commonly used modules and add them to standard library
  - Reduce dependency on coregen and ip generator by creating parameterized native VHDL versions of common library cores (FIFOs, RAMs, DSPs, etc)
  - Create hierarchical building blocks which can be used in more complex algorithms
- Similar approach is being employed for HLS and Simulink designs
  - Identify common DSP and RF blocks which are used in many designs
  - Create building blocks written in VHDL with configuration parameters
  - Slowly replace vendor library black boxes in Simulink and HLS designs with locally maintained blocks
- Library approach reduces risk by leveraging well tested common blocks used in many designs
  - Readability and revision tracking is better than auto generated VHDL/Verilog
  - Provides path to convert initial high level design to native VHDL
  - Ensures long term maintainability of designs
- Create well documented build scripts and library structures
  - Supports multiple vendor tools with a common project structure
  - Text based configuration and module based structure definition
  - Allows build from checkout instead of deploying Xilinx or Altera projects
  - Eases integration of re-usable libraries

Libraries & Open Source

SLAC

- SLAC's AIR division has created an expansive library for firmware development
  - VHDL helper utilities to bridge the gap to VHDL-2008 availability in tools
  - Parameterized modules for commonly used blocks (FIFOs, RAMs, AXI-Lite, AXI-Stream)
  - DMA engines for Zynq and PCI-Express designs
  - Ethernet blocks and custom high speed serial protocols (PGP)
- Common software libraries and drivers also available
  - Support scripts and libraries for RCE based systems
  - General purpose hardware abstraction software

- We are currently exploring legal options for releasing libraries and build scripts as open source
  - DOE has defined guidelines
  - Libraries are already released as part of core design within collaborations
  - Encourage adoption of our libraries at other laboratories
  - Encourage other laboratories and collaborators to add to and enhance libraries and build systems
- Can the various DOE laboratories collaborate in firmware and software development?
  - Look towards open source projects as an example
  - Some structure required but can be sectional with localized expertise
  - Encourage interface similarities to enable portable design reuse?
  - Ideal result would be design portability across open hardware platforms

- What can we learn from the current open source trends?
  - Rise of open hardware platforms

Roadmap

- Continue development of RCE platform
  - Improved SDK and support tools
  - Research available real time options for Linux
  - 40G upgrade for COB
  - Ultrascale Zynq upgrade
- Continued R&D into RCE based applications
  - Low latency trigger architectures and algorithms
  - Online data reduction with software/firmware
  - High density flash storage coupled to RCE processors (LSST)
- R&D into Gigachip (GCI) memory systems
  - Multiple processors/FPGAs accessing central shared memory
- Demonstrate low noise analog designs in ATCA
  - LCLS-2 controls platform
  - High density photon readout with tight integration to RCE platform
- Continue R&D into FPGA based RF platforms
  - ATCA based carrier board at the core
  - Build IP library for RF & DSP cores
  - Improved design flow and revision tracking
  - LCLS-1 low level RF upgrade
  - TES based photon detectors with RF
- Improved hardware abstraction
  - “Device Tree” like description file to define the hardware registers and overall structure

Conclusion

- SLAC has a successful SOC based data acquisition platform (RCE)
- We have an eye towards future upgrades of our existing platform
- SLAC is embarking on integrated analog and RF designs in ATCA
- We are continuing our successful development of data acquisition systems, detectors and high performance data processing
- We are addressing the needs of a diverse development community with varying skill sets
- We are embarking on bringing our data acquisition expertise into controls systems
- We hope to join in a larger collaboration of DOE laboratories