Implementing a Time-to-Digital Converter (TDC) in a Field Programmable Gate Array (FPGA)

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Abstract

A Time-to Digital converter (TDC) implemented in a field-programmable gate array (FPGA) as high-resolution time measurement device is presented. This TDC FPGA is innovative in that it solved many problems prevalent in the previously developed firmware. Its new flexible firmware enables it to be utilized in many practical applications. The TDC has several unique features: (1) Its time recording structure, based off a newly designed method, allows it to yield multiple usable measurements that sub-divide each timing bins, thus improving measurement precision. (2) The TDC supports advanced timing reference distribution schemes that are established with multiple measurements, subsequently eliminating the need of high-quality timing distribution media. (3) Some of the necessary digital processing functions of the TDC FPGA, such as the semi-continuous auto-calibration, are integrated into the firmware to give user a "turn-key" solution. This significantly shortens the learning curve while maintaining is flexibility to many applications. The TDC FPGA has been used for many Time-of- Flight (TOF) experiments, and is currently being used in Main Injector Particle Production Experiment (MIPP) at Fermilab.

Introduction

Fermi National Accelerator Laboratory (Fermilab) is a world renowned Department of Energy Laboratory located in Batavia, IL. Fermilab's world-class scientific research facility attracts researchers from around the world who conduct fundamental, yet innovative, research that seeks to unravel phenomena in physics and high energy related fields. Fermilab's Main Injector has been a major instrument in many of Fermilab's experiments. The Main Injector has been a decade in the making. The initial design work started in 1987, when a small group of physicists undertook a study of how Fermilab could enhance the performance of the Tevatron beyond its original performance goals, by integrating a new accelerator or accelerators within the existing complex. The Main injector's primary function is to accelerate particles. Furthermore, there was a dramatic increase in the number of proton-antiproton collisions that can be created and observed in the Tevatron, by increasing the beam current in the Main Injector, its reliability and the cycling rate over the Main Ring which it replaces, This extends the physics "reach" to higher mass and rarer particles that will, if discovered, expand our understanding of the nature of matter and the forces that hold it together.

Image 1: Main Injector

The Main Injector, as shown in figure 1 is currently being used to complete the Main Injector Particle Production Experiment (MIPP). The MIPP Experiment (Fermilab E907) is a fixed target experiment in the Meson Center Enclosure 7 (MC7) beam line of the Meson Area at Fermilab. It will use 120 GeV/*c* Main Injector beam and will measure particle production from primary beam interactions in the NuMI/MINOS target, and from secondary beams interacting with thin targets. One of the main detectors is a 2 m^3 time projection chamber (TPC), operated with P10 gas, a –10 kV drift potential, and +1300 V anode potential for gas gain of the ionization signal. The Time Projection Chamber(TPC) uses custom readout electronics and VME interface to commercial data acquisition processors.

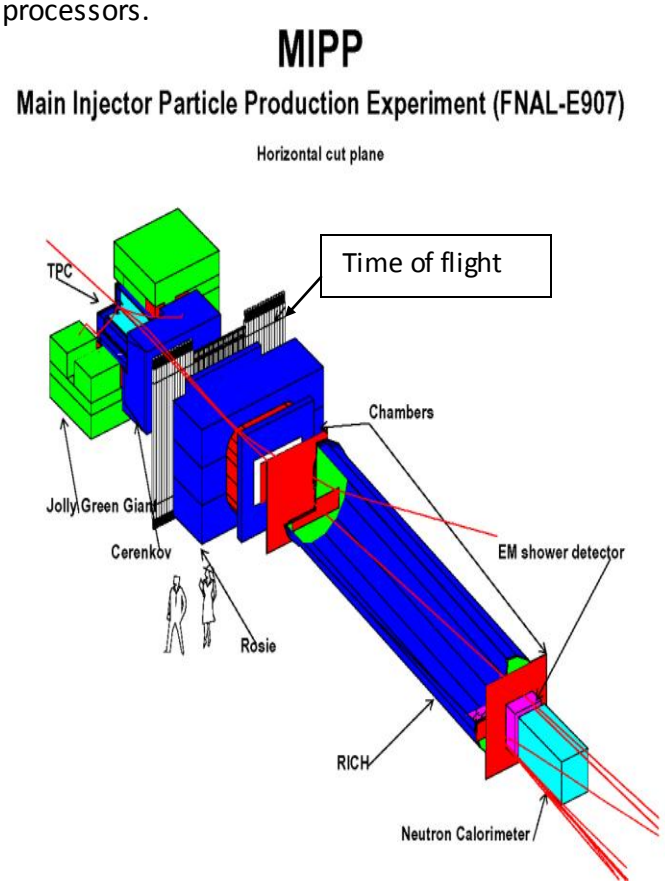

Image 2: MIPP spectrometer

This experiment will also be used to study hadron fragmentation in order to get a better understanding of the behavior of neutrinos. In particle physics, a hadron is a group of particles that contain all particles that interact with the strong force. Hadrons are held together by the strong force similar to how molecules are held together by the electromagnetic force. As shown in image 2, the injector is composed of several components including: detectors and large magnets. The Jolly Green Giant is a 250-ton magnet, named for its size and bright green color, that is used to steer the particles. Cerenkov Detectors are detectors designed to detect the light coherently emitted by the atoms along the path of a relative particle passing through a medium at specific velocity. The angle at which the light is emitted can be calculated using the relation between the distance traveled by the particle and by the emitted radiation in time [5]. The Ring Imaging Cerenkov detector (RICH) will be used to distinguish different charged particle species. Cerenkov radiation is emitted by particles traveling with speeds faster than the speed of light in the radiator material, similar to the sonic boom effect generated by airplanes exceeding the speed of sound in air. The opening angle of the Cerenkov radiation cone measures the speed of the radiating particle (v), which can be used to determine particle mass (m) since the particle momentum (p = mv) is measured independently. The Ring Imaging Cerenkov detector uses a gaseous radiator (C_4F_{10}) in which the particles radiate light. This light is reflected by a spherical mirror. The reflected light is collected by an array of Hybrid Photo Diodes (HPD's) [6]. The EM shower detector uses electronic flow, neutral particles and absence of tracking seeds to suggest cluster structure. Small cells allow a differential approach to cluster resolution. The collective cell approach cancels out the small cell sampling fluctuations. Applicable to both analog and digital readouts, and a test calorimeter will be placed behind the RICH counter in MIPP will enable the study of neutral particle response. Moreover, the most relevant aspect of the MIPP spectrometer, as it relates to the TDC FPGA, is the Time of Flight wall (signified in image 2). The Time of Flight detector is used to precisely measure the time a particle needs to travel from the interaction point to the time of flight detector. The FPGA will be in the MIPP time-of-flight (TOF) readout sub-system. A Time-to Digital converter (TDC) implemented in a field-programmable gate array (FPGA) as high-resolution time measurement device is presented.

Hardware

FPGAs are semiconductor devices composed of programmable logic components that can be configured and re-configured to perform complex combinational functions. FPGAs contain thousands of these logic blocks, and a hierarchy of interconnects that allow the blocks to be "wired together" and connected in any way the user seems fit. FPGAs are programmed using a logic circuit diagram or a source code in a hardware description language to specify how the chip will work.

Image 3: FPGA

The TDC was implemented into the firmware of an Altera Cyclone II FPGA EP2C8T144. This FPGA, shown in image 3, was used to encode the data and register it into some data acquisition (DAQ) circuits. However, there also needed to be a way to transmit the data and allow it to be processed by other network capabilities. Consequently, another FPGA was necessary to complete our project. The Altera Cyclone II FPGA EP25Q208 was used to as a DAQ chip. In other words, it interfaced the TDC FPGA, Synchronous Dynamic Random Access memory (SDRAM), the serial port, the Ethernet circuit, the VMEbus, a flash memory and the USB connection. A RJ-45 connector was used for the serial port, and a DB9 Converter was used for the Ethernet connection. These components were used that the FPGA would be able to transfer data to another processing unit (such as a CPU). A couple of crystal oscillators were used to drive the clock as well as an on-board signal for internal testing. BNC Connectors were used to allow external signals to be passed through the comparators. To download the firmware, a Serial Connector to an Altera USB Blaster is also mounted on the board. The fully built board is shown in image 4 identifying some important hardware components.

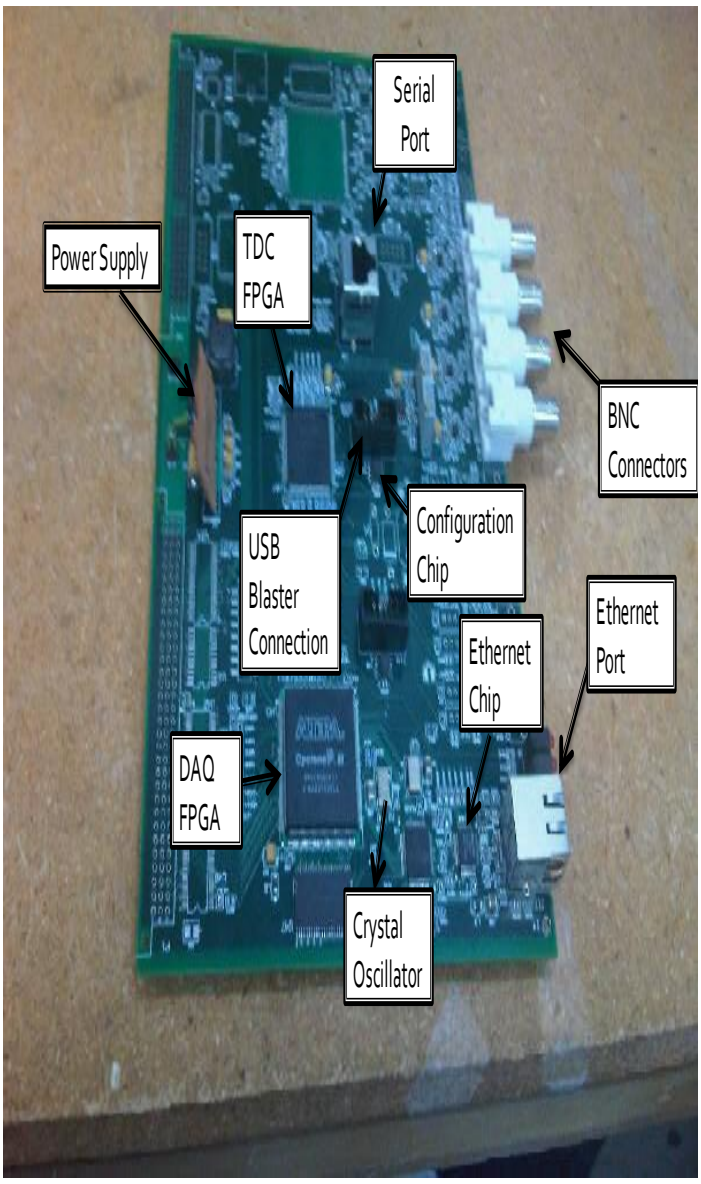

Image 4: TDC Board

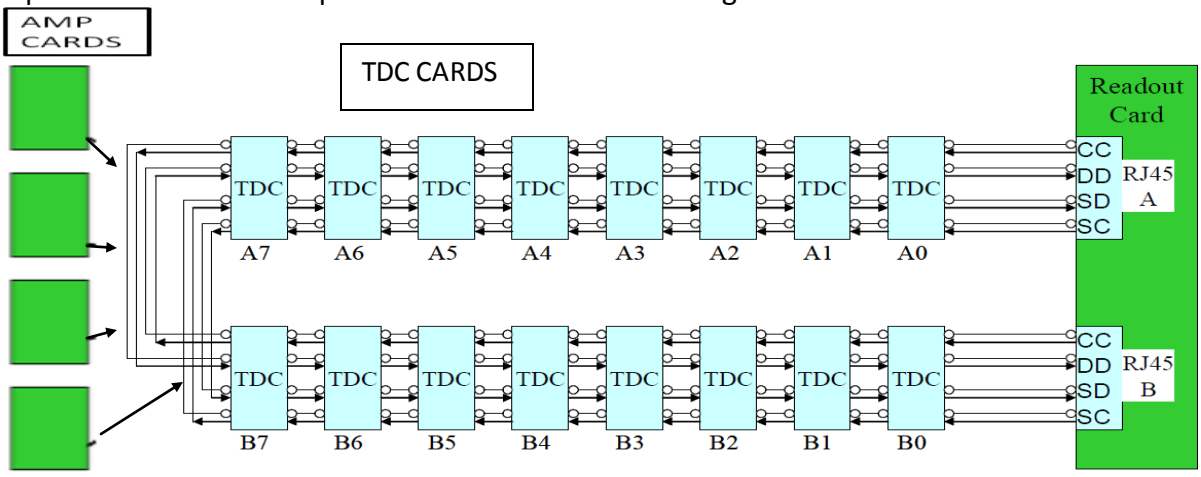

Image 5: TDC System

The architecture of the TDC system is shown in Image 5. When a charged particle hits the TOF wall a pulse will be sent into the TDC board where it is input into a comparator. The pulses are then amplified and compared with thresholds by discriminators to generate differential logic signals in the AMP cards. The hit signals are then transmitted over short cables to the TDC cards mounted near the TOF detector. Each TDC card digitizes 32 channels of inputs [3].

Firmware

There were two major problems in the previously implemented firmware, due to uneven internal delay in the carry chain. The first problem was that the bin widths were unbalanced and depend on temperature and power supply voltage. The second problem was that in many applications, the TDC resolution is limited by the ultra-wide bins, or large variations in the data, correlating with the crossings the logic array blocks. The apparent widths of these ultra-wide bins can be several times bigger than the average bin width.

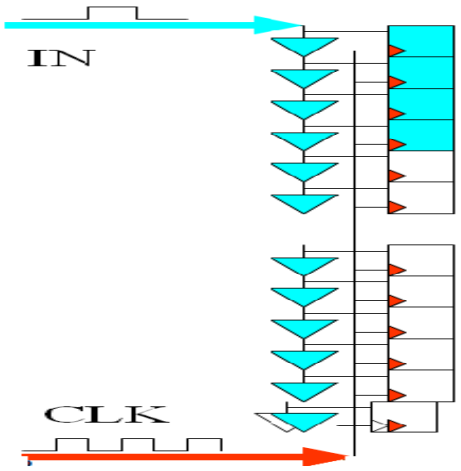

Image 6: FPGA Infrastructure

As you can see in Image 6, the infrastructure of the Cyclone II FPGA is based a chain of logic blocks (LB) connected to delay buffers. Consistently, measuring data accurately with just one input passing into a clock controlled loop of flip flops, that store the input signal in a register array when the clock is high, is very difficult.

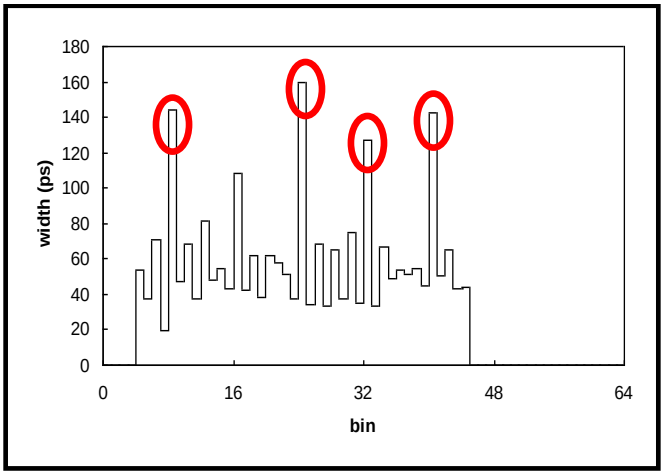

Image 7: Histogram

As you can see in Image 7, there are some ultra-wide bins in the data. The widths of bins are different and vary with supply voltage and temperature. Some bins are ultra-wide due to the logic array block (LAB) structure. Each LAB has its own propagation delay; trying to calculate the total delay and attempting to synchronize the clock to a single signal would be an arduous task, as the propagation delay varies with temperature and supply voltage. However, if we were able to create a better time measurement process, while constructing a functional automated time reference and calibration block structure in the firmware of our TDC FPGA, then the ultra-wide data bins would be eliminated.

The auto-calibration functional block provides semi-continuous calibration that

converts the TDC measurements from bins to picoseconds.

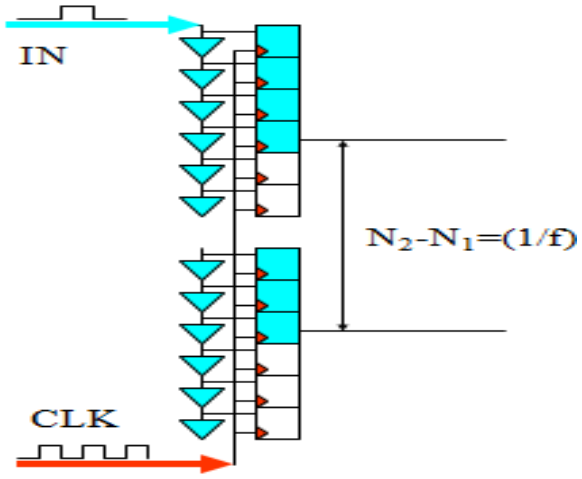

Image 8: Auto-Calibration

The idea was to use longer delay line, thus enabling some signals to be registered twice at two consecutive clock edges. The two measurements can then be used to calibrate the delay, and to reduce digitization errors (as shown in image 8). However, there needed to be a timing reference established so that the system can know when to reset itself.

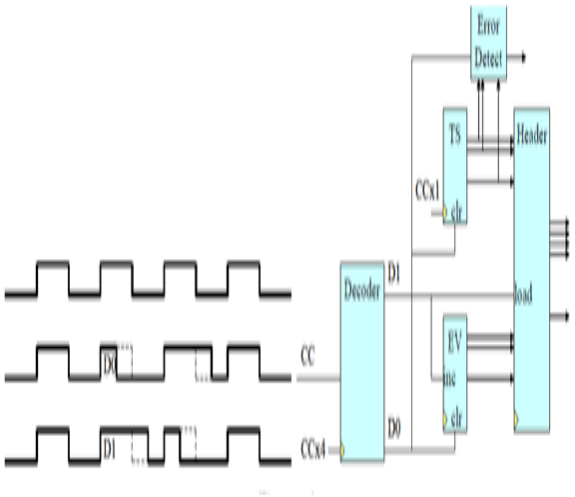

Image 9: Time Stamp

A timing reference, or time stamp, was implemented at the beginning of each run. The readout cards send 50% duty cycle pluses at 26.5 MHz to the differential pairs of the clock line (CC) for several seconds. The phase-lock-loop (PLL) circuits in the TDC cards become stable. However, the time stamp counters are not synchronized yet. At reset, a signal we marked as D0 is carried by the CC signal as shown in image 9. The D0 marker is a 25% duty cycle pulse followed by a 75% duty cycle pulse. Once D0 is detected by the decoder the time stamp counters TS and event counters EV in all TDC FPGA are reset which determines the 0th clock cycle, and time reference, of the data taking run. After a power up or a system reset all input are fed with calibration hits. Once all hits are booked into the histogram, a sequence controller starts to build the lookup table (LUT) in the FPGA internal memory as shown in image 10 below. The LUT is incorporated from the DNL histogram so that it outputs the actual time of the center of the addressed bin. Once the LUT is built, the outputs of the LUT are the TDC times calibrated to the temperature and power supply condition. Each time a new DNL histogram is booked with a certain amount of hits, a new calibration LUT can be built and used for ensuing events.

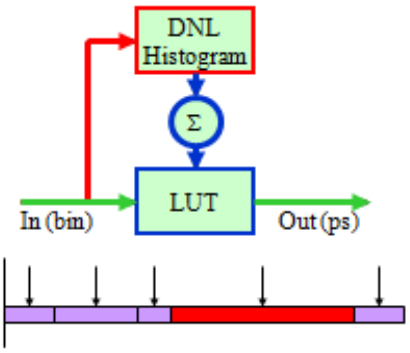

Image 10: Auto- Calibration

The previous time measurement wasn't effective. As a result, a new method was put in place called a "wave union launcher". The wave union launchers are designed to make multiple measurements with a single delay chain structure, in order effectively to sub-divide the ultra-wide bins in each raw measurement. The wave union launcher creates multiple logic transitions after receiving an input signal.

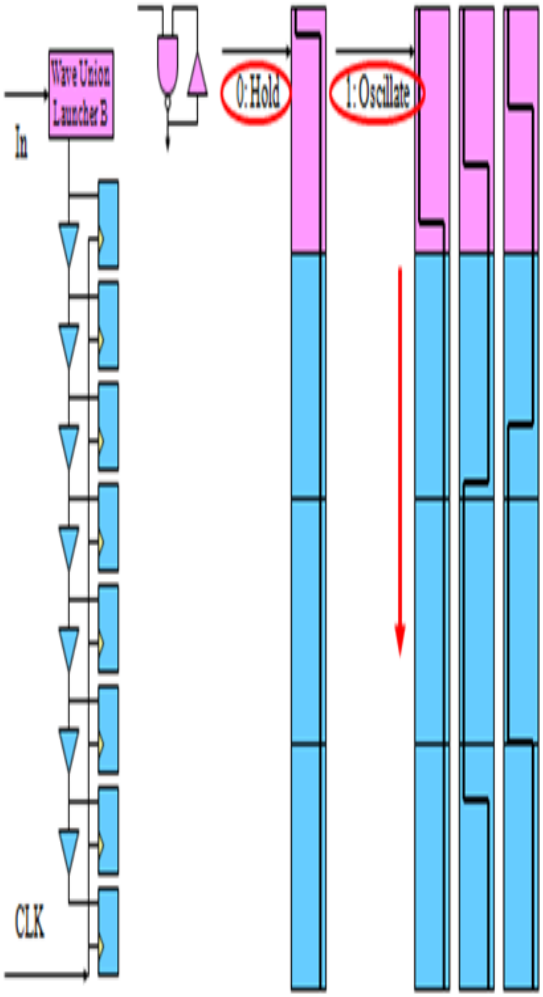

Image 11: Wave Union

When the input level is "0" the output is held at "1". After arrival of the input an infinitely long oscillating logic pattern (or "wave union") starts to launch into the carry chain as shown in image 11. The wave union launcher is simply a ring oscillator enabled by the input, implemented by a NAND gate with a feed back through a delay buffer. The carry chain array structure takes 16 snap shots of the oscillation bit patterns in 16 clock cycles at a frequency of 400MHz. The phase of the oscillation is determined by the arrival time of the input signal measured by the TDC. The oscillation frequency of the ring oscillator is designed to be around 400 MHz. Multiple measurements can be made for one input. In return, an average of the 16 snap shots of the locations of the logic transitions can be utilized to compute the arrival time of the input signal to a higher resolution. A priority encoder is implemented for the output of the lower 48 registers. Only 1 to 0 logic transitions are encoded and the bin numbers are chosen from 16 to 63 with 16 representing earlier and 63 later arrival times, respectively. If in one snap shot more than one valid logic transitions exist, the transition with smaller bin number is chosen [7]. As a result of the auto-calibration and the newly installed wave union, the ultra wide bins where eliminated, as shown in image 12.

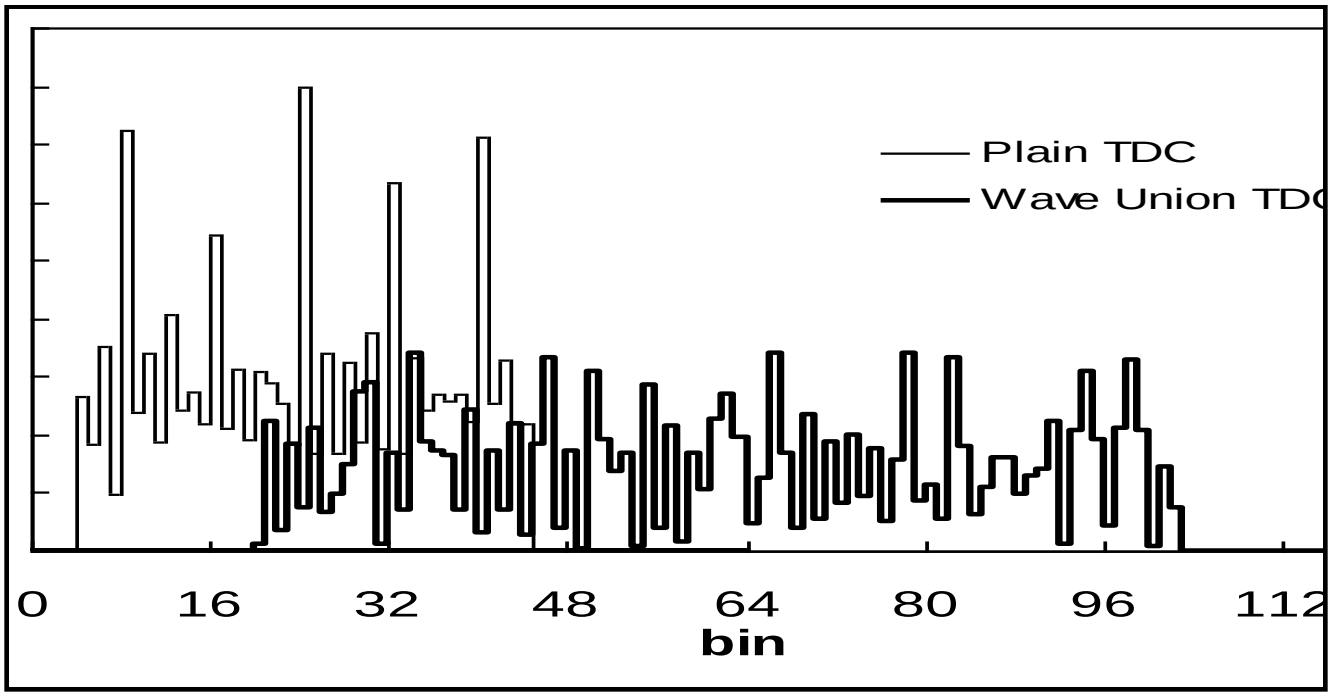

Image 12: Histogram of Wave Union vs. Plain TDC

Testing

The Board was built and the firmware was downloaded successfully into the FPGAs. Some Preliminary tests were done to verify that that the FPGA were able to collect and transmit data. The test was run using a 25 MHz crystal oscillator as an on-board signal. The signal was processed and data was registered from the DAQ counter located in the FPGA shown in image 14. The data was then transmitted through the Ethernet port and displayed in a histogram show in image 15.

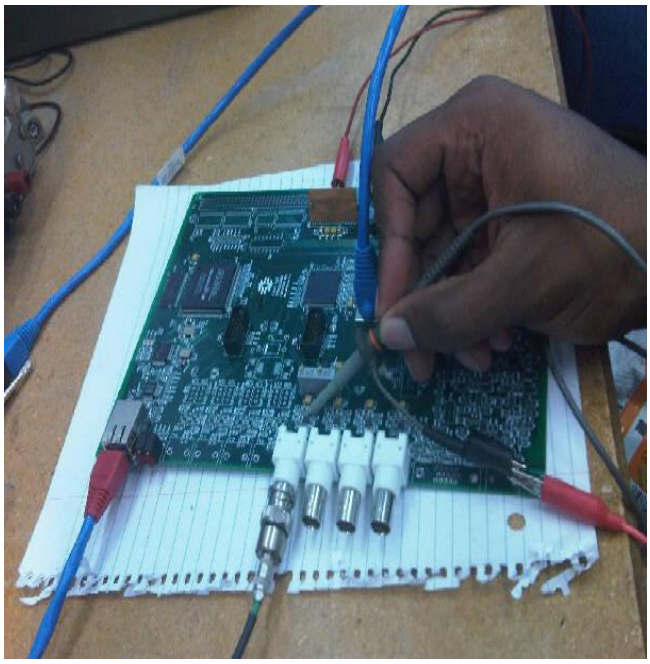

Image 13: Testing Board

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FF80  2222  FF80  2626  FF80  2A2A  FF80  2E2E  FF80  3232  FF80  3636  FF80  3A3A  FF80  3E3E
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Hello World   FTctrlFPGA1
Press DEL to go TDCFPGA ~ to rtn abcdefghijklmnopqrstuvwxyz{|}~

FF80  0202  7F80  0606  7F80  0A0A  7F80  0E0E  7F80  1212  7F80  1616  7F80  1A1A  7F80  1E1E
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Hello World   FTctrlFPGA1
Press DEL to go TDCFPGA ~ to rtn abcdefghijklmnopqrstuvwxyz{|}~
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Image 14: DAQ Counter

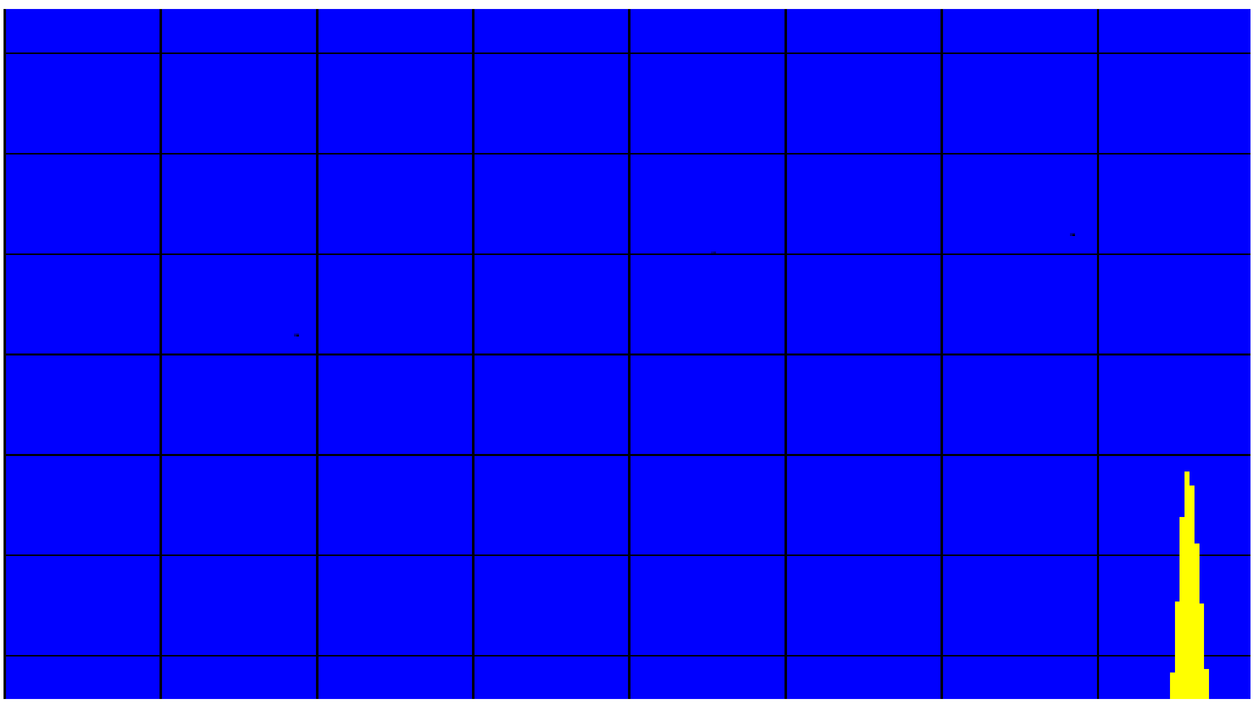

Image 15: Histogram

Conclusion

The TDC board functioned well. Several improvements for the carry chain delay were studied. Viable solutions were found for many problems prevalent in the previously developed firmware. Its new flexible firmware enables it to be utilized in many practical applications. Further improvements can be made on the time resolution and the bin width.

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