# Challenges of High Rate and Multiplicity for Tracking and Vertexing

(A summary of known problems and some proposed development)

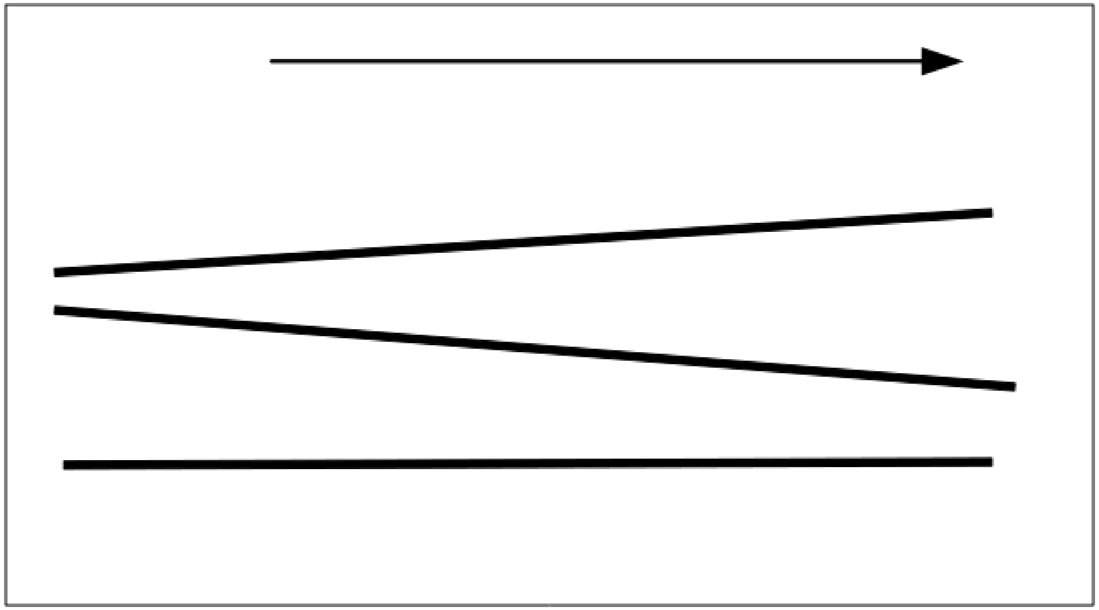
Workshop on Detector R&D
Fermilab, 2010

# Overview

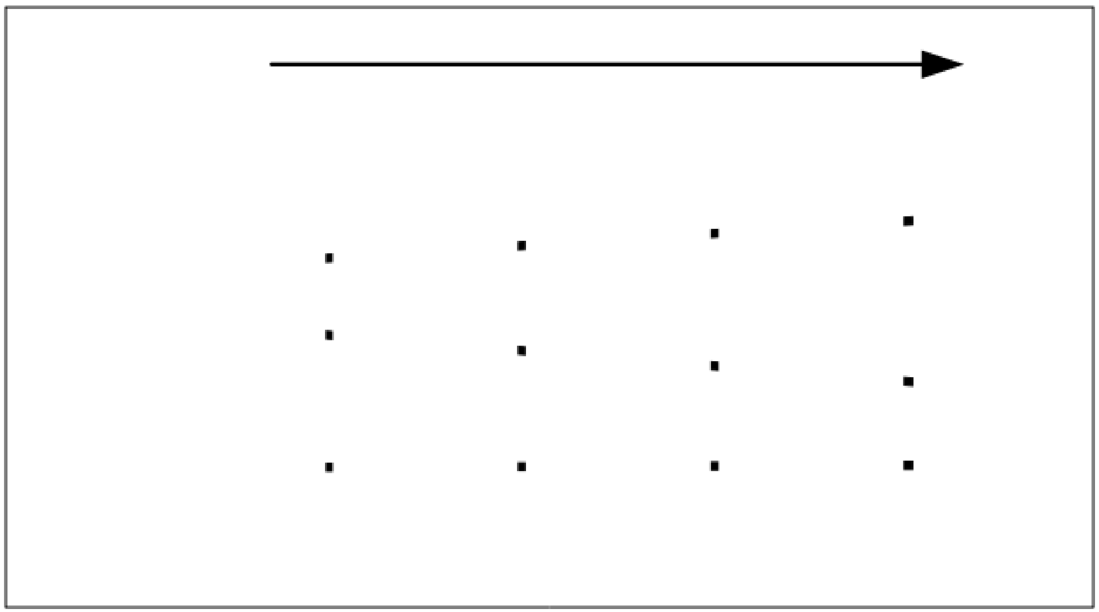
- Problem 1 is high multiplicity AND high rate at the same time
  - Occupancy = fraction of channels busy at an given time
    ~ multiplicity x rate / ( $N_{ch}$ x $BW_{ch}$ )
  - Need low occupancy (<1%) to resolve individual tracks
  - But low occupancy is not enough for finding the correct tracks: sampling density also matters (number of measurement planes)
- Problem 2 is high radiation dose
  - Limits technology choices (along with $BW_{ch}$)
  - Approaching regime where every atom of detector material will be crossed by O(10) MIPs over its lifetime
- Additional problems from performance requirements
  - New capabilities (eg. Trigger)
  - Computational constraints (tracking speed & resources)
  - New colliders with new backgrounds ($e^+e^-$ already covered)

($Bw_{ch}$ = data bandwidth of a single channel: how many hits per unit time.)

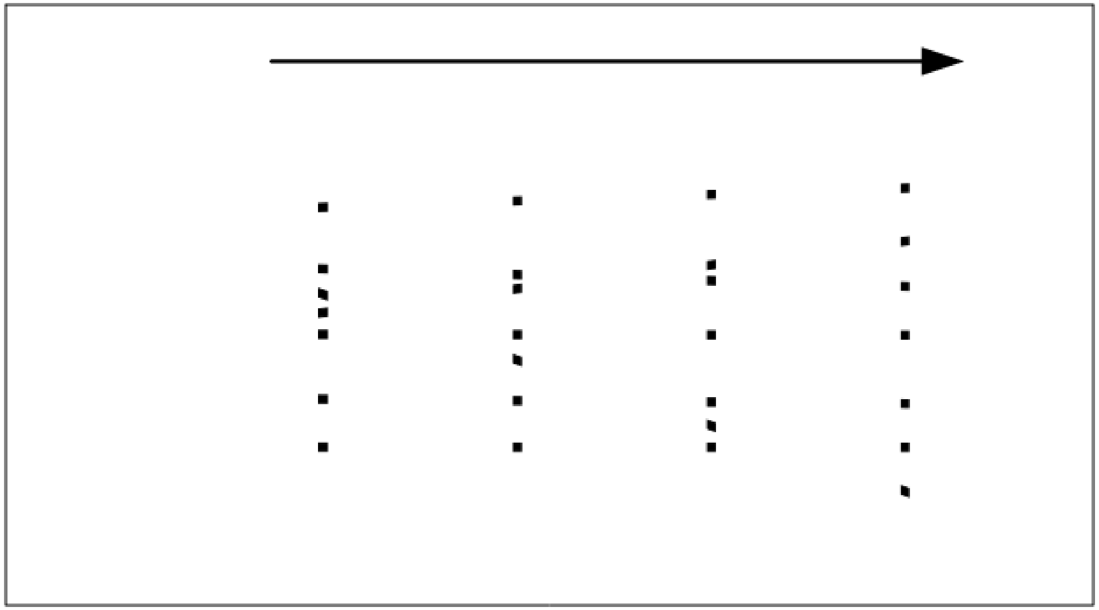
# Low multiplicity cartoon



# Low multiplicity, sparse sampling

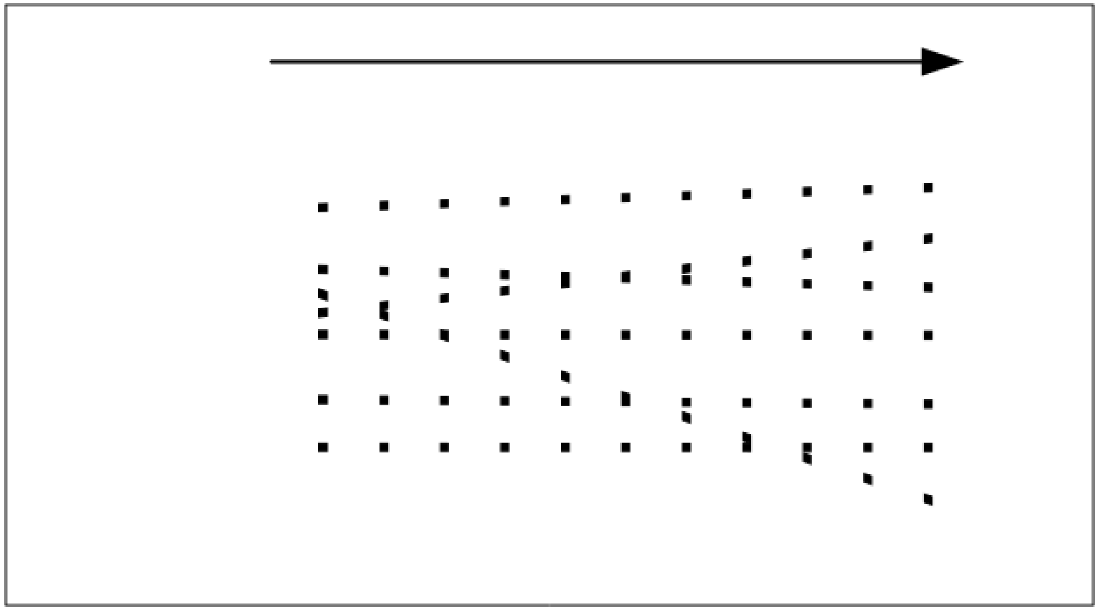


# High multiplicity, sparse sampling



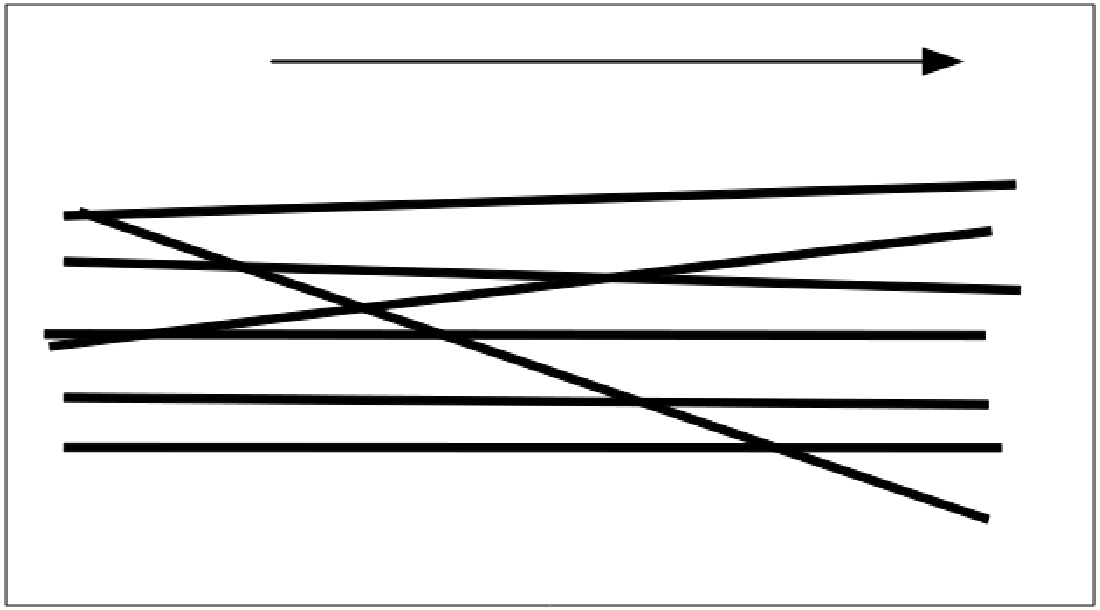
Note there is no lack of granularity in each plane. Every hit is resolved.

# High multiplicity, more samples



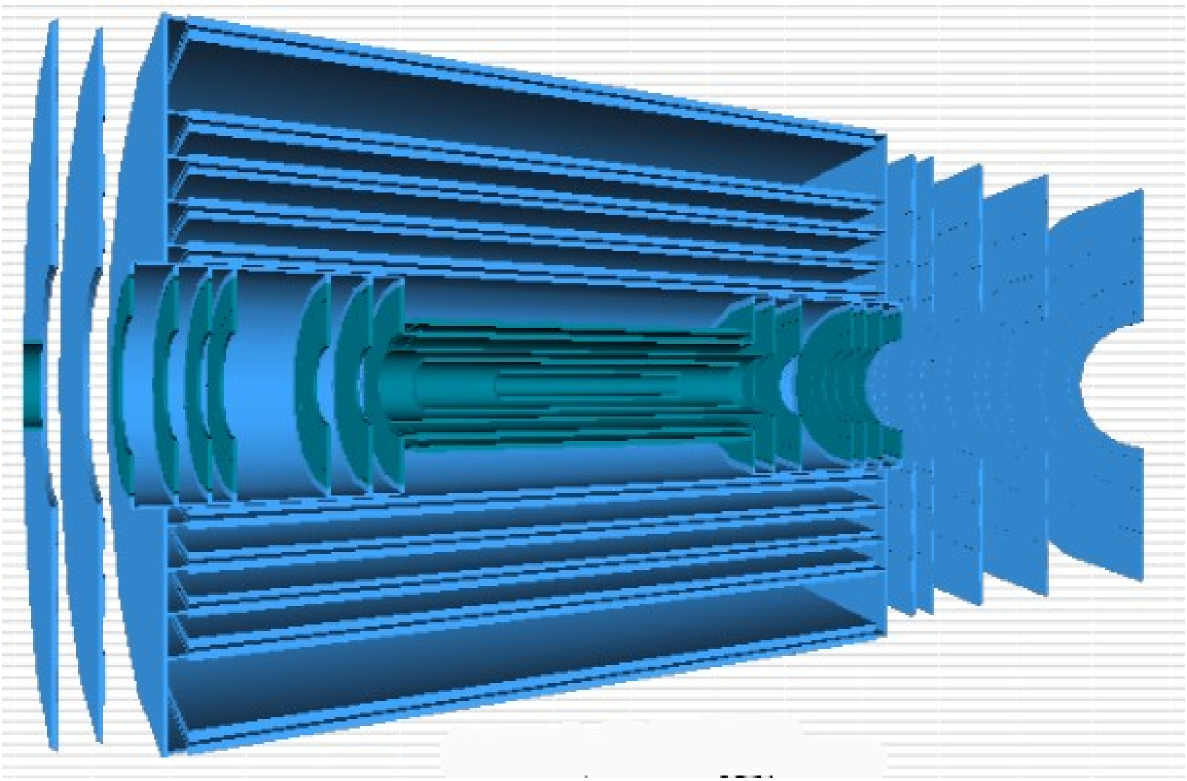
Now the eye can start to see the tracks

# Truth tracks



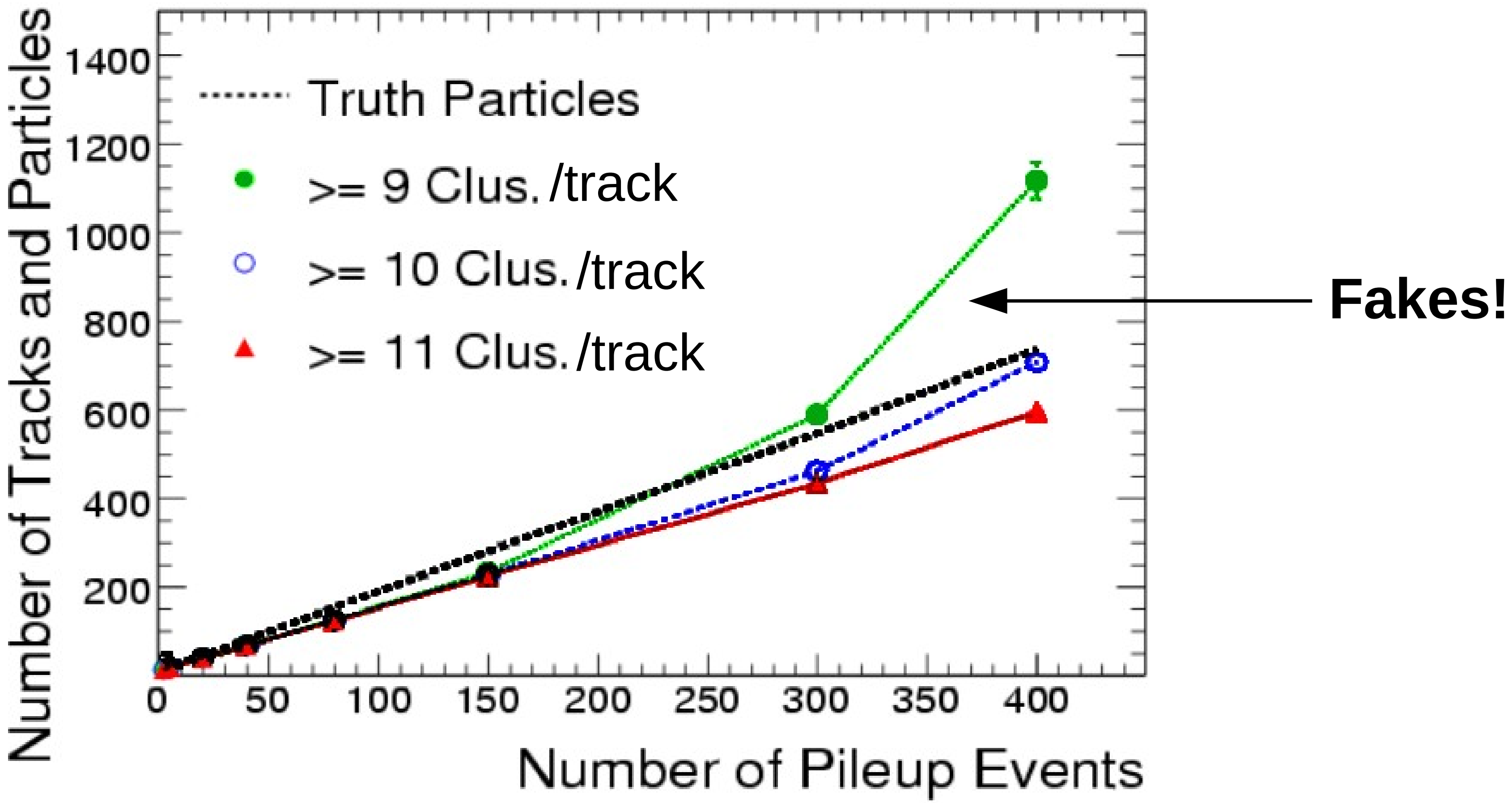
# ATLAS upgrade simulation example

- Same study as illustrated by cartoon, but done with GEANT simulation and ATLAS track reconstruction.



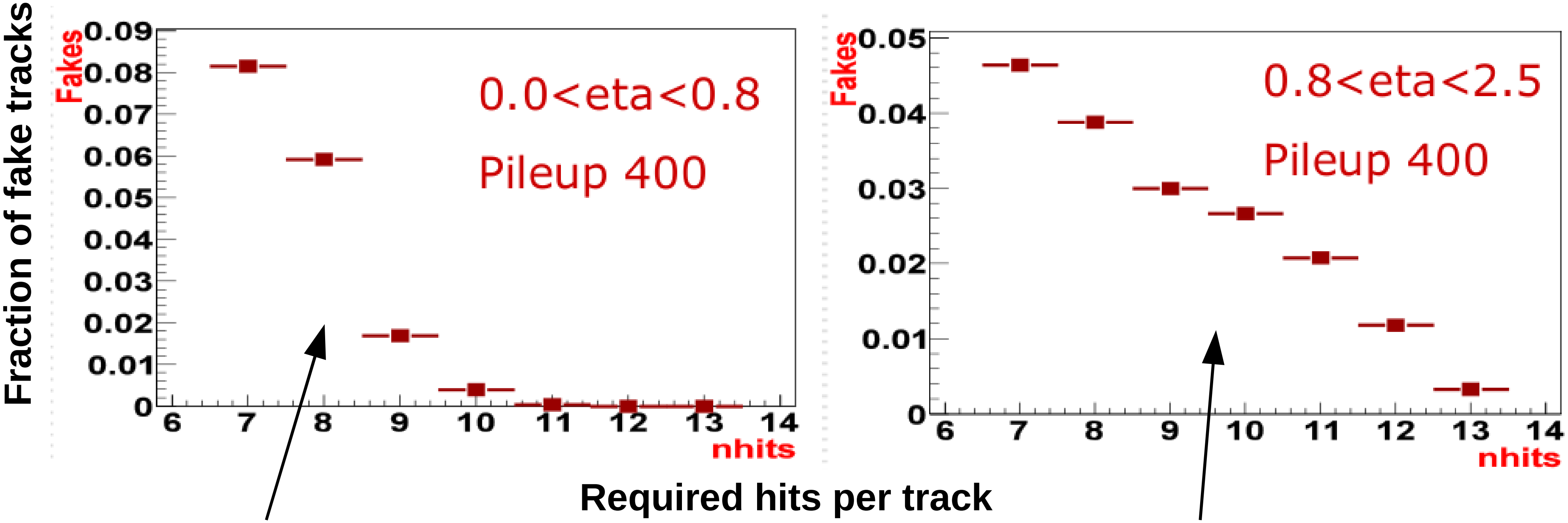
- From inside out each layer is pixels, 2.5cm strips, or 10cm strips to keep occupancy below 1% at highest multiplicity
- Multiplicity is varied by changing the number of piled-up minimum bias events.

# Found tracks vs. multiplicity




*J-F arguin. B. Heinemann, LBNL*

# Need enough hits per track to avoid finding fake tracks




**Looks like a threshold behavior**

**Where is the threshold here?**

- More hits per track = more layers
- More layers = more mass
- But more mass = more tracks ! (secondaries)
  - In this layout there is more mass at higher eta.

*A. Abdesselam, Oxford*

# Conclusions #1

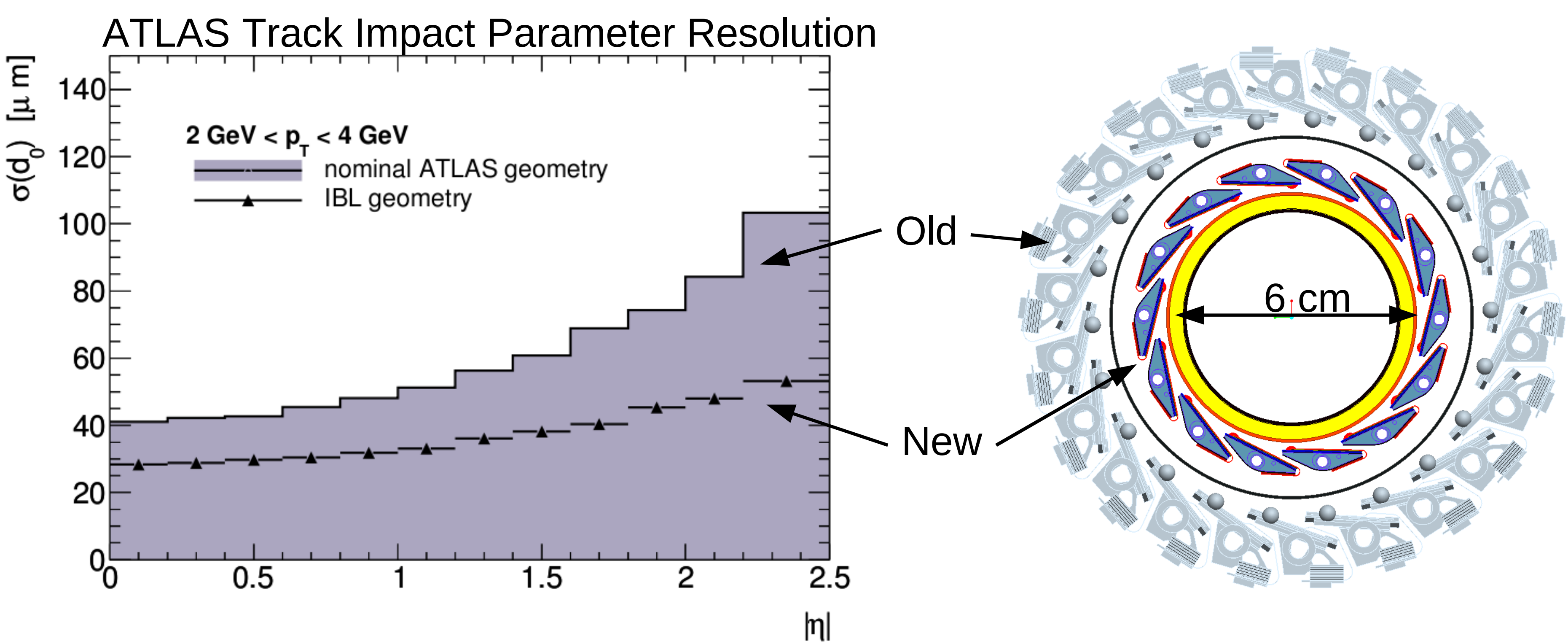
- Lowering mass/layer is not JUST nice for the calorimeters downstream, it is REQUIRED for pattern recognition at high multiplicity
- Theoretical analysis to calculate minimum sampling density needed as a function of multiplicity?

# Vertex Reconstruction

- Specific requirements for e+e- linear colliders covered in dedicated talk
- Vertex finding is based on tracks
- Low track fake rate needed for secondary vertex purity (but no plot to show)
  - Impact of fake rate on secondary vertex tails.
- Main specific requirement is high precision close to IP
- => Extreme radiation environment
  - Main radiation hard challenge lies in inner 1 or 2 layers.
- These layers also have the highest output data rate
  => challenge for readout bandwidth
- High track projection precision means low mass

# Impact of inner layer

- Both Tevatron detectors have a special inner layer with the ultimate technology available at the time.
- ATLAS has “IBL” proposal for new inner layer with newest hybrid pixel technology

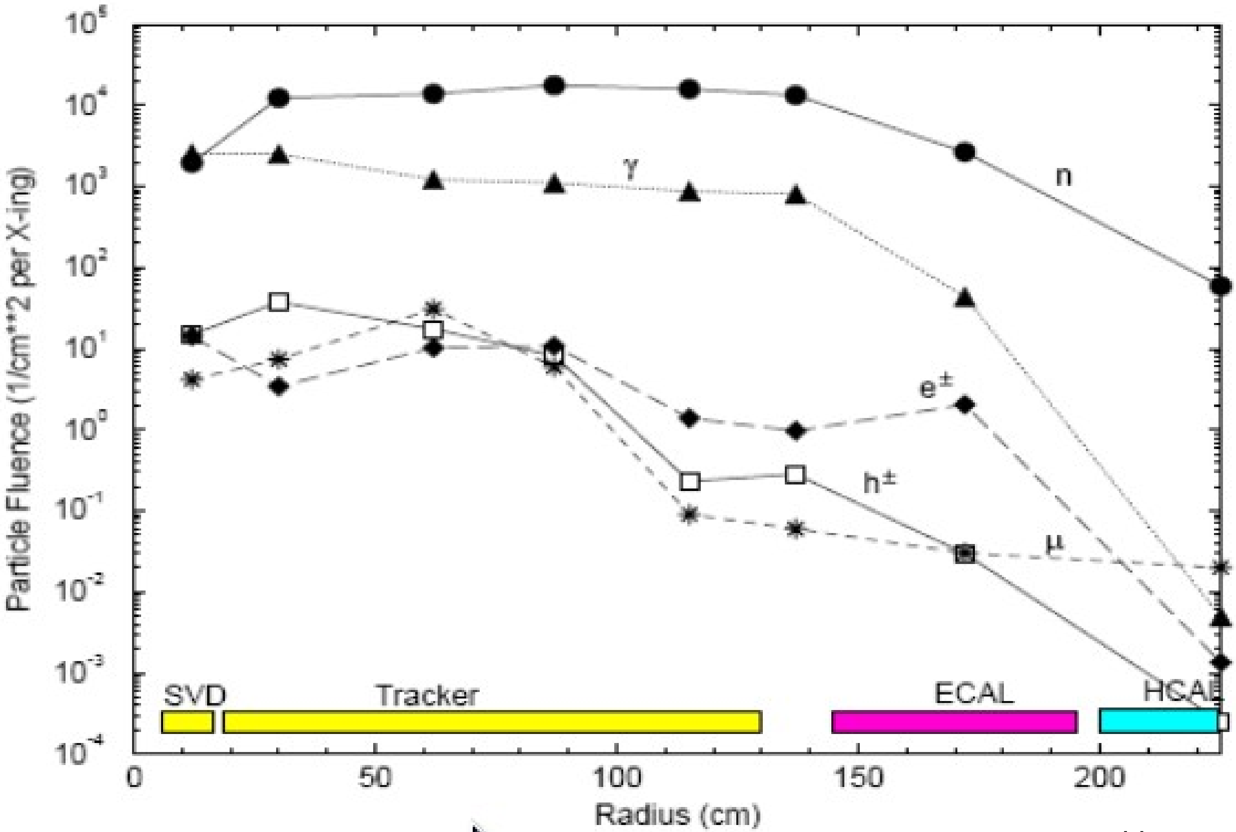



*ATLAS IBL TDR, 2010*

# Background dominated case

- Conditions normally applicable to vertex layers can apply to ALL layers in the case that multiplicity is dominated by non-collision backgrounds.
- Muon collider is the obvious example for now.

Order 40 charged particles / $cm^2$ everywhere in tracker




N. Mokhov, Mu collider Wkshp. 2009

# Conclusions #2

- Want special technology for inner layer(s) Lower mass, but also
  - Extremely radiation hard
  - Very high rate
  - Not necessary affordable for rest of the detector in collision dominated case
- Need this technology everywhere in non collision background case
  - Develop inner layer for SLHC and then figure out how to make them cheaply enough for full tracker of muon collider?

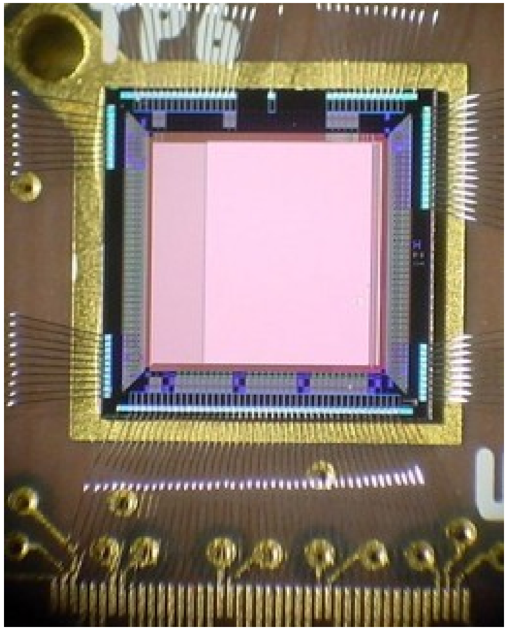
# Technology

Occupancy ~ multiplicity x rate / ( $N_{ch}$ x $BW_{ch}$ )

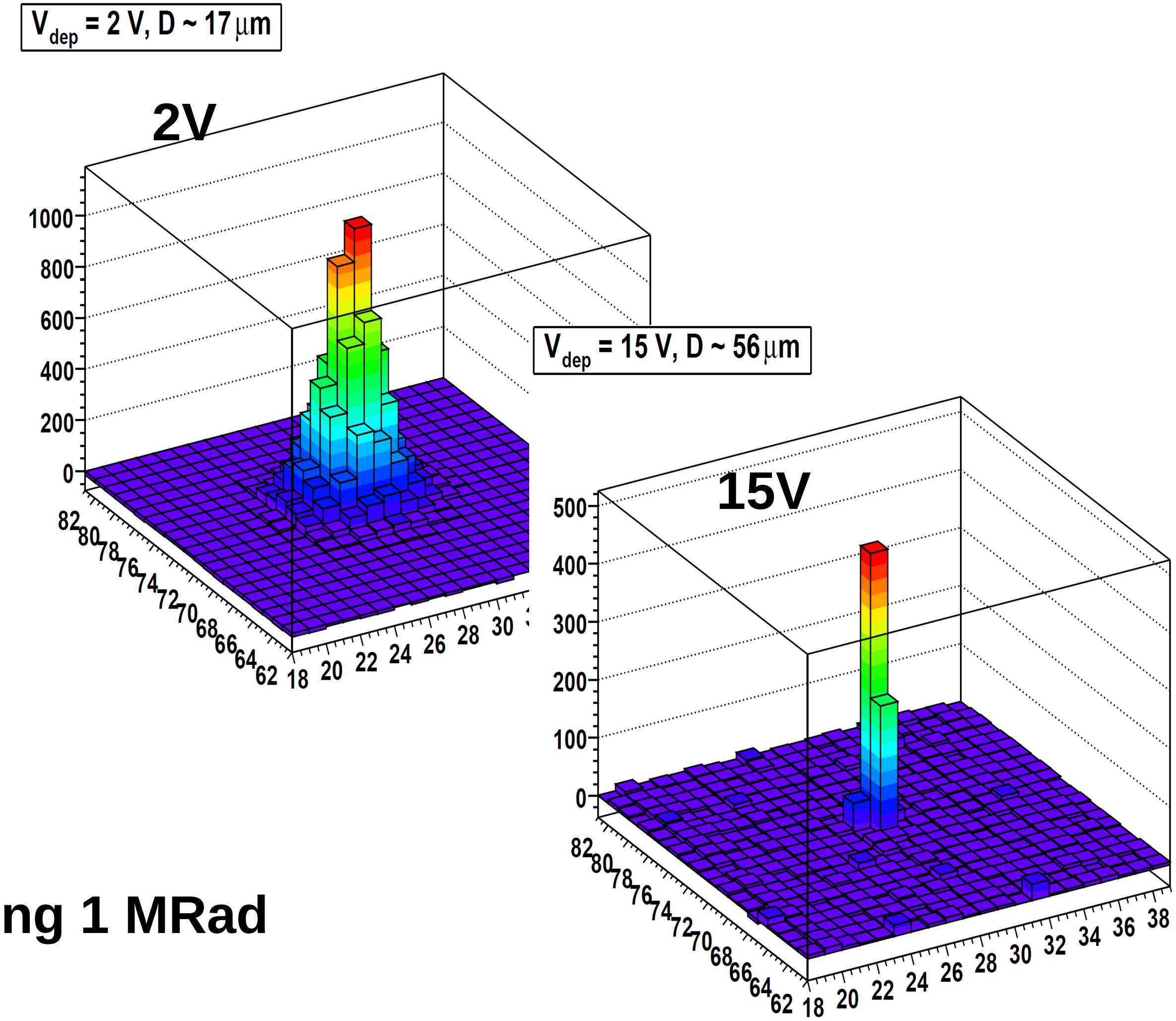
- Hybrid technology (strips and pixels) combines large denominator with radiation hardness.
  - Presently the only solution for high rate and multiplicity.
- High bandwidth (all channels in parallel) is the key.
- Challenges: high bandwidth = power
  large $N_{ch}$ = cost

- Higher granularity technologies are not presently very radiation hard, but even if they were can't compete with hybrid pixels due to significantly lower bandwidth.
- Perhaps could compete with strips however, because while the bandwidth is lower, $N_{ch}$ is very much higher.

# Monolithic Active Pixels on SOI with reverse biased bulk



LDRD-SOI-2 back-illumination with 850 nm laser




After Thinning SOI sensor
to 50 μm and adding
P implant in backplane
via LBNL low-T process:

**Rad hardness approaching 1 MRad**

*D. Contarato, SOI coll. Mtg. 2010; M. Mattaglia, et. al., JINST 4 P04007*

# Hybrid technology road map

| Goal | Likely Target |
|---|---|

| | FE Electronics | Mechanics | System | Sensors |
|---|---|---|---|---|
| Lower mass | Lower power,<br>System-on-chip. | Materials,<br>Integration,<br>Cooling. | Integration,<br>Power distribution. | |
| Lower cost | More<br>channels/chip | Modular<br>assembly | Modular assembly | Larger wafers,<br>Simpler process. |
| More radiation tolerance. | Deep submicron.<br><=45nm ??? | | | Rad hard silicon,<br>Other materials. |
| Higher data rate | Architecture,<br>Deep submicron. | | Data transmission.<br>**(no time to cover)** | |

# Front end electronics has the greatest potential to realize gains

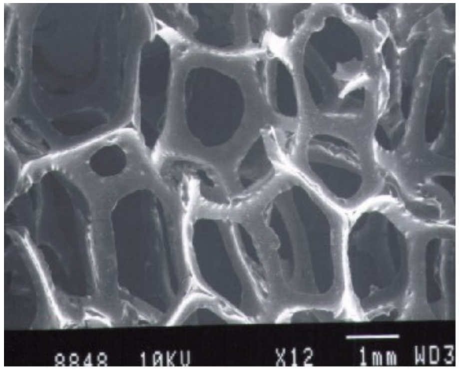
- Power reduction
  - For equal sensor capacitance same performance with lower power requires higher $g_m/I_D$ transistors.
  - CMOS feature size scaling does not provide this.
    - Could use special processes (like SiGe)
  - Or outside the box approach: reduce analog performance and compensate with digital processing.
- Radiation hardness
  - Have been lucky with thin gate oxide
  - Can't assume luck will last forever
  - Are high K metal gate processes rad hard?
    - (45nm feature size and smaller)

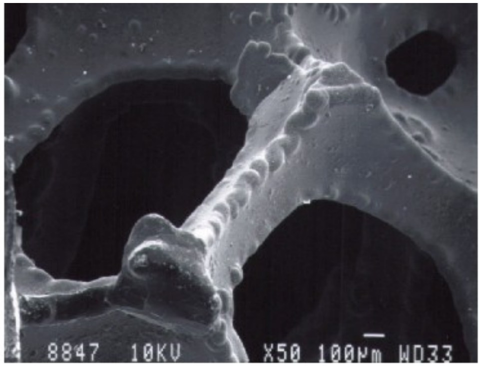
# Electronics continued

- Increased integration
  - More channels per chip
  - High level functionality in front end chip
  - More sophisticated digital design and verification
- System on Chip
  - 3-D integration
  - Deep submicron
  - On-chip power conversion and conditioning
  - Larger design collaborations
  - See FE-I4 poster

# Mechanics

- New materials
  - Fully exploit carbon composite possibilities
    - Example: new type of thermally conductive foam
    - Improved FEA foam models needed




*~20 W/m/K at 0.2 g/cc has been achieved*
*(Allcomp, Inc.)*

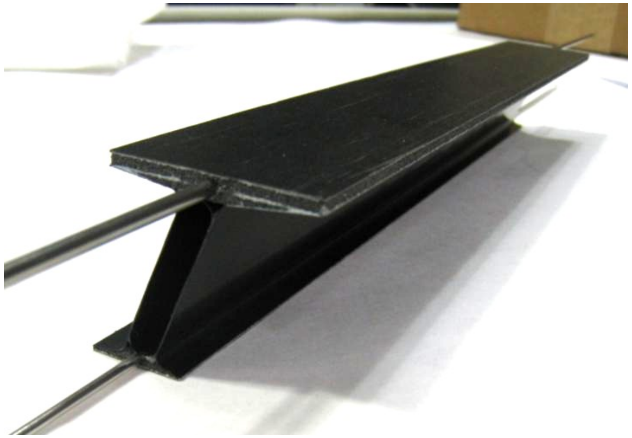
    - Example: braided carbon pipes

*Leak tightness at 100bar seems achievable*

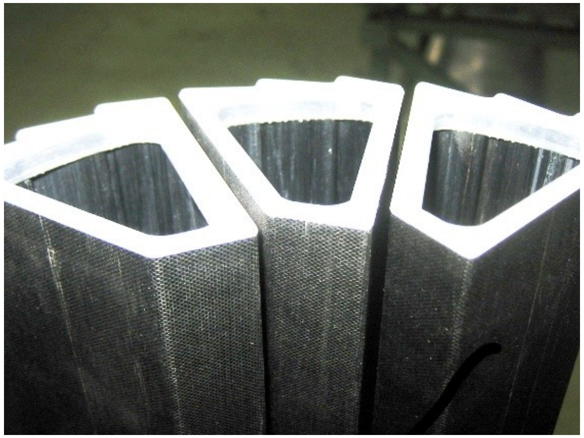
- CO2 cooling
  - Example of LHCb sysyem working very well
  - Generally assumed to be the cooling solution for LHC tracker upgrades

# Mechanics: Layers with shared structure

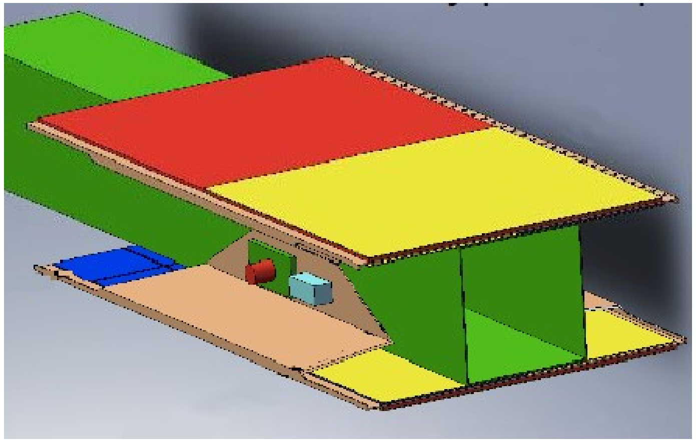
ALICE hybrid pixel wedge



ATLAS pixel R&D I-beam prototype



STAR HFT upgrade air cooled wedges
(CMOS active pixels)



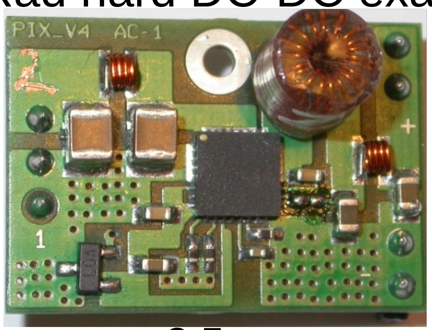
CMS upgrade box beam concept

# Electro-mechanical integration

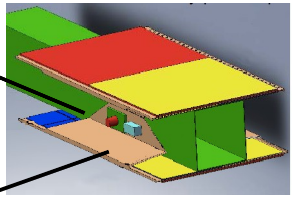
- Mass reduction by making elements serve multiple purposes.
- Assembly effort reduction by integrating large modular units (important to make detectors with very large $N_{ch}$ affordable)
- Power conversion at point of use to minimize electrical services.
  - Lots of work being done on discrete, rad-hard converters.
  - If it can all be done inside the chip that will be best

Rad hard DC-DC example

1.8cm

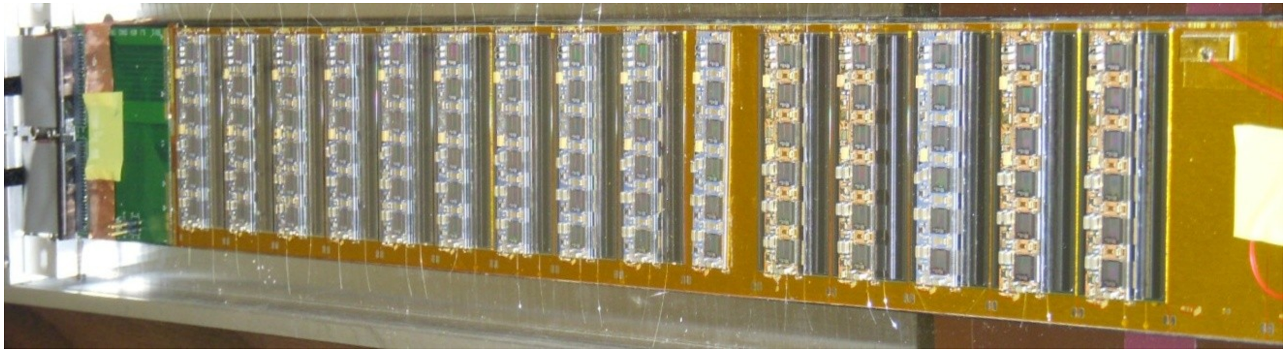



2.5cm



*K. Klein, WIT2010*

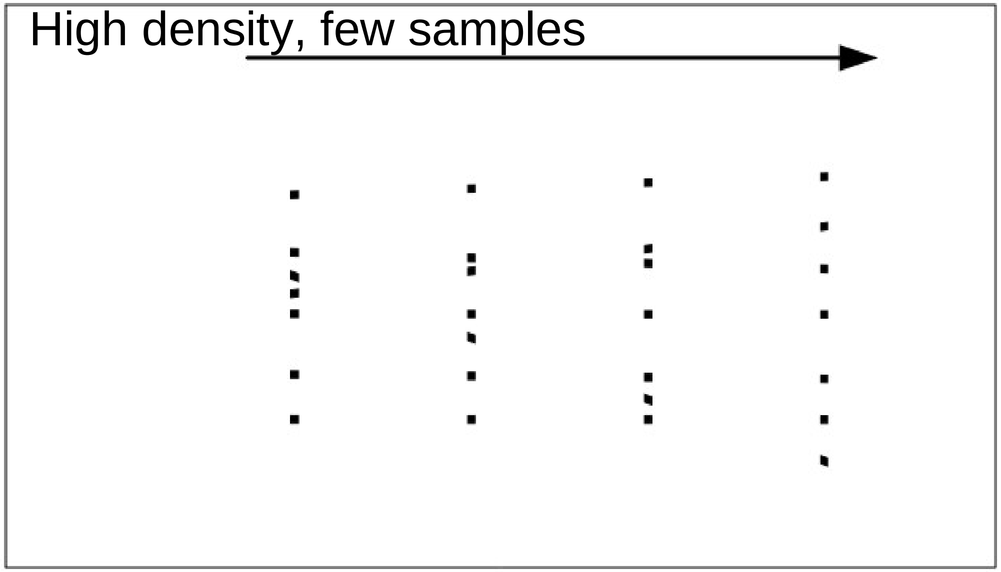
OR:
Serial connection instead of DC-DC conversion:

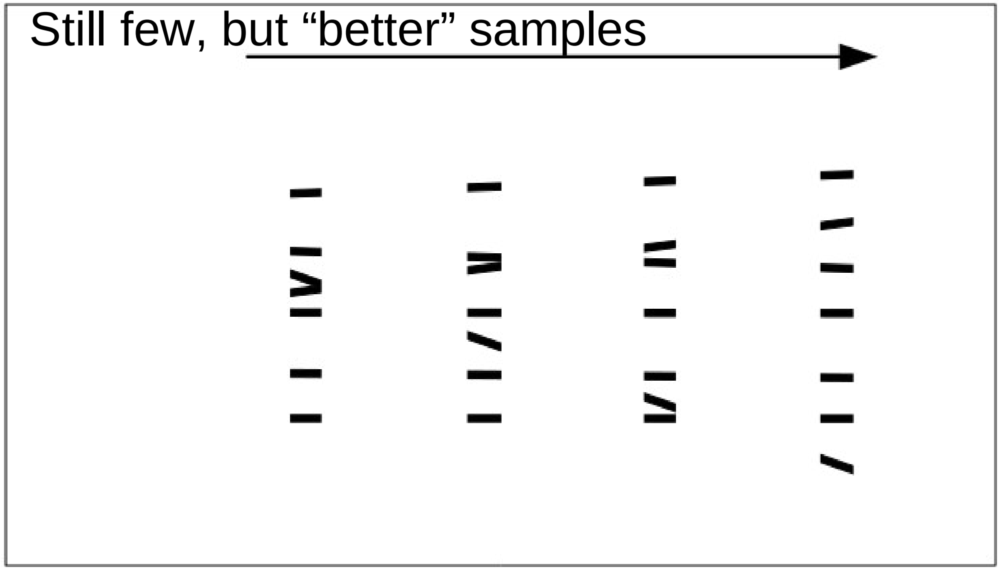
*C. Haber, WIT2010*

# Keep in mind new directions

- May be possible to surpass incremental technology improvements by reinventing the  detector
- Revisit pattern recognition cartoon.



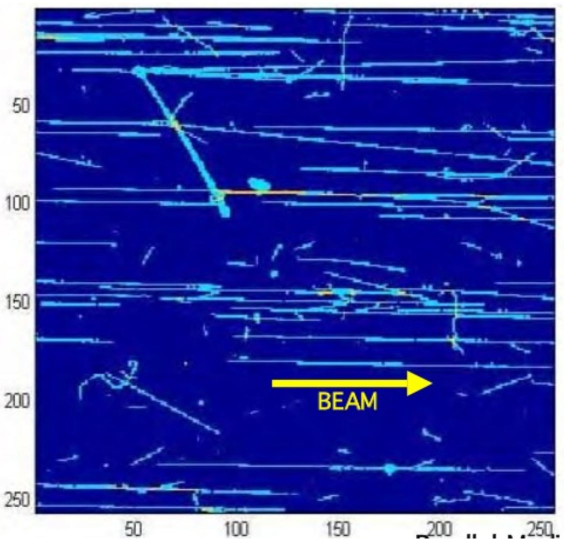

- Instead of more samples
- More information per sample
- Vectors instead of points




- Not really a new concept, but not yet applied to silicon

# Coupled layers

- Significant recent interest in coupling silicon layers not just mechanically, but also electrically in order to produce vectors
  - See eg. proceedings of 2010 Workshop on Intelligent Trackers http://jinst.sissa.it/jinst/common/JINST_proceedings.jsp
- Work has been so far motivated by the possibility to generate a self-seeded track triggers
- However, the vector concept should be considered more generally as a potential high multiplicity high rate solution (solve pattern recognition with potentially lower mass).
- Again a theoretical analysis of the min. number of vector layers needed vs multiplicity would be very useful.
- Extreme case: silicon emulsion --> 120 Gev pi+ beam sideways through Medipix module




*E. Heijne, WIT2010*

# Conclusions / wish list

- Lowering mass/layer is not JUST nice for the calorimeters downstream, it is REQUIRED for pattern recognition at high rate and multiplicity.
- Theoretical analysis of required sampling density needed as a function of multiplicity, for space points or vector samples.
- Want special technology for inner layers or bckd. dominated.
- Hybrid technology presently only candidate, but for outer layers others may be soon viable.
- Front end IC development is the first place to make gains:
  - Reduce power, increase BW, increase integration (lower cost and mass), preserve radiation hardness
- Mechanics and higher level integration (modularity) not far behind.
- New concepts (vector samples, trigger capability) must be explored further.
- Did not cover data transmission