Collider Detector Development

Marcel Demarteau
Fermilab

DOE KA12 Review
June 22-23, 2010

U.S. DEPARTMENT OF ENERGY

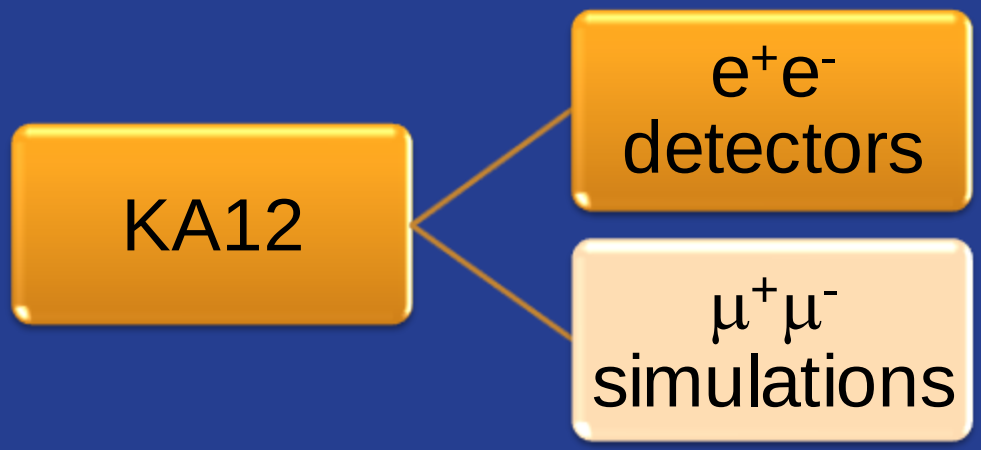
Fermilab

Outline

- Introduction and overall strategic direction
  - Fermilab core capabilities
  - KA12 resources
- Scientific leadership provided by KA12 in:
  - Silicon Sensors
  - Pixilated Photon Detectors
  - Calorimetry
- Three year plan

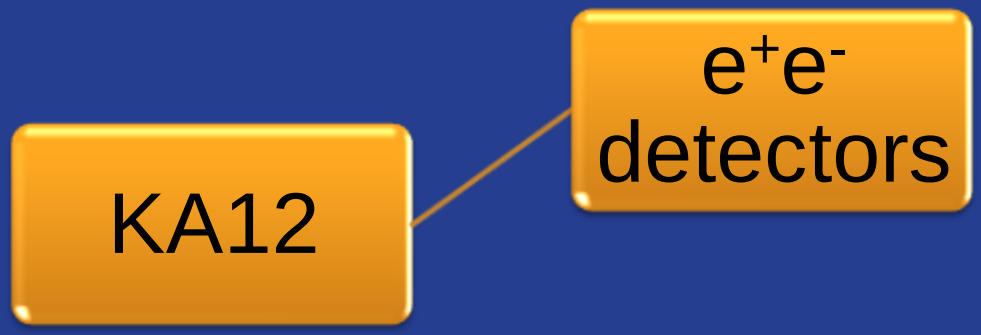
KA12

- Our KA12 budget presentations have two components
  - Existing support for the scientific leadership in the development of e^+e^- detector concepts and new detector technologies
  - Request for additional support in future years, mainly in the area of simulation, for the development of a physics and detector program for the Muon Collider



Current KA12

- Our KA12 budget has supported the scientific leadership in the development of new lepton collider detector technologies
  - This was done in the framework of the ILC
- Our FY10 budget in this category is $756k (mainly SWF)



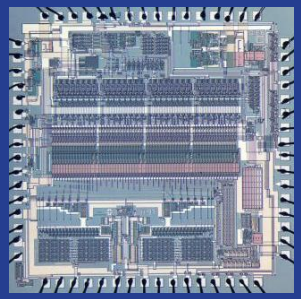
- Description of current activities

Strategy

- Key word is: “To Enable”

- Emphasis is placed on innovation
  - scaling of current technologies is not a viable option
- Goals:
  - Develop novel detector technologies; emphasis on “transformational” technologies, i.e. “high-risk” and “high-payoff”
  - Improve performance of existing technologies by factor of ~ (log) 10
    - Mass budget, radiation hardness, resolution, cost
  - Invest in technologies with broad range of applicability
  - Maximize synergy and coordination among projects
  - Transfer technology to system design

Core Capabilities



- End-to-End Mechanical Engineering
  - Mechanical structures, cryogenics, FEA
- End-to-End Electrical Engineering
  - Front-End ASIC
  - High speed DAQ
- Assembly Facilities
  - Silicon Detector Center
  - Scintillator extrusion
  - Thin film deposition
  - Chamber stringing
  - CNC routing
  - Metrology
- Test Facilities
  - Test Beam at Mtest
  - LAr cryogenics

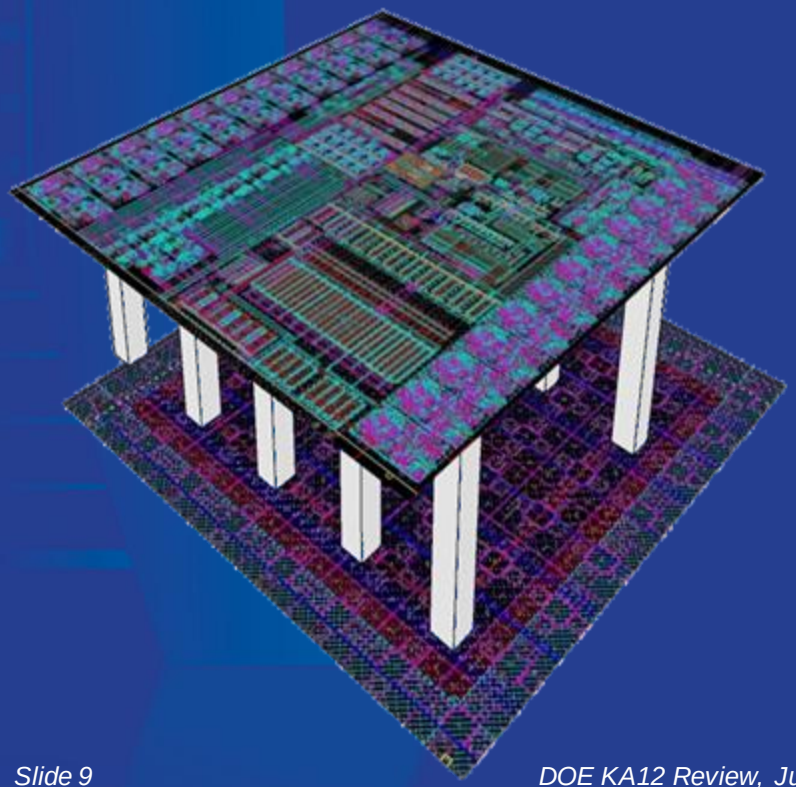
Identification of R&D Areas

- Which R&D areas to focus on?
- Identified those areas that are experimental science drivers, which would benefit most from innovative ideas that match our core strengths
  - Completely driven by scientists supported by KA12

- Higgs and Flavor Physics at LHC, b-factories
  - Vertex and Tracking detectors
  - Critical science enablers, issues with mass, power, dead zones, dead time, occupancy, precision, …
- Jet Energy Resolution and Scale
  - Limits nearly any measurement involving jets
- Scientific Opportunities at new facilities, concept detectors
  - e^+e^-, $\mu^+\mu^-$ detector concepts

Activities in Detector R&D

- Leverage our core capabilities
- Research diagonalized along technologies

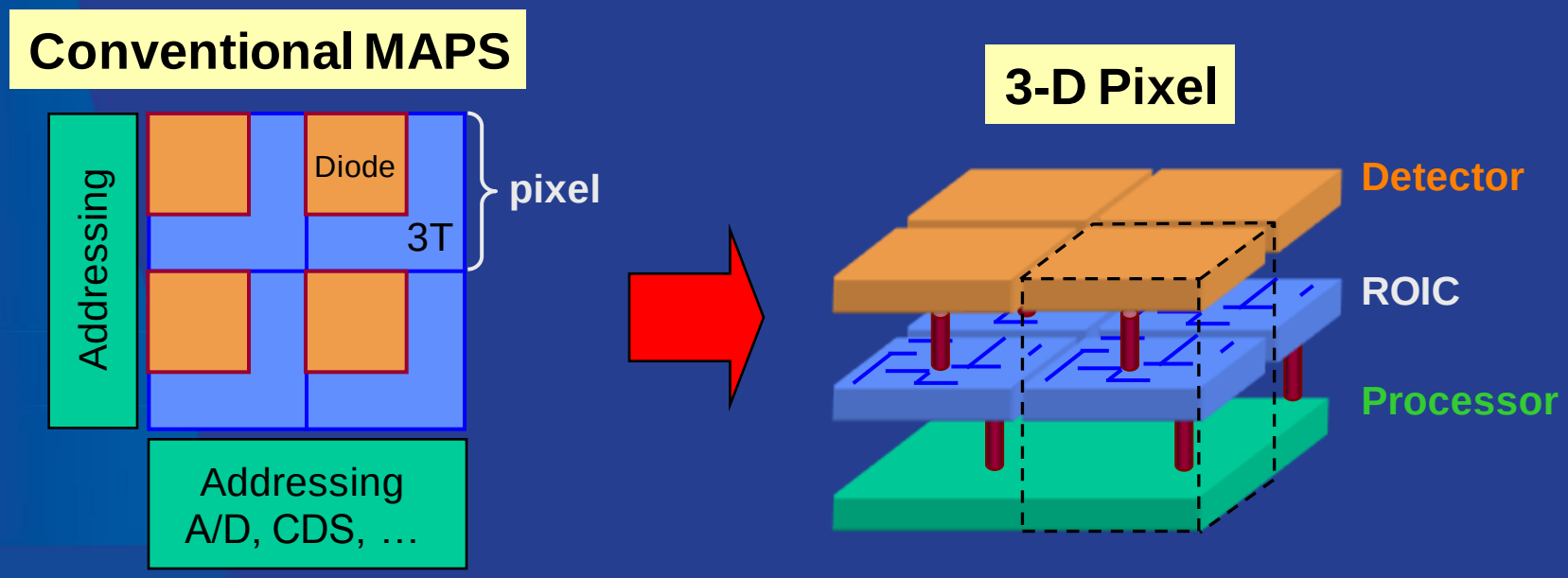


3D Silicon

Key scientists:
Dave Christian, Bill Cooper, Marcel Demarteau, Ron Lipton, Lenny Spiegel

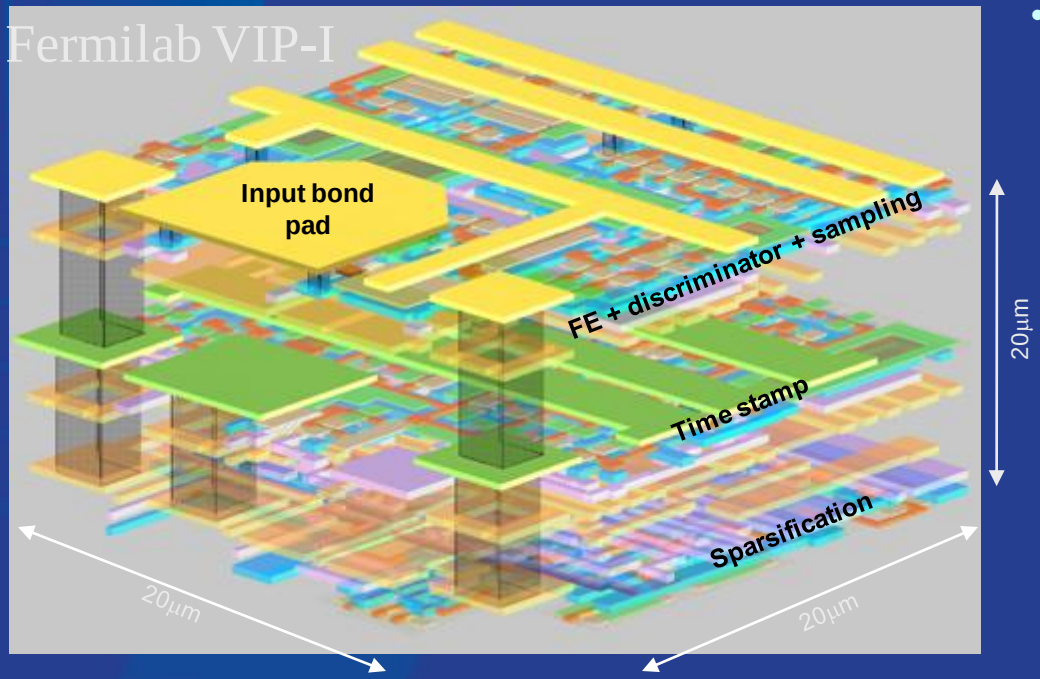
Vertical Integration – 3D

- Vertical integration of thinned and bonded silicon tiers with vertical interconnects between the IC layers
- Technology driven by industry; offers potential for transformational new detectors



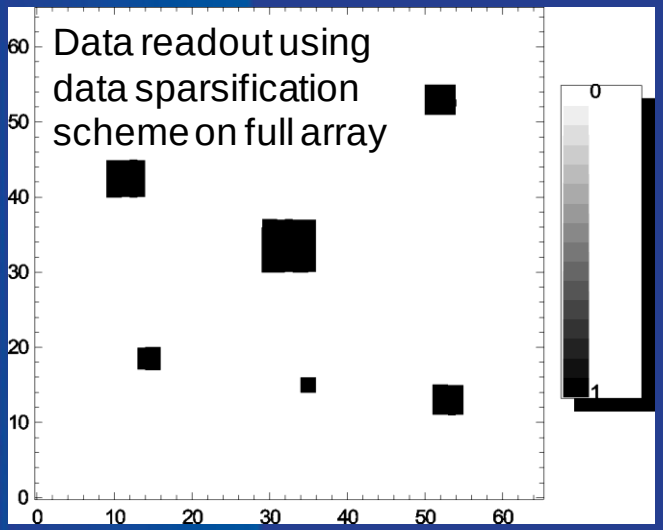
3D Demonstrator Chip

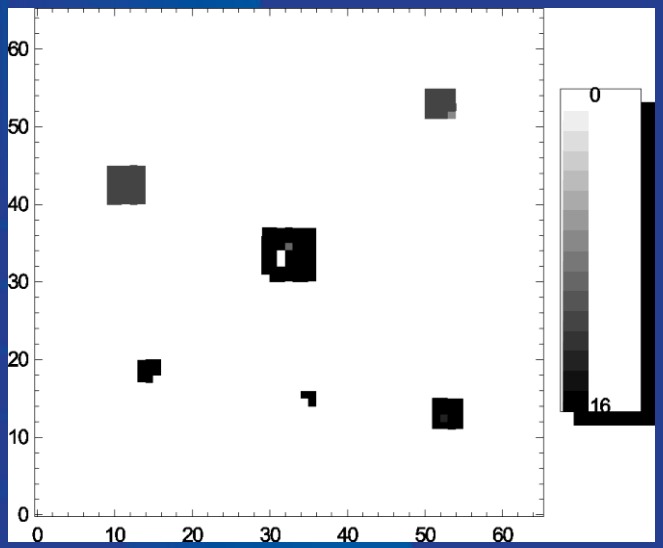
- Fermilab started to actively pursue the 3D technology in early 2006 in collaboration with MIT-LL
  - MIT-LL offered several DARPA funded three-tier multi-project wafer (MWP) runs
- Designed Vertical Integrated Pixel (VIP) Chip for ILC detector readout



- VIP-I Design
  - 3D design in three-tier, via last, 0.18 µm SOI process
  - 64 x 64 pixel array, 20x20 μm^2 pixels, scalable to 1M pixels
  - Data sparsification, 5-bit digital and analog time stamp, high speed token passing
  - Analog output
  - No integrated sensor

VIP-1 and VIP-2a





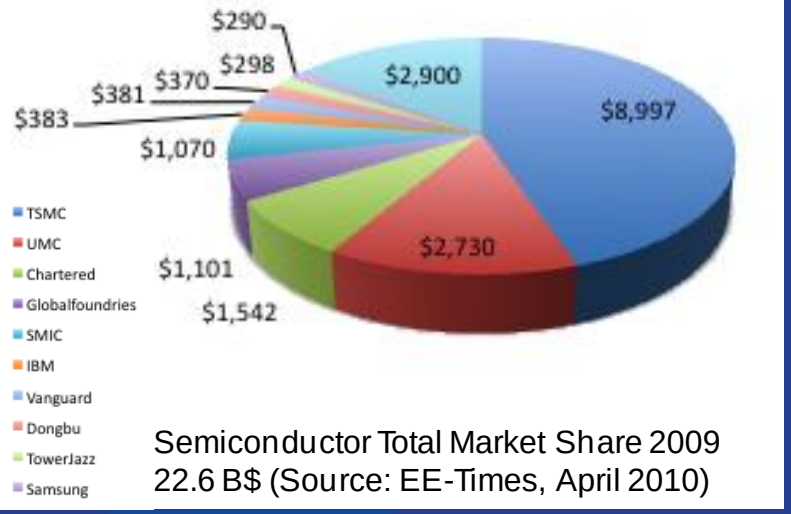
Preselected Injection (top) and Readout (bottom) pattern of pixels reported as hit using data sparsification

- VIP-1 chip submitted Oct. 2006; ~20 devices delivered late 2007; chip works !
- Major breakthrough in the development of advanced ASICs and integrated detector systems

- An improved version of VIP-1 has been submitted to MIT-LL on October 13, 2008 (150nm, SOI, 3 tiers): VIP-2a
  - Different power and grounding layout;
  - Redundant vias and larger traces in critical paths
  - Added diagnostics
  - Slightly larger pixels

Collaboration with Industry

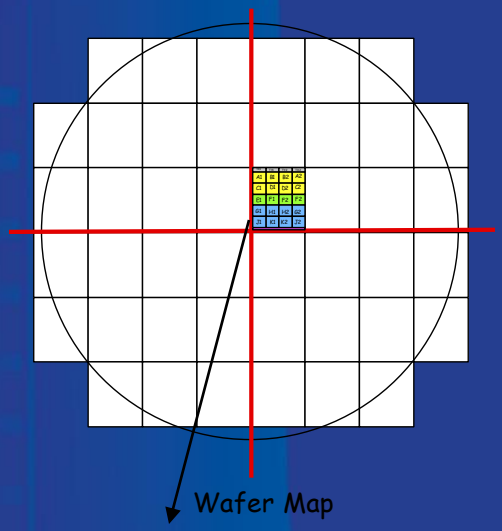
- 3D technology driven by industry
- We started an initiative with local vendor, Tezzaron, willing to accept MPW runs
- Tezzaron:
  - One of the leaders in developing 3D technology
  - Wafers are fabricated by Chartered in Singapore
    - Chartered bought by GlobalFoundries in 4Q09
  - 3D assembly is completed by Tezzaron in Singapore

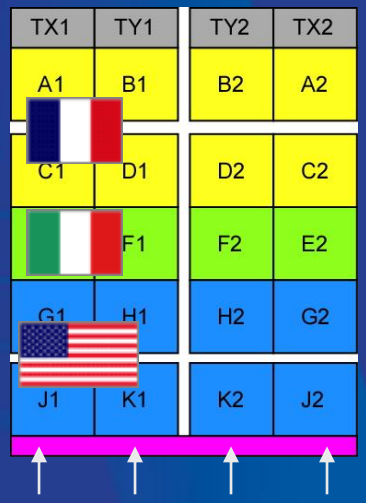


Semiconductor Total Market Share 2009
22.6 B$ (Source: EE-Times, April 2010)

- Advantages:
  - Existing rules for vias and bonding
  - Relatively fast turn around
  - One stop shopping for wafer fabrication, via formation, thinning, bonding
  - Process is available to all customers
  - Low cost

Fermilab 3D Multi-Project Run





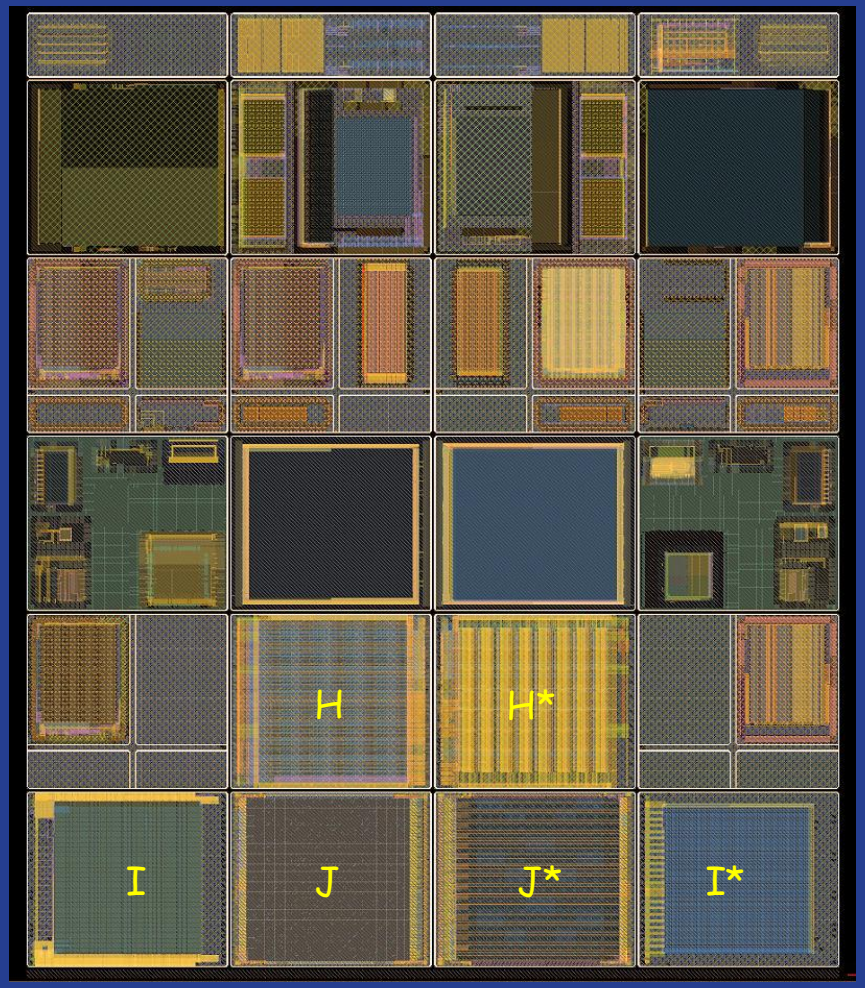
Reticle Layout

- Fermilab formed a 3D collaboration and hosted a 3D multi project run with Tezzaron
  - Two layers of electronics fabricated in the Chartered 130 nm process, useful reticle size is 16x24 mm
  - Wafers will be bonded face to face
  - Submission closed September 2009
- 17 Participating institutions in the MPW run
  - Fermilab host
  - 14 European institutions
  - Two US institutions (LBNL, BNL)
  - Application for b-factory, ILC, CMS, ATLAS, imaging, …
- Frame divided into 12 sub-reticules for consortium members; more than 25 two-tier designs

MWP Full Frame Layout

Test chips:
TX, TY
2.0 x 6.3 mm

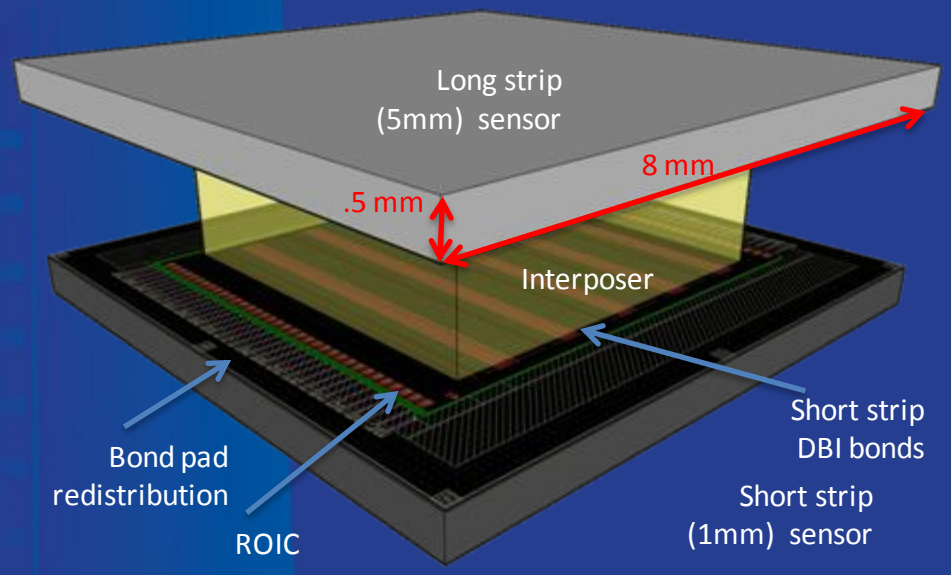
Subreticules:
A, B, C, D,
E, F, G, H, I, J
5.5 x 6.3 mm

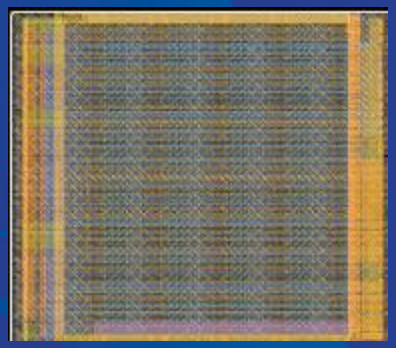


Notice
Symmetry
about vertical
center line

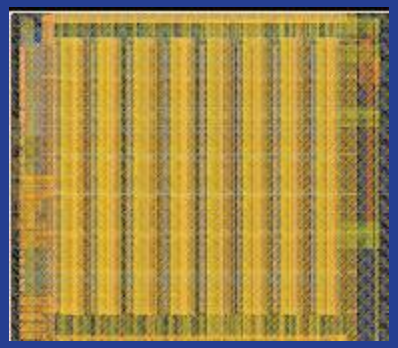
← Top tiers → ← Bottom Tiers →

Fermilab 3D Project: VICTR





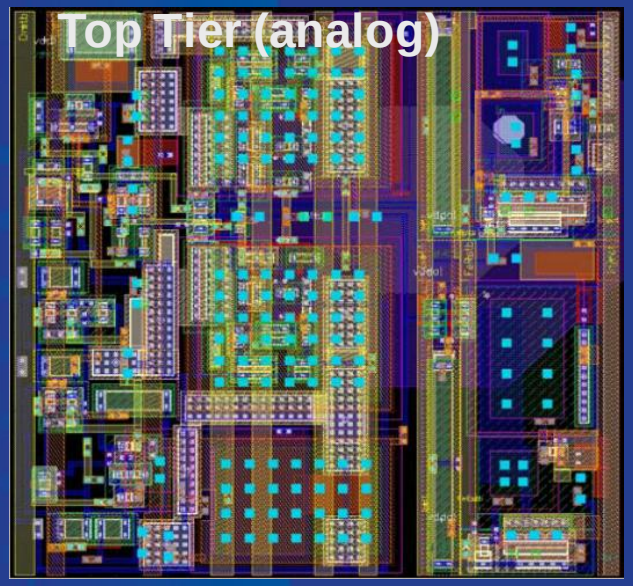
H Left

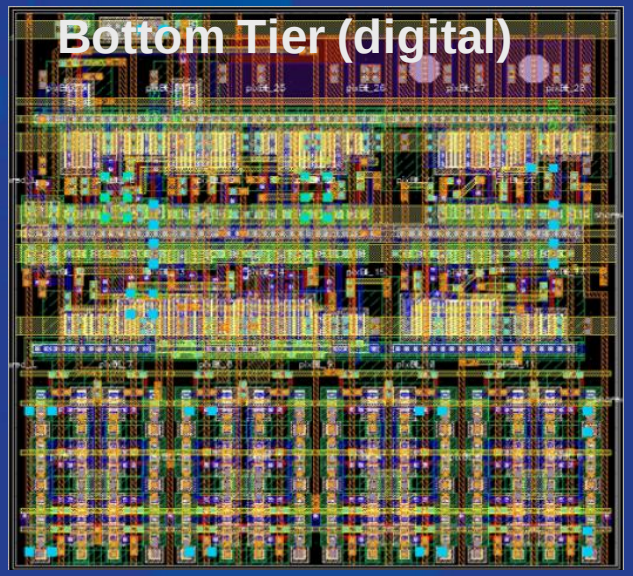


H Right

- Vertical Integrated CMS TRigger chip
- Form a track-trigger at the first trigger level for sLHC
  - Momentum filter using a pair of Si sensors separated by ~1mm
- Data flow is vertical !
  - Hits from two sensors correlated
- Chip design:
  - The top tier looks for hits from long strips to provide phi information
  - The bottom tier looks for coincidence between phi and shorter z strips connected to bottom tier through interposer
- Could be used for hit correlations at Muon Collider

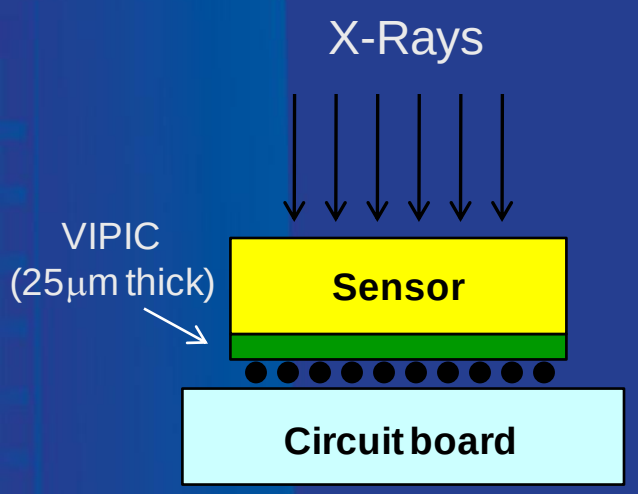
3D Project: VIP-2b

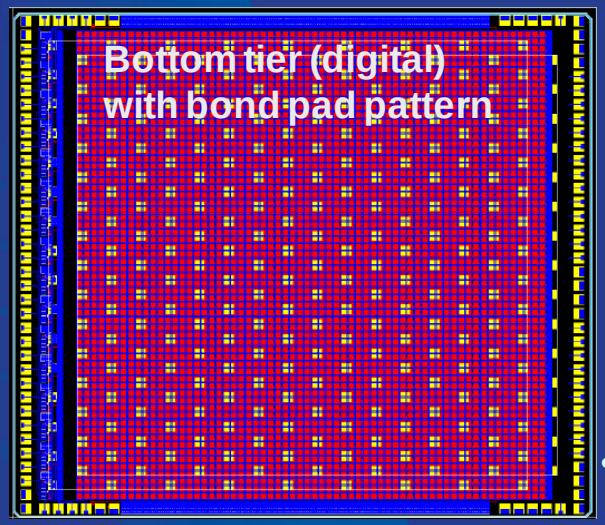




- The ILC 3-tier VIP2 design (MIT-LL) converted to a 2-tier design (VIP-2b)
  - 192 x 192 array, 24x24 μm^2 pixels
  - Removed analog time stamp
  - Increased digital time stamp from 5 bits to 8 bits for ~3.9 us resolution
  - Switch for collection of h^+ or e^-
- Through silicon vias implemented
  - Allows for I/O connections through either the top or the bottom of the chip.
- Connections to vias on the bottom side can lead to four side buttable layouts with absolute lowest circuit and sensor mass.

3D Project: VIPIC





- Vertical Integrating Pixel Imaging Chip (VIPIC)
  - Evaluating application for X-ray photon correlation spectroscopy (XPCS) in collaboration with BNL to calculate autocorrelation function per pixel
- Functionality
  - 64x64 array of 80x80 μm^2 pixels
  - γ flux: 1000 γ/pixel/s
  - Dead timeless, triggerless operation
  - Sparsified data readout
  - Binary readout (no energy information)
  - High speed frame readout time
  - 16 serial high speed LVDS output lines
- Pads for backside bump bonding allows for 4-side buttable arrays

Timeline and Schedule

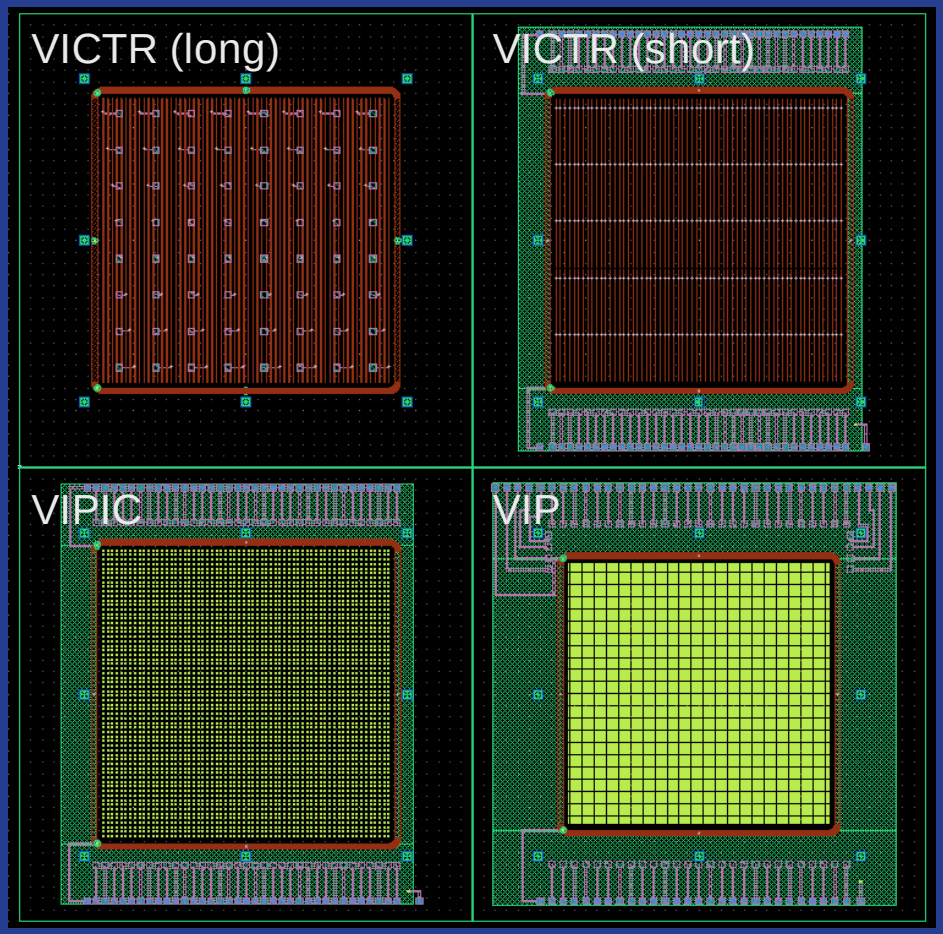
- All designs were received by Fermilab in May 2009
- June 2009 – March 2010 spent preparing and reviewing the submission(s)
  - Note, this was the first time for Fermilab and Tezzaron to organize a MPW run and there were a large number of 'growing pains'
    - Frame and street definitions
    - Design kit incompatibilities, software bugs
    - TSV issues: protection, spacing, bond interface
- March 6, 2010: Fabrication started
- Awaiting return of 2D and 3D wafers from 1st MPW run in mid-July

Future

- New consortium members have been added and space for the next MPW run is fully booked
- Our success has not gone unnoticed by industry: MOSIS (US), CPM (Europe), CMC (Canada) have entered into an arrangement with Tezzaron to offer 3D MPW runs
  - Development and organization of tools is being lead by CPM with support from CMC
  - MOSIS will act as direct interface to Tezzaron, and organize the MPW frame for submission
- In our humble opinion, this would not have occurred if it had not been for the DOE KA12 sponsored HEP program at Fermilab
- The consortium will continue to provide a venue to discuss design issues and compare test results and collaboration in general

Sensor Design

- Sensors need to be developed to be mated to the 3D circuits
  - Will allow for complete testing of technology
    - 3D circuits and bonded devices
    - Integrated devices with interposer
    - Test beam characterization
- Four sensors designed to be fabricated at BNL
  - CMS short strips
  - CMS long strips (not DBI bonded)
  - VIP
  - Imaging sensor



Silicon on Insulator (SOI)

- Investigating SOI as alternative for integration of sensor-electronics and alternative bonding technique
  - Program strongly supported by US-Japan fund
  - SOIPIX Workshop held at Fermilab in March 2010
  - First time outside of Japan

March 30, 2010

FEATURE STORY

Thriving new detector technology: SOIPIX

[Silicon-on-insulator, Pixel Detector]

On March 4-5, 2010, KEK's detector scientists and international collaborators from around the world gathered in a meeting room at Fermilab to discuss a new detector technology: silicon-on-insulator pixel (SOIPIX). Learn about KEK's new technological endeavor, and the recent steps made by collaborators to make this powerful new technology work.

Participants of the 5th SOI collaboration meeting gather in the Wilson Tower at Fermilab for a group photo.

Silicon on Insulator (SOI)

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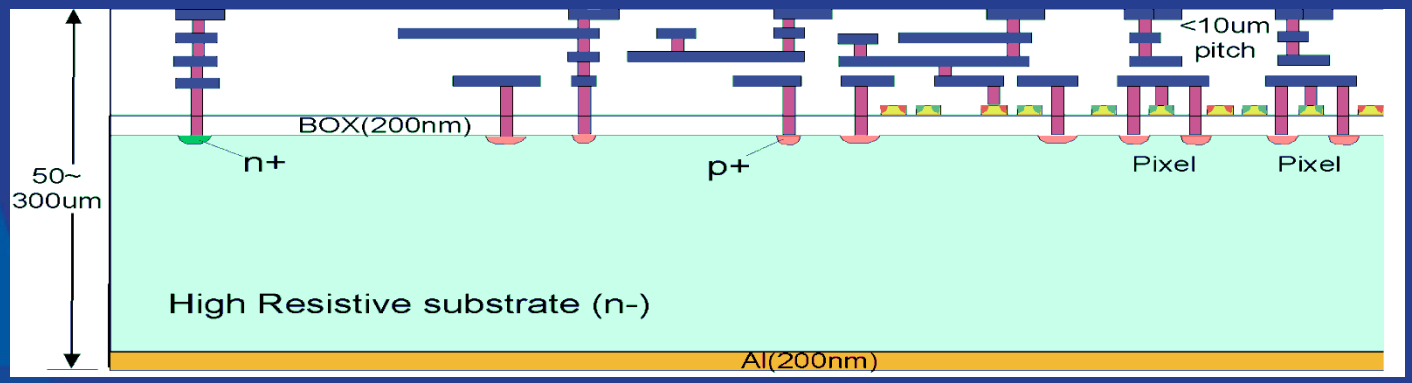
  - Program strongly supported by US-Japan fund
- MAMBO III chip
  - Two tiers in KEK/OKI 200nm SOI process

1st SOI wafer



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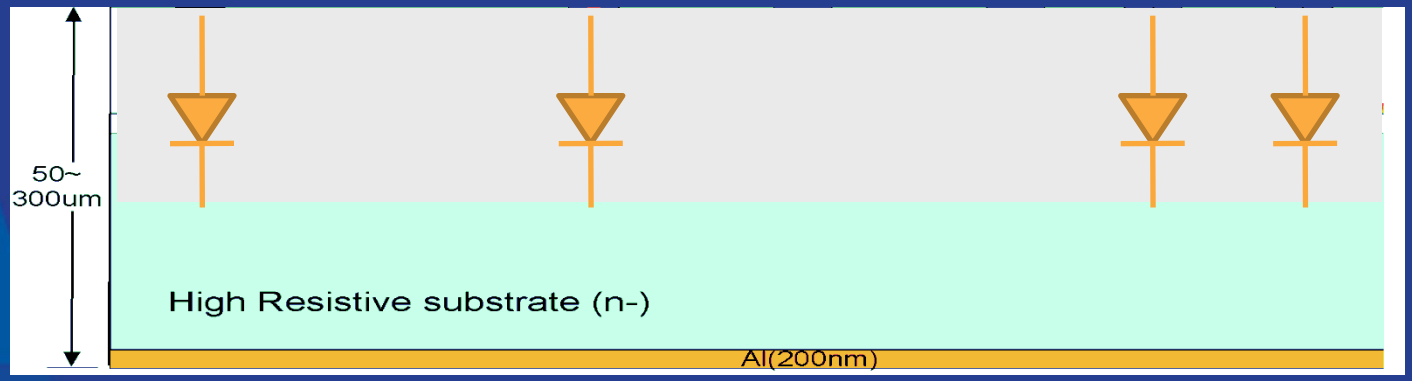

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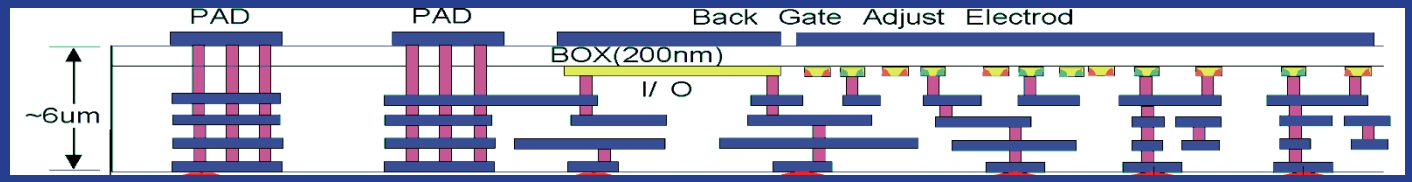

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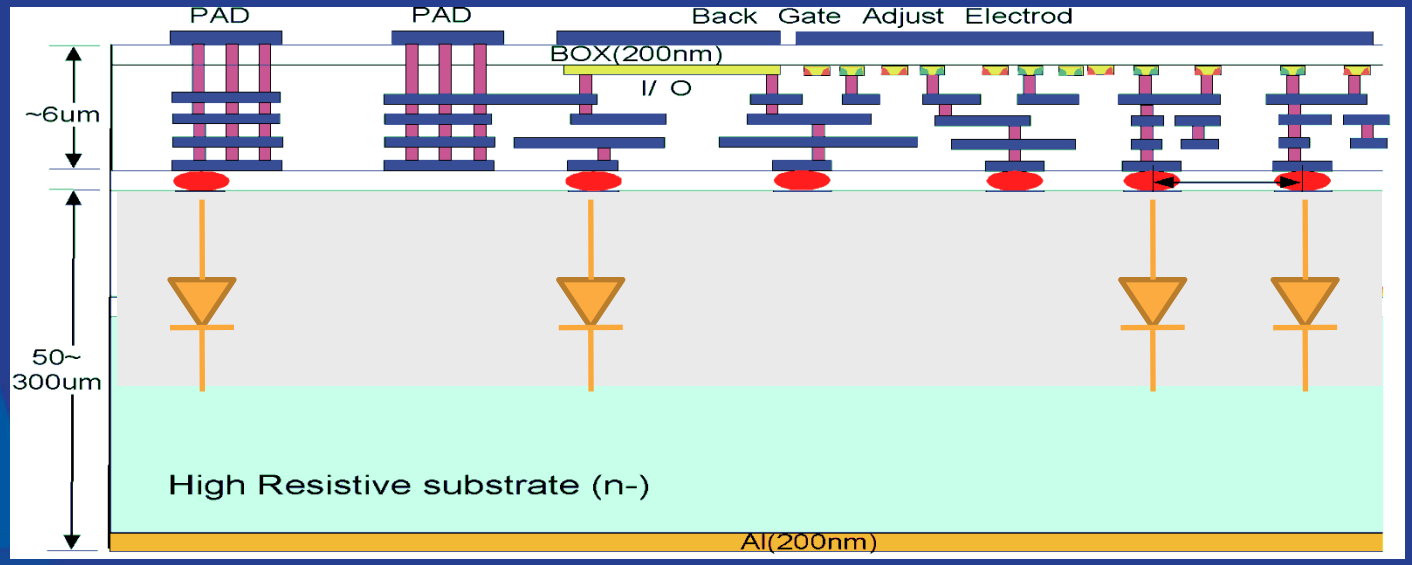
2nd SOI wafer

Micro-bumps

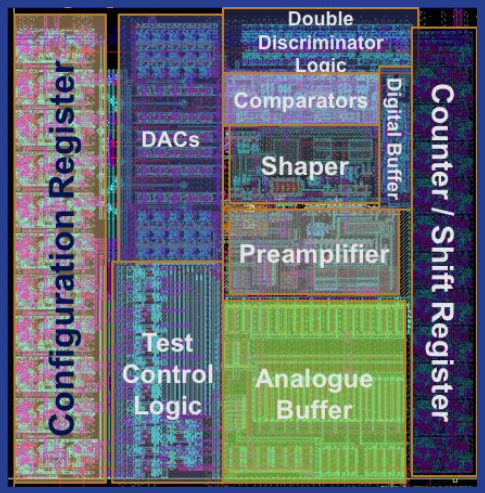
1st SOI wafer

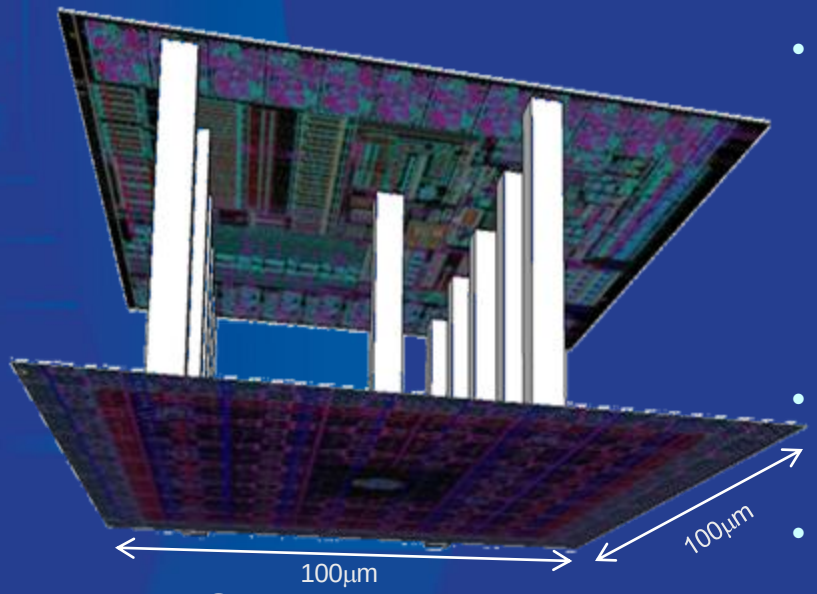


Silicon on Insulator (SOI)

- MAMBO III: pixel counting chip
  - Chip size: 5mm x 5mm
  - 1936 pixel matrix (44x44) of 100x100 um^2 pixels
  - 8-bit DAC, 12 bit counter/shift reg.

MAMBO III : Top chip





MAMBO III

- Bonding done by T-micro (formerly ZyCube)
  - Sponsored by US-Japan funds
  - One bond per pixel, with 10 redundant bonds
- Bottom chip: connections only made through micro bump pads
- Top chip: Pads with back metal opening

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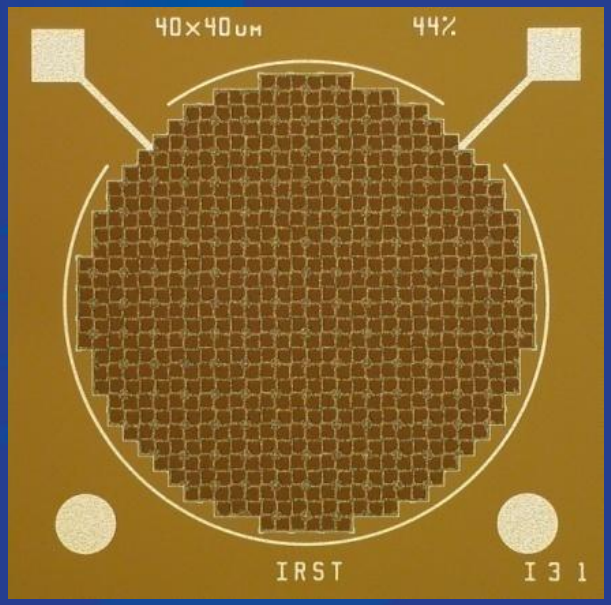
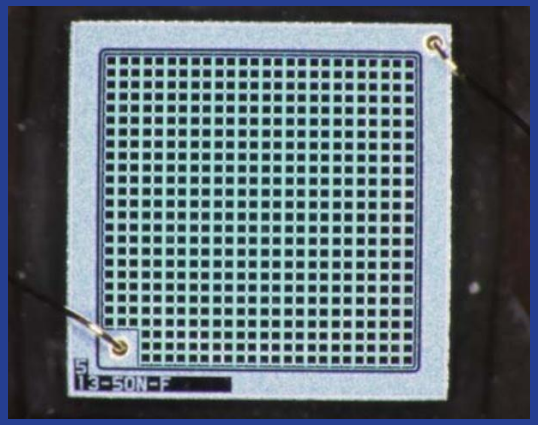
Photo Detectors



Key scientists:
Gene Fisk, Adam Para

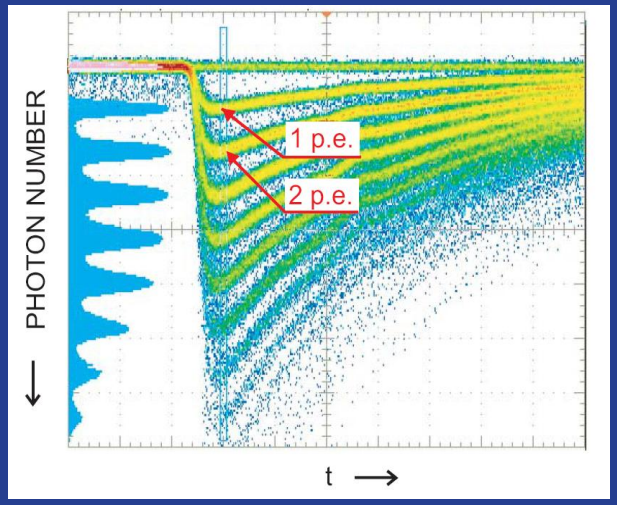
PPD or Silicon Photo-multiplier

- Pixelized Photon Detector (PPD) is avalanche photodiode operating in Geiger-mode
  - Array of pixels connected to a single output
  - Digital device read out in analog way
    - Pixel is either on or off
  - Signal = Sum of all cells fired
  - Devices compact, insensitive to B-field low bias voltage



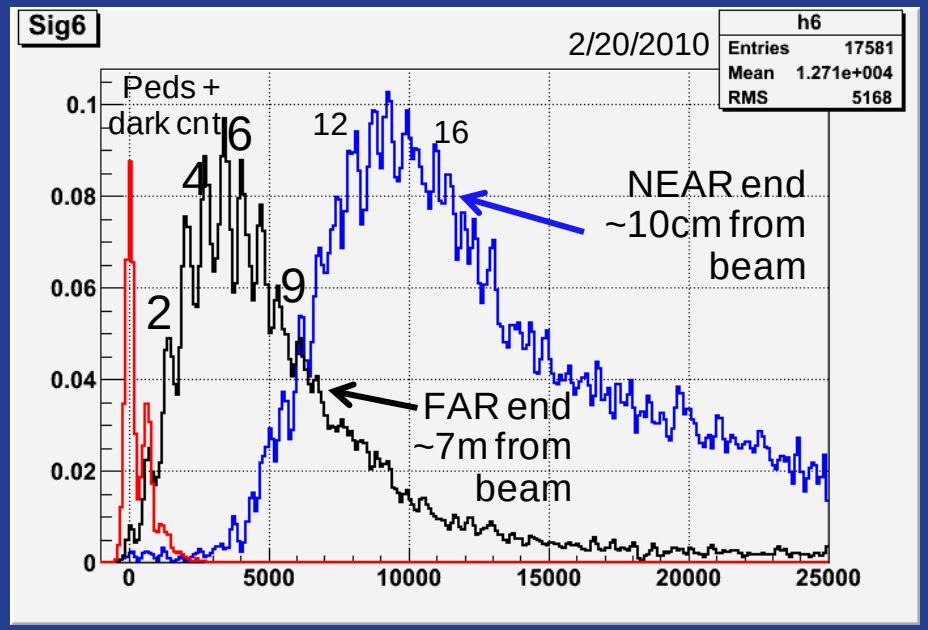
- The availability of PPDs has opened up many avenues that were until now closed

- Developed general facility for characterization of PPDs
  - Dark and photo response



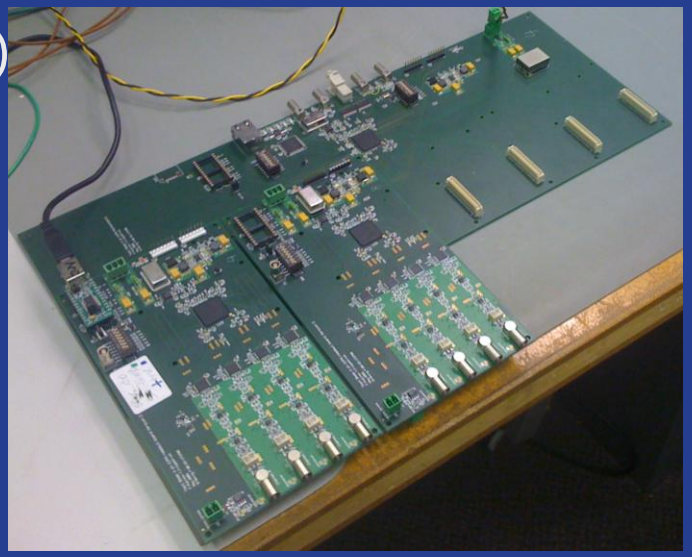
Scintillator Application

- Studied, within the context of the SiD detector, the applicability for muon detector system
- Double strip tested in test beam



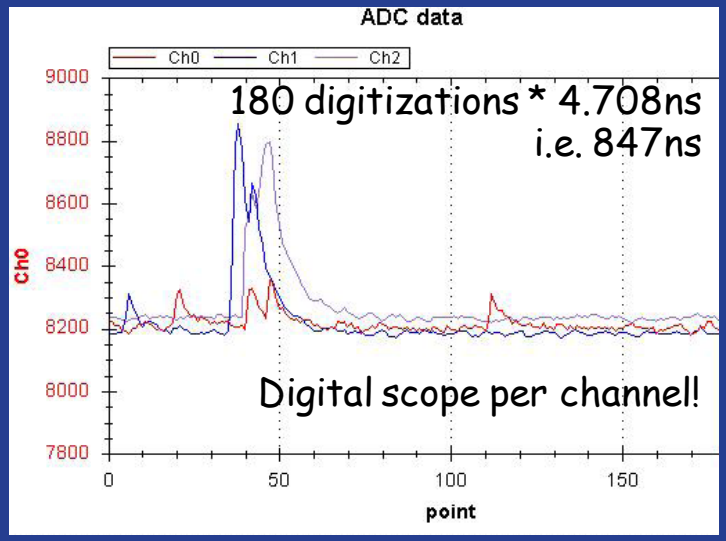
PPD Readout

- Developed TB4 (test beam 4-channel)
  - 12bit ADC (large dynamic range)
  - 212 MSPS (4.7ns)
  - ~100MHz bandwidth
  - Bipolar signals
  - USB setup, readout Ethernet
  - On-board bias generation
  - Allows for online signal processing



- Used by collaborators at Notre Dame, WSU, Munich, Shinshu, …

- Developing plans for dedicated ASIC for PPD readout

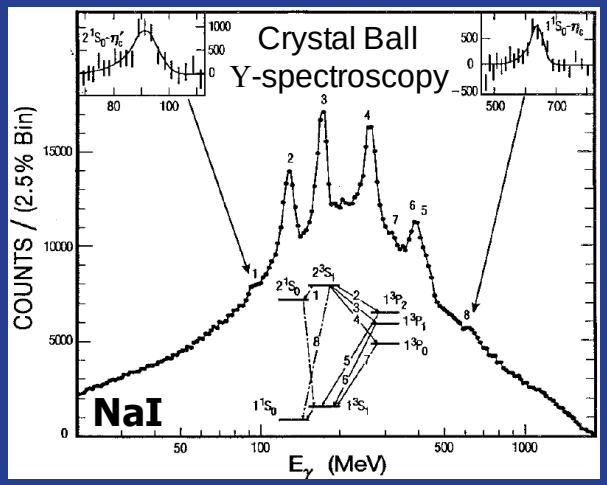


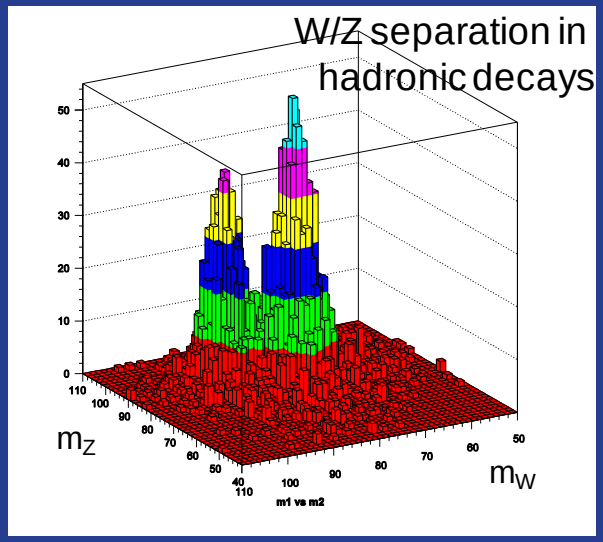
Dual Readout

Key scientists:
Marcel Demarteau, Gene Fisk, Adam Para

Total Absorption Hadron Calorimetry

- Total absorption calorimetry proven to be highly successful for EM calorimeters
- Extend to hadron calorimeters
  - Photo-detectors (SiPM)
  - Dual readout
  - Simulation and beam tests
  - Dense radiators
- International effort exploring material development
  - 3rd workshop at IEEE, Knoxville
  - Collaborative effort with scintillator facility and HEP at LBL





Marcel Demarteau, Steve Derenzo, Auffray Etiennette, Jun Fang, Alexander Gektin, Paul Lecoq, Michele Livan, William Moses, Adam Para, Yifang Wang, Marvin Weber, Tianchi Zhao, Ren-yuan Zhu

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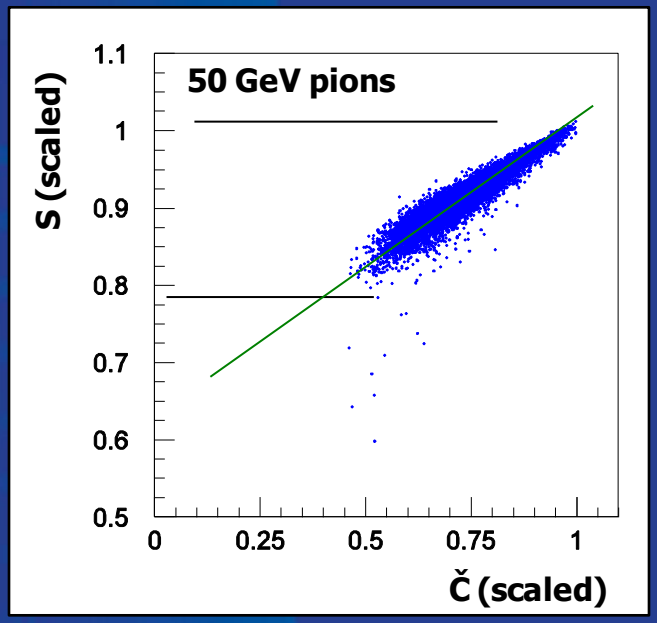
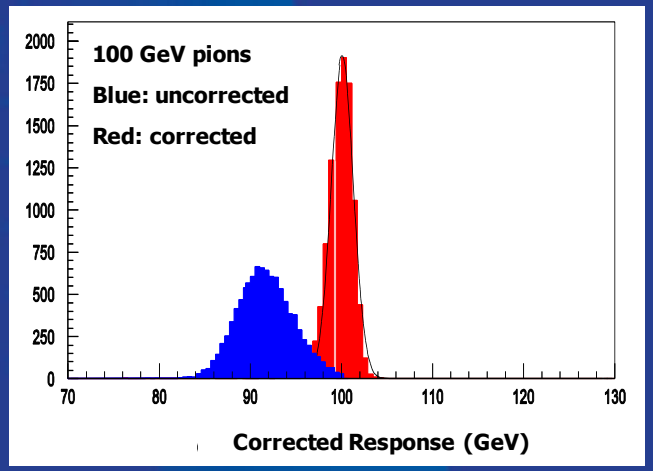
Dual Readout Calorimetry

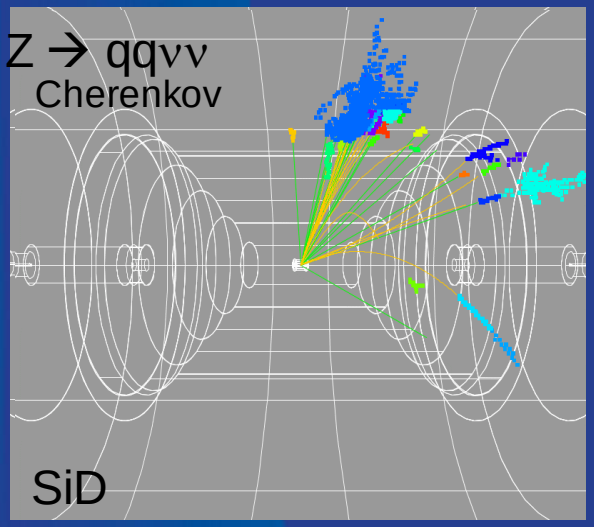


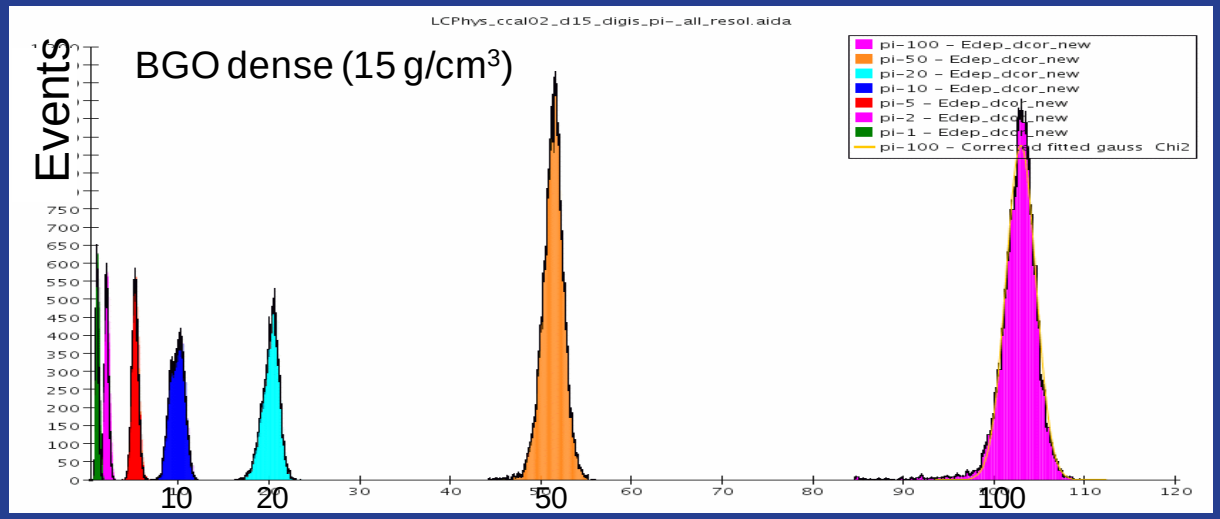


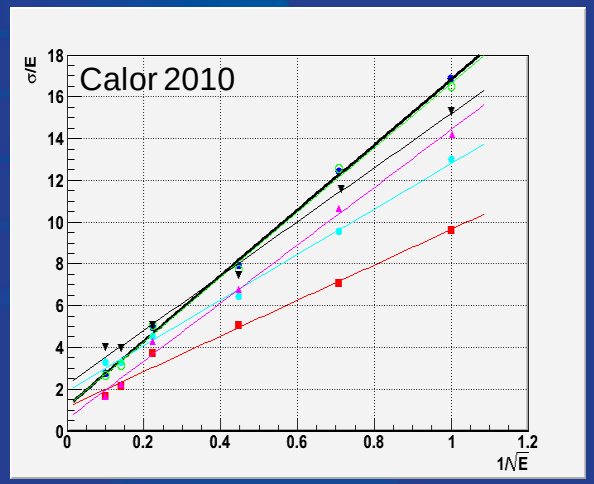
- Dual-readout calorimetry: measure every shower twice
  - Scintillation light: from all charged particles
  - Čerenkov light: β=1 particles, mainly EM
- Correct on a shower-by-shower basis using the correlation of the total observed ionization (S) and Čerenkov (Č) light
- From Monte Carlo studies:
  - Energy resolution (0.1-0.2)/$\sqrt{E}$ (Gaussian)
  - No constant term up to 200 GeV
- The enabling technology is pixelized photon detectors

Simulation

- Implemented crystal calorimeter in SiD detector in slic framework





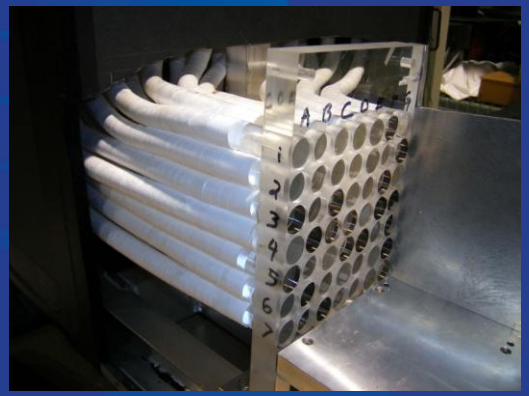


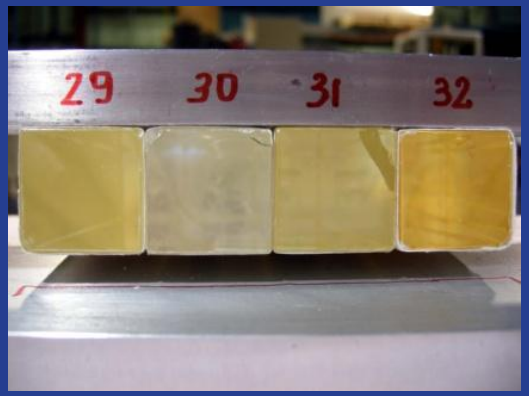
- After scintillation/Cherenkov correction
  - Response linear
  - Energy resolution ~15%/√E
    - Depending on physics model

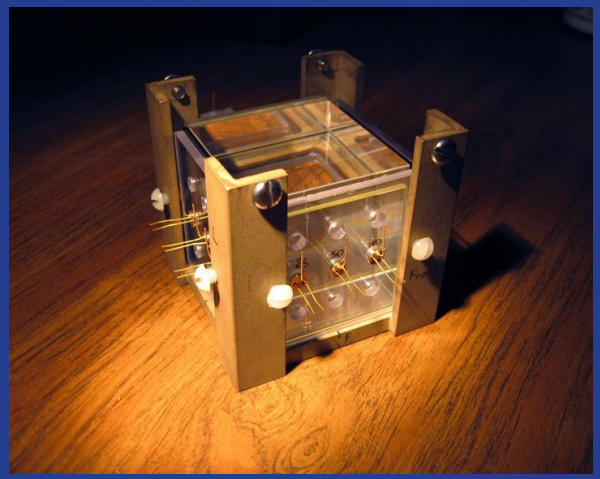
Fermilab

Bench and Beam Tests

- Investigate and characterize crystals and response:
  - Crystals, photodetectors, geometries, surface treatment, filters
  - Separation of Č / S, light collection, uniformity; Č light yield; angular dependence of Č signal.
- Crystal stack
  - $PbWO_4$ crystals (Iowa), former CMS test beam calorimeter
  - 7 x 7 crystal array, tested in test beam T-1004 (Argonne, Cyprus, Caltech, Fermilab, Iowa)
- Single crystal exposure to cosmic rays and beam tests
- Internal review in July

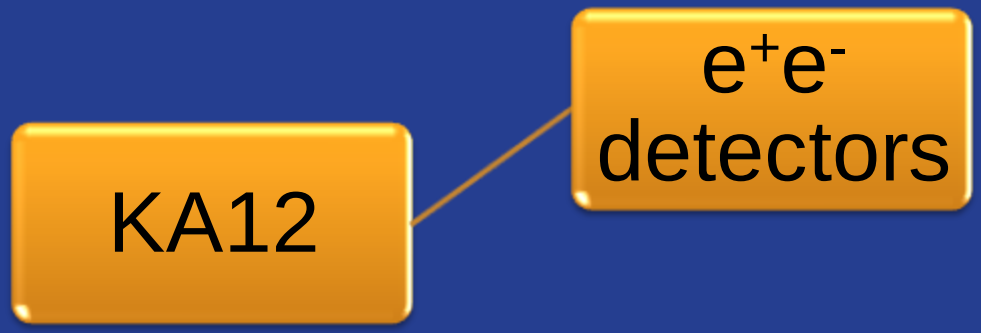






Summary of Activities

- Coherent, successful scientific leadership of a challenging detector R&D program
  - maximizes leverage of each branch
  - Broad reach: vertex detectors, power, scintillator
  - R&D targets key limitations of the current generation of detectors



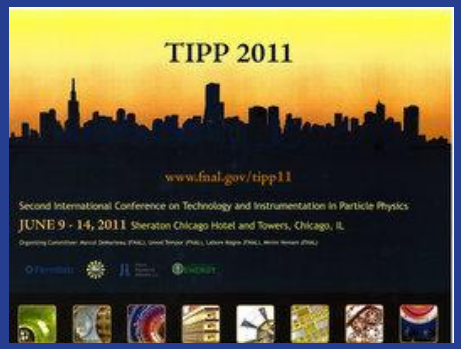
  - If successful, these new technologies could lead to transformational new detectors
- Leadership recognized outside of our own program

Other Activities

- Detector R&D Workshop at Fermilab, Oct. 7-9, 2010
  - Chairs: Chip Brock (MSU), MD

- International Panel to promote Vertically Integrated Silicon technology (VIPS)
  - Junji Haba (KEK), Hans-Günther Moser, Valerio Re, MD
  - Organized successful 1st workshop: VIPS 2010

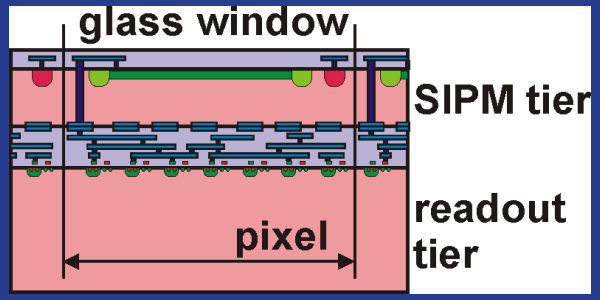
- CERN, KEK, Fermilab Detector school being organized, Jan 31 – Feb 10, 2011 at CERN
  - Advisors: Adam Para, Erik Ramberg, MD



- Fermilab hosting TIPP 2011 workshop, June 9-14, 2011 in Chicago (chair: MD)
- Internationally recognized leadership supported by KA12

Future

- Silicon 3D and SOI devices will be available mid-July.
  - Effort to date had strong engineering component. Need strong scientific effort to test devices
- Next MPW run scheduled for FY11
  - Needs scientific guidance for implementation of different architectures (such as for CLIC, MuC, …)
- The opportunities of our R&D, especially the 3D silicon effort, are immense
  - Explore other areas of applicability and areas of broad societal implications



- Unique opportunity to further develop this truly transform-ational technology initiated by KA12 support

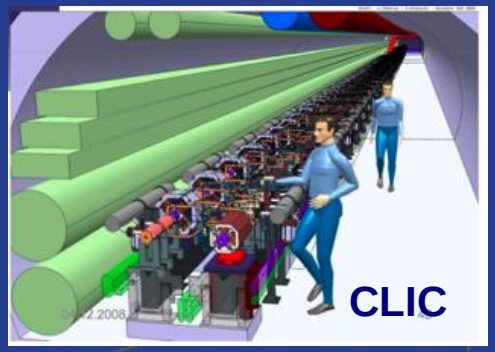
Proposed Funding Profile

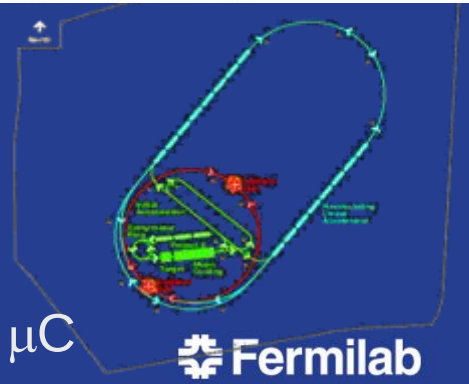
- To retain the momentum and capitalize on the transform-ational opportunities, request support for one more FTE
  - FY10 budget $756k

	2011		2012		2013	
Personnel Support from DOE:	Lepton Collider		Lepton Collider		Lepton Collider	
	No. heads	FTE	No. heads	FTE	No. heads	FTE
Permanent PhD	7	3.10	7	3.10	7	3.10
Temporary PhD	1	0.25	1	0.25	1	0.25
Graduate Students						
Engineer						
Computing Professional						
Technician						
Administrative						
TOTAL	8	3.35	8	3.35	8	3.35
DOE/HEP Funding (per activity):						
SWF (in $, include overhead)		$885,000		$910,000		$930,000
M&S (in $, include overhead)		$64,000		$65,000		$67,000
Travel (in $, include overhead)		$51,000		$52,000		$53,000
TOTAL		**$1,000,000**		**$1,027,000**		**$1,050,000**

Lepton Collider Projects

- Three major future lepton collider projects are being discussed at the moment:
  - ILC: International Linear Collider
    - e^+e^- collider based on SRF technology
    - $\sqrt{s}$ = 500 GeV – 1 TeV
  - CLIC
    - e^+e^- collider based on warm X-band
    - $\sqrt{s}$ = 3 TeV
  - Muon Collider
    - $\sqrt{s}$ = 3 TeV





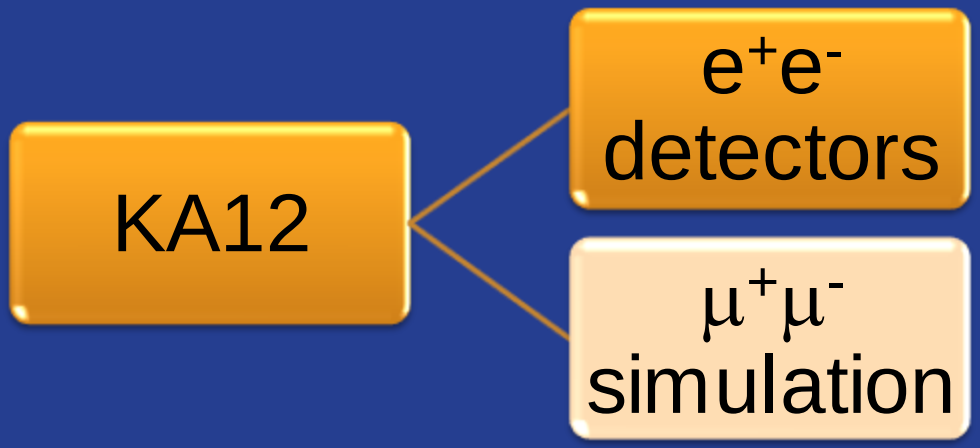
Synergies

- Lepton collider projects are synergistic:
  - The overall physics goals of a future lepton collider are similar for ILC/CLIC/MuC
  - Analysis techniques are essentially the same
  - Some detector technologies are shared
  - Software infrastructure could be common

- Need to develop an objective comparison of the options in terms of physics performance so that the relevant information is available to enable a well-informed choice for a future energy frontier lepton collider

Muon Collider

- A Muon Accelerator Program (MAP) to address the technical challenges and feasibility issues for a future Neutrino Factory and multi-TeV Muon Collider has been submitted to DOE
- This technical program needs to be accompanied by a physics and detector study
- The physics program at a MuC is promising; the challenges are controlling the backgrounds and evaluating their impact on the physics reach



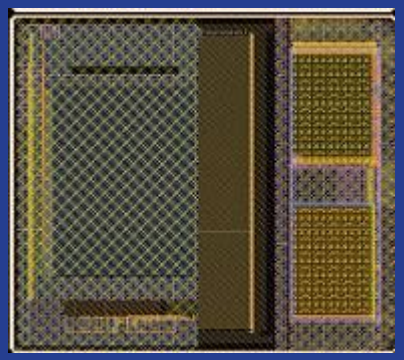
Following Presentations

- Nikolai Mokhov:
  - Background Studies at a Muon Collider (20')
- Marcel Demarteau:
  - Plans and Summary (10')

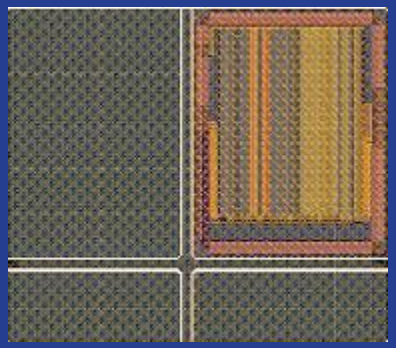
Backup Slides

Sub-Reticules

- Sub-reticule A (Strasbourg, Saclay, Pavia) :
  - FE to be bonded to sensors from XFAB
- Sub-reticule B (CMP, Strasbourg, Saclay):
  - MAPS for ILC
- Sub-reticule C (CPPM, Bonn):
  - ATLAS 2D pixel design (FEI4)
- Sub-reticule D (CPPM, Bonn, LAL)
  - ATLAS 3D pixel design
- Sub-reticule E (Roma, Pavia, Bergamo, Pisa):
  - 3D MAPS
- Sub-reticule F (Pavia, Bergamo):
  - 3D MAPS
- Sub-reticule G Sub-reticule G (Orsay/LBNL)
  - ATLAS Pixel FE
- Sub-reticule H (FNAL/CPPM/LBNL):
  - Vertically Integrated CMS TRigger chip
- Sub-reticule I (FNAL):
  - VIP, adapted to two layers
- Sub-reticule J (FNAL/AGH-UST/BNL):
  - VIPIC: demonstrator for X-ray Photon Correlation Spectroscopy



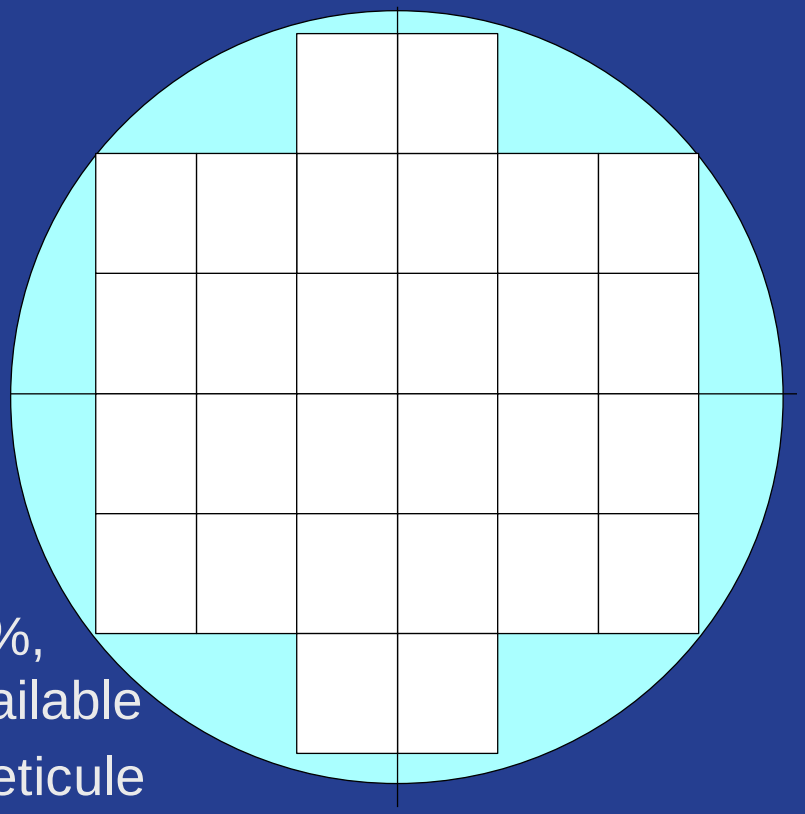
B Right



G Right

Parts Count

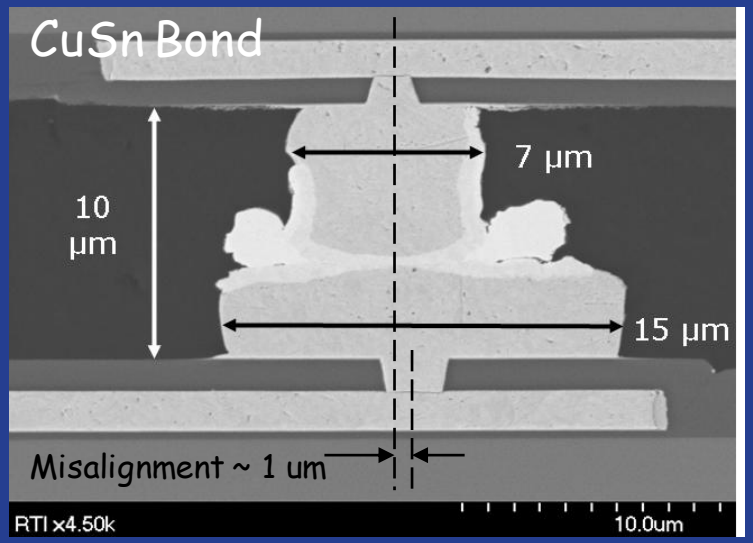
- Procured one lot of 31 wafers, with 28 full reticules per wafer
- Partition of wafers:
  - 3 wafers will be used for 2D wafer testing
  - Available for 3D bonding 28 wafers, which yields 14 3D wafers
- There are 14 3D assemblies per wafer
- If one assumes a yield of 50%, seven working 3D wafers available
- 98 assemblies of each sub-reticule



- A lot of work ahead !

Integrating Detectors

- Ultimate goal is to have integrated unit of front-end and thin (~50μm thick) detectors with very fine pitch (~20μm):
  - How to bond ultra-thin devices?
  - How to bond at very fine pitch?



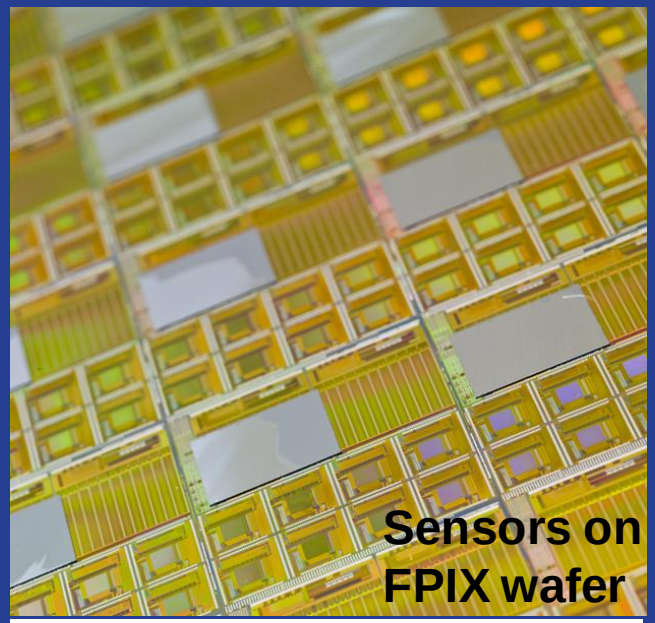
- Study I: developed with RTI (NC) bump bonding process at 20 μm pitch
  - CuSn bonded to Cu; good yield
  - SnPb bonded to Ni/Au
  - Demonstrated the feasibility of CuSn bonding for fine pitch (20 μm) assembly of 3D circuits (ignoring mass budget requirements)

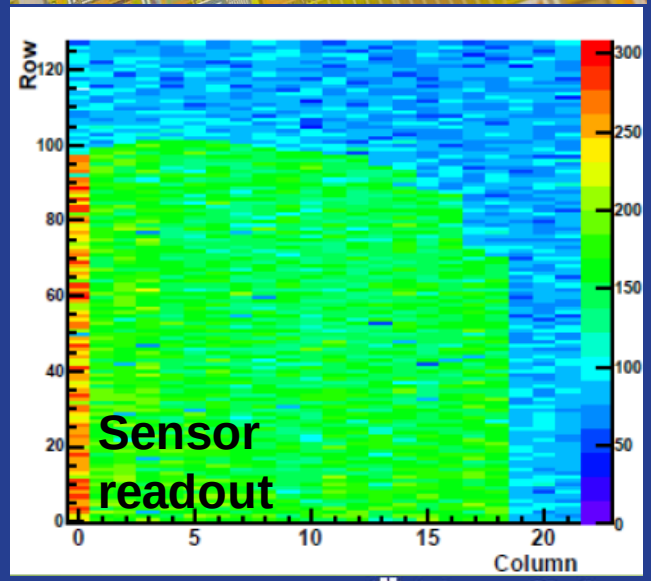
- Study II: developed with Ziptronix (NC) Direct Bond Interconnect (DBI) process, that provides greater flexibility and constitutes much lower mass

Integrating Detectors

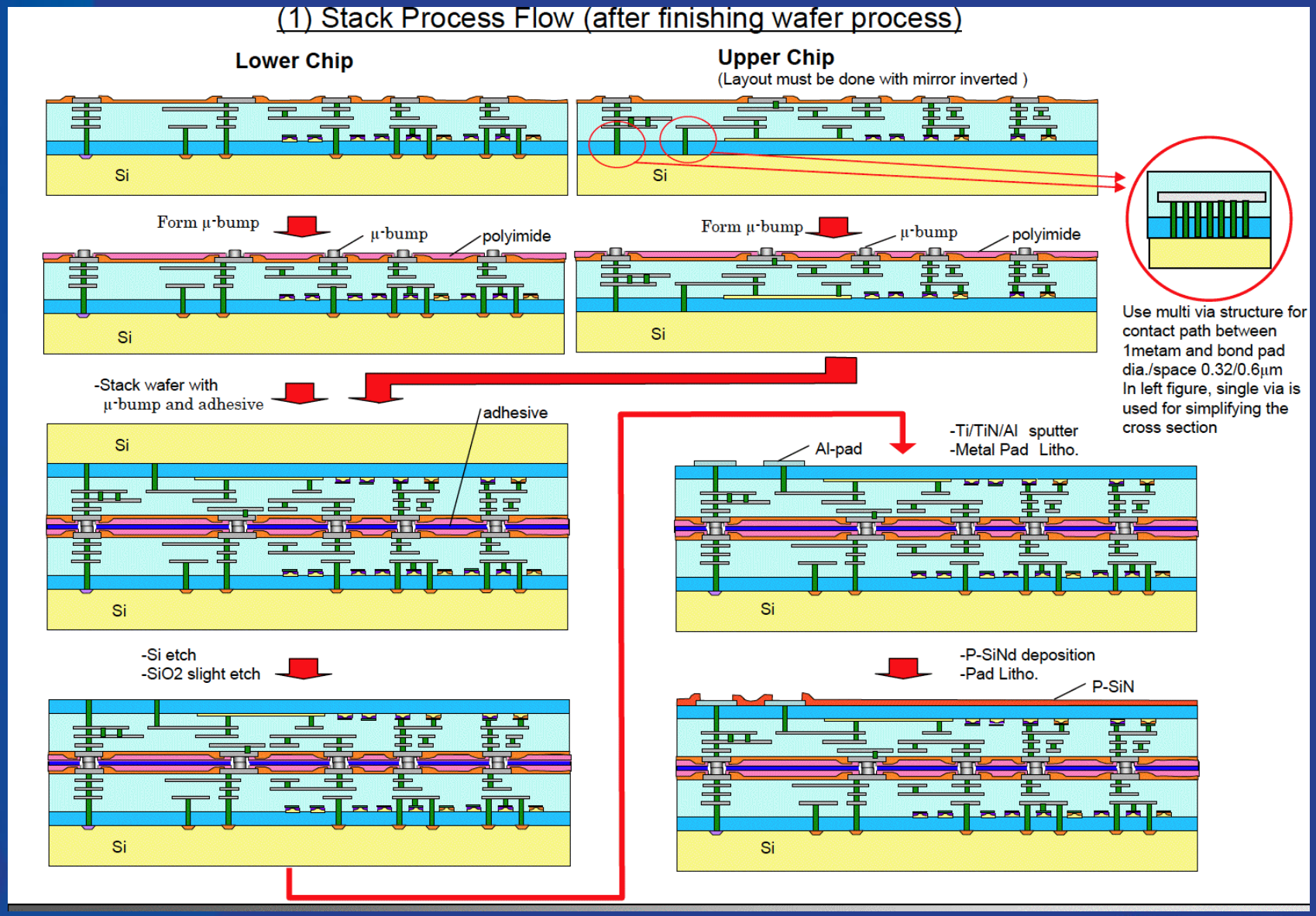
- DBI bonded BTeV FPIX2.1 readout chips to pixel sensors
  - 22x128 pixel cells of 50x400μm^2;
  - Edgeless trenched pixel sensors
  - 50 μm deep n^{++} trench at the edge
  - Masks designed at Fermilab
  - Fabricated by MIT-Lincoln Lab

- Above two items DBI bonded at Ziptronix; after bonding sensors thinned to 100 μm (can go as low as 50μm)
  - Very strong bond with good yield
  - Devices have full readout; issues understood
  - Method valid for pitch down to ~ 5 μm





T-Micro 3D Process



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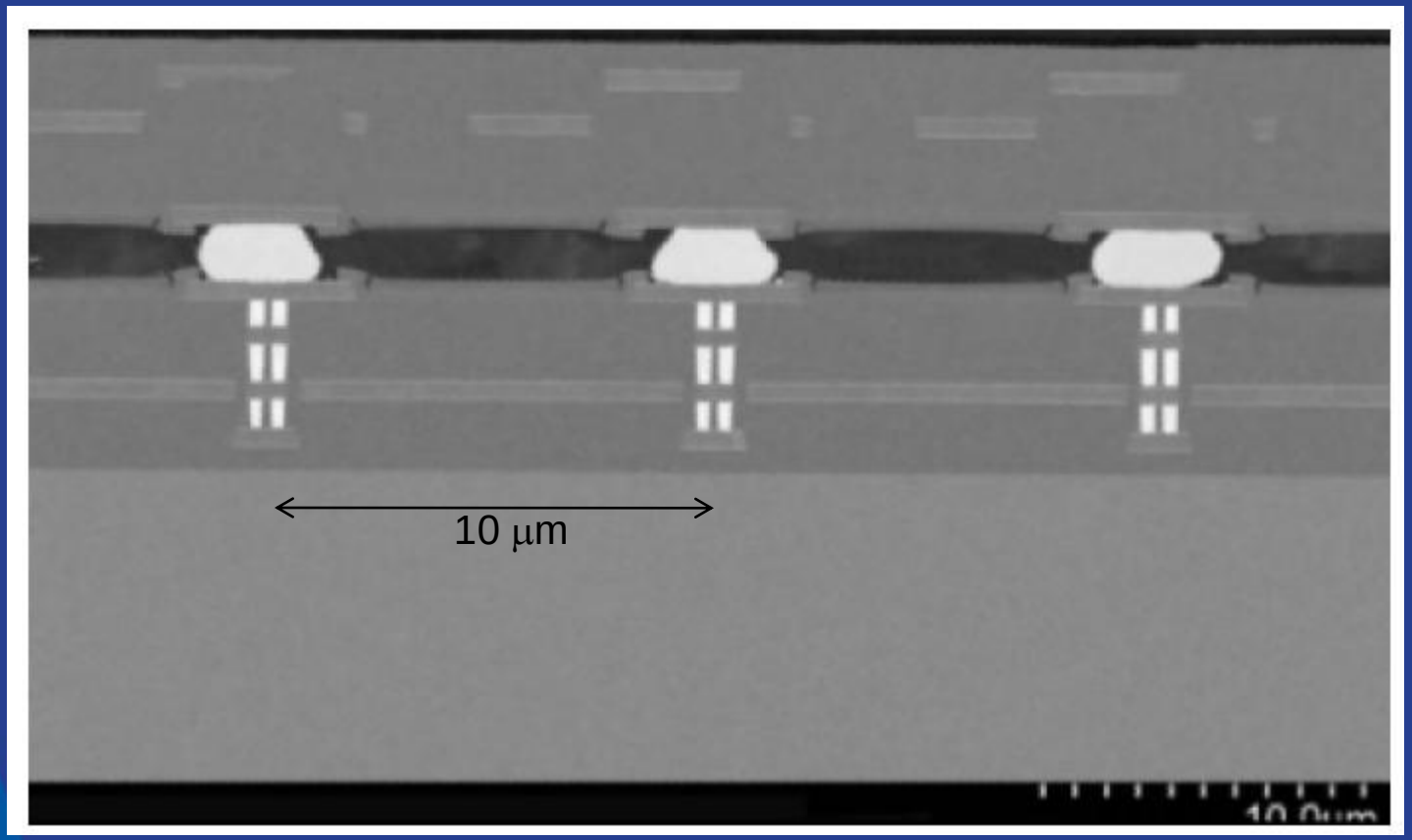
T-Micro Prototype



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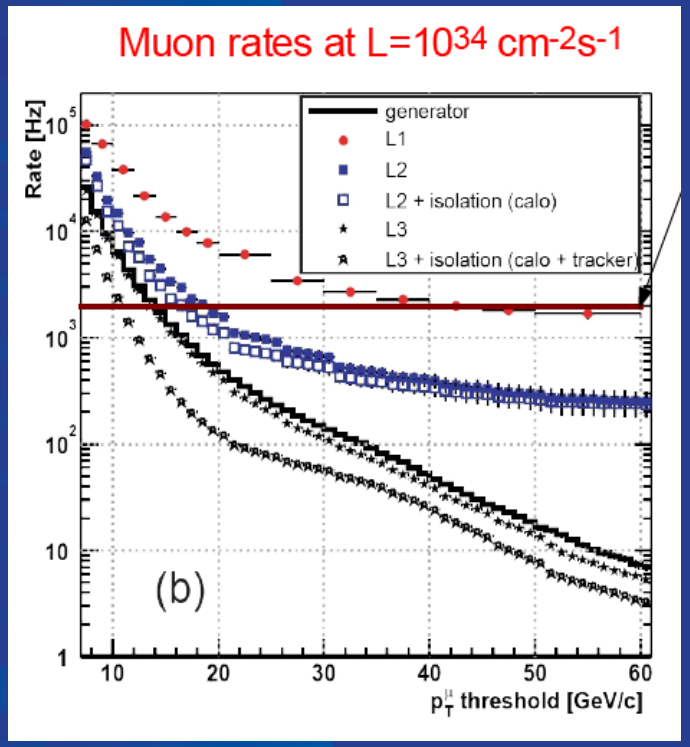
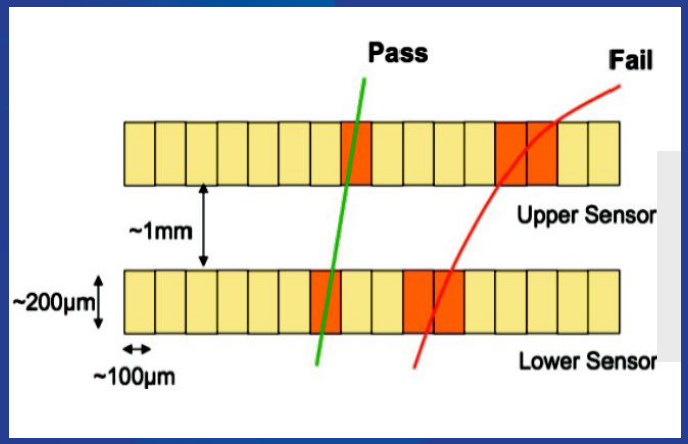
Fermilab 3D Project: VICTR

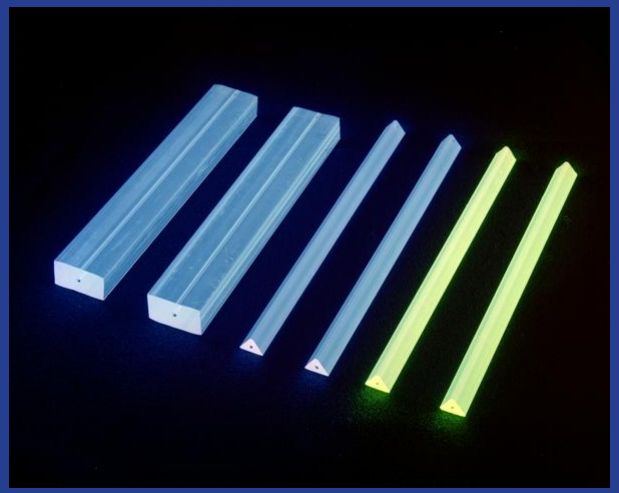




- Vertical Integrated CMS TRigger chip
  - R&D project to study viability of the 3D technology for sLHC experiments
- The problem: at the sLHC triggers saturate the available bandwidth
  - Muon trigger rate at L1 > 20 kHz at $L=10^{35}\ cm^{-2}s^{-1}$, flat in p_T
- A solution: tracking information available at L1
  - Collect info from 10^8 pixels in $200m^2$ of silicon at 40 MHz
  - Power and bandwidth to send all of the data off-detector is prohibitive
- An implementation: stacked modules that provide a momentum filter

Scintillator R&D

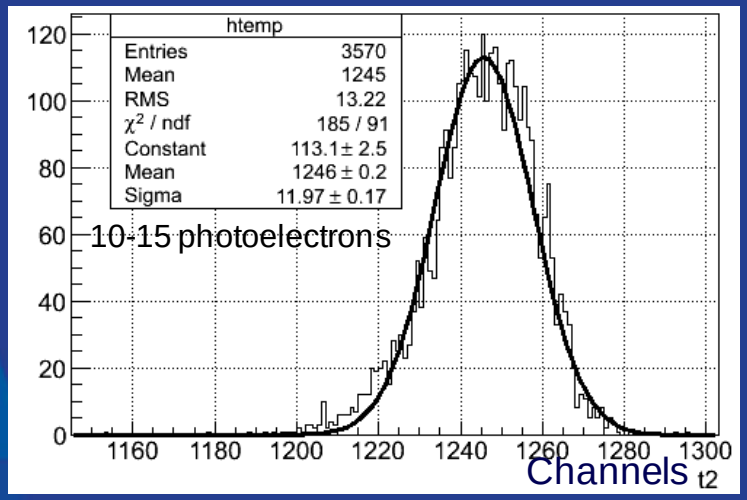
- Scintillators have wide applicability and will continue to play a critical role as detector particle physics
  - Low cost, large area experiments
  - Veto walls (e.g. dark matter experiments)
- R&D centers around the following strategic areas:
  - Development of the scintillator/fiber co-extrusion
  - Preparation of high Z and neutron-sensitive extruded plastic scintillator
    - Initial studies on BaF_2
  - Investigation of the use of an environmentally-friendly solvent for liquid scintillator applications
    - Initial studies on Titanium dioxide

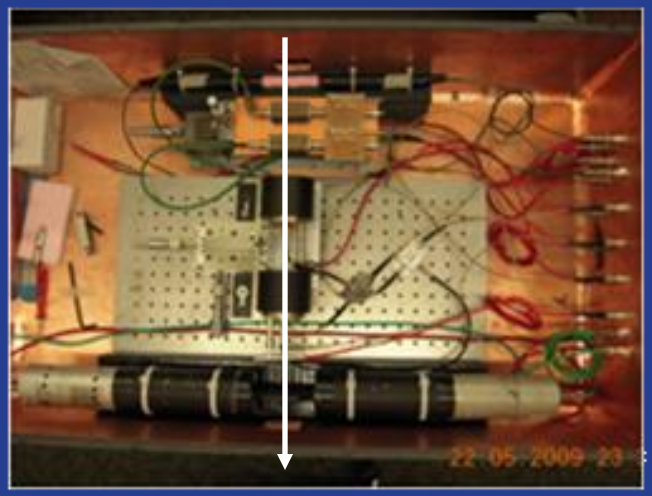


Key people:
Alan Bross, Anna Pla-Dalmau

Spin-off: TOF at Test Beam

- Determination of timing resolution with Silicon Photomultipliers (SiPM) and quartz bars
  - Eight Hamamatsu SiPMs, 3mm x 3mm
  - In beam with quartz Cherenkov radiators
  - several thicknesses (4 – 12mm), mirrored and not mirrored.
- Under best conditions: σ(t) ~ 33 – 37 ps

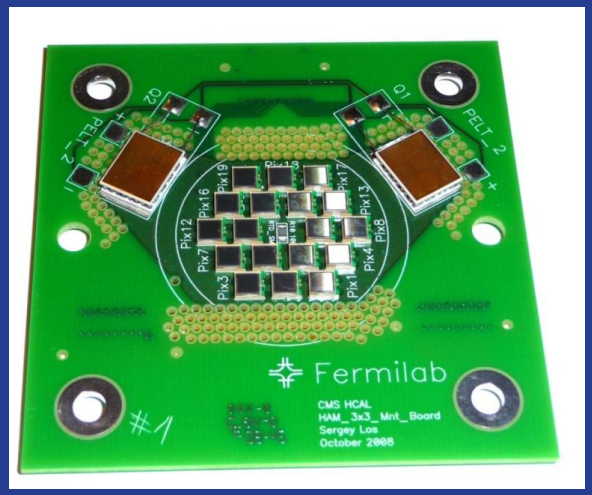




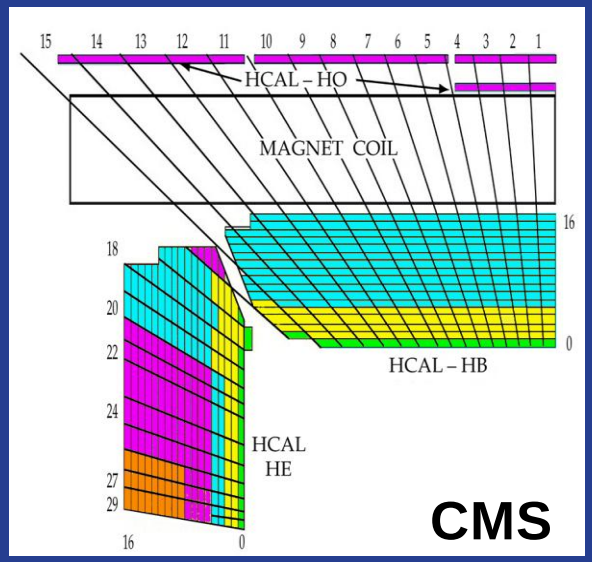
Pulse height slewing correction applied

SiPM CMS Synergy: HCAL

- CMS HPD replacement step 1: Outer Calorimeter (~2011)
  - ~3,000 PPDs
  - Each fiber in bundle (18) guided to its own SiPM
  - Readout by QIE ASIC (Fermilab)

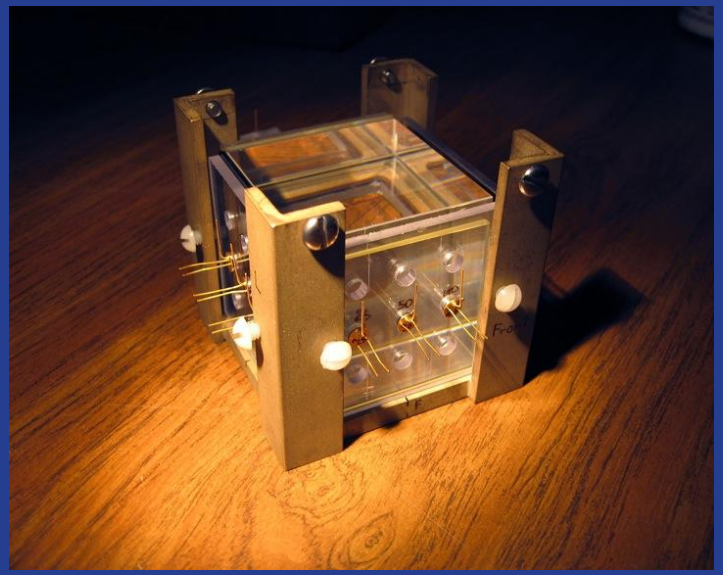


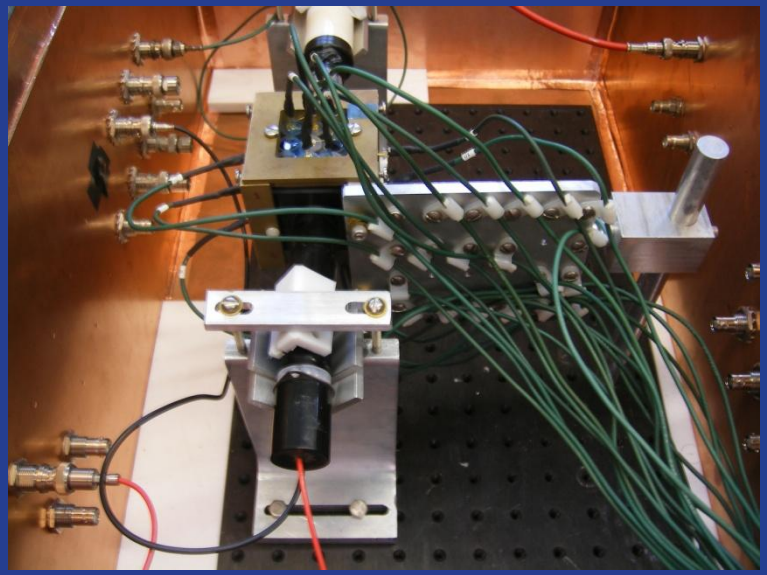
- CMS HPD replacement step 2: Whole calorimeter (Phase I)
  - ~110,000 PPDs
  - Allows for longitudinal segmentation
  - SIPM tailored to HCAL
  - New ADC = new ASIC (QIE10)



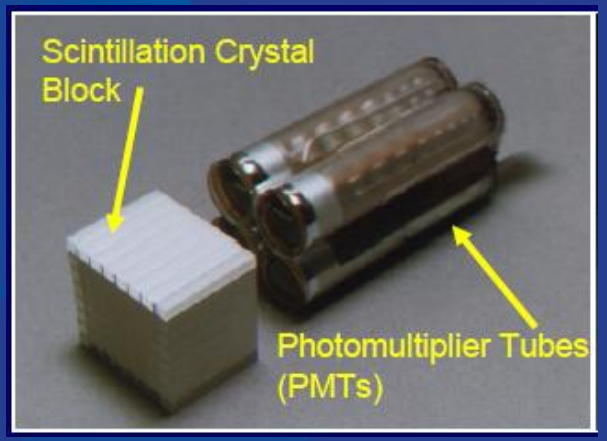
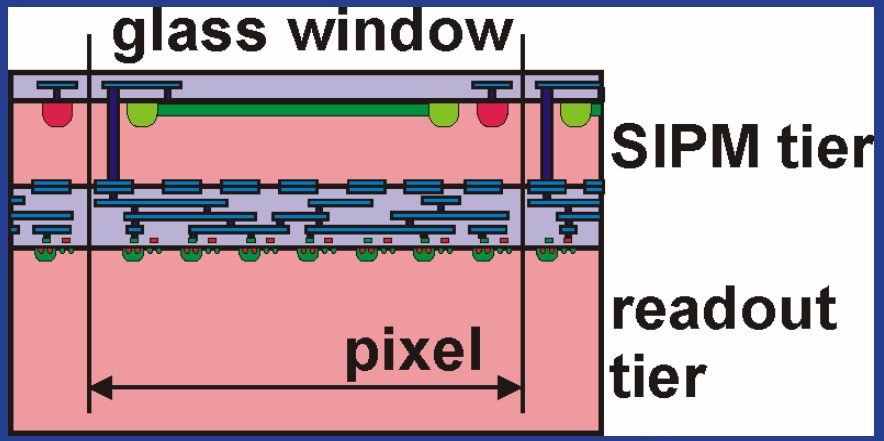
- Strong overlaps

Single Crystal Setup





- BGO crystal (from Caltech)
- Visible and UV filters
- Two PMT's
- 20 Hamamatsu SiPM's
- TB4 readout boards

An Aside: PET

- Two University of Chicago – Fermilab seed grant proposal submitted ($100k/yr for 2 years) for PET
- PET: Crystals + PMT
- Proposal to develop front-illuminated SiPM with through-silicon-vias (diameter <2μm) to connect to 3D circuit with back-to-front bonding
  - Allows for individual pixel control and much more functionality