MicroBooNE Detector, Digitization at Feed Through

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Abstract

The MicroBooNE detector project is set to benefit from a subtle change in its digitization design. Digitization can be implemented at feed through instead of over 20 meters away from the signal source. We have a designed card with capability of digitizing signals at feed through. The card has added features which include a high time resolution (up to 50ps LSB) and an efficient noise handling. The card is compatible with the detectors; the card is designed to fit the slots available at feed through. The digitization scheme used is a TDC implemented on an FPGA. Dedicated carry lines of an FPGA are used as delay cells to perform time interpolation within the system clock period and to realize the fine time measurement. Two Gray-code counters, working on in-phase and out-of-phase system clocks respectively, are designed to get the stable value of the coarse time measurement. The fine time code and the coarse time counter value, along with the channel identifier, are then written into a first-in first-out (FIFO) buffer. Tests have been done to verify the performance of the TDC. This paper explains the TDC card design and the details the performance test carried on the card.

Introduction

The Fermi Lab Research facility is mainly involved in high energy particle physics research. Particles studied here include neutrinos, Higgs and proton/anti proton. Several divisions work together to successfully run the Lab, some of which include: Accelerator Division, Business Services Section, CMS Center, Computing Division, ES&H, Finance Section, Particle Physics Division. Collaboration between these divisions has yielded success stories like the D-Zero experiment which is focused on precise studies of interactions of protons and antiprotons at the highest available energies. It involves an intense search for subatomic clues that reveal the character of the building blocks of the universe.

I am researching with the electronic section of the Particle Physics Division. My group is working on the MicroBooNE detector. This is a large detector (>100kton) and it detects neutrino events through observation of signals from outgoing charged particles. The MicroBooNE detector is a product of the MicroBooNE experiment and is still undergoing developments. My group is developing enhancements on the data acquisition component of the detector.

A data signal from the detector currently goes through a grandiose circuitry involving multiple amplifications, shaping, digitization and interpretation. With the current path, noise and interference and other factors have well reduced the efficiency of the detector. We believe that suitable changes and circuit simplifications can be made in the detector to optimize its function.

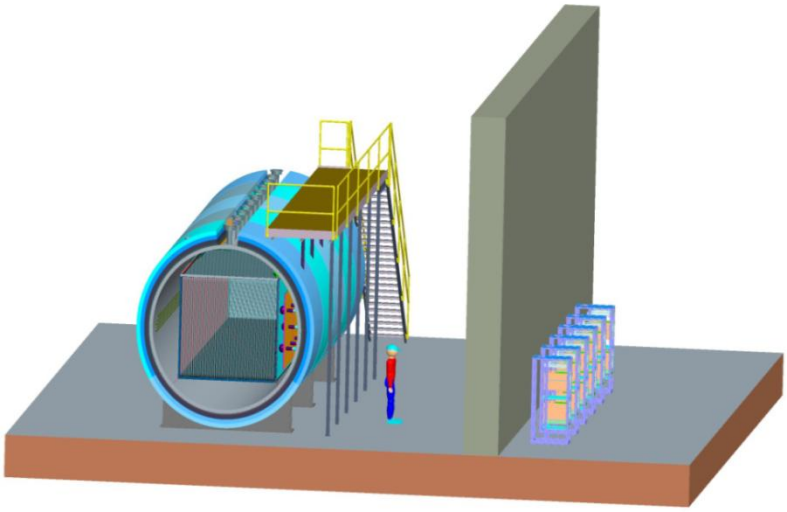
I spent better time working on the digitization of signals. The plan is to replace the Analog to Digital Converter (ADC) chip with a novel Time to Digital Converter (TDC) implemented on an FPGA chip. This feature is added to the data conversion card that is currently under development. We also studied the data conversion card's performance and sought ways to enhance its operation in the detector.

MicroBooNE Project

The MicroBooNE project employs a Liquid Argon Time Projection Chamber (LArTPC) R&D which has an amazing technology for future neutrino physics research. The device is designed to reconstructs particle interaction with their identification in incredibly high precision.

General Description

- 150 tons total Liquid Argon
- 89 tons active volume
- TPC: ~2.5 x 2.3 x 10.4m long
- Ionization electrons drift to beam right
- 30 PMTs peek through the wire chambers on beam right
- Will use BNB and NuMI beams at FNAL for physics program



Pic 1: MiniBooNE Detector Model

Project goals:

- Resolving the source of the MiniBooNE low energy excess by employing precision electron/photon differentiation offered by LArTPC's;
- Measuring exclusive cross sections on argon in the 1 GeV range by exploiting high resolution of event topology available from LArTPC's;
- Exploring technological innovations and methods to provide a basis for the design of the next generation of LArTPC detectors at larger scales. [reff]

MicroBooNE has a 70 ton fiducial volume (170 ton total volume) of Liquid Argon Time Projection Chamber (LArTPC). The high purity liquid argon serves as the neutrino target and tracking medium for the particles produced in the interaction. The TPC active volume is 2.3m x 2.6m x 10.4m.

MicroBooNE detects neutrino events through observation of signals from outgoing charged particles in the interaction. Electrons are ionized by the passage of these charged particles through the liquid argon and transported by a uniform electric field to three wire planes on the beam right side of the detector. The electric potentials of the three wire planes are arranged so that the electrons pass through the first two (induction) planes and are collected on the third (collection) plane (fig. 2). The induced and direct electrical signals on each wire are amplified and sampled at 2 MHz by an analog to digital converter. The wire pitch is 3mm; therefore position resolutions are on the millimeter scale. The trajectory of particles in the detector is reconstructed from the known wire positions and the arrival times of electron signals on the wires combined with the time the interaction took place in the detector – in the 1.6 microsecond beam spill. The amplitude of the ionization electron signals measures the energy loss of the particles which allows an estimate of their momentum and particle type.

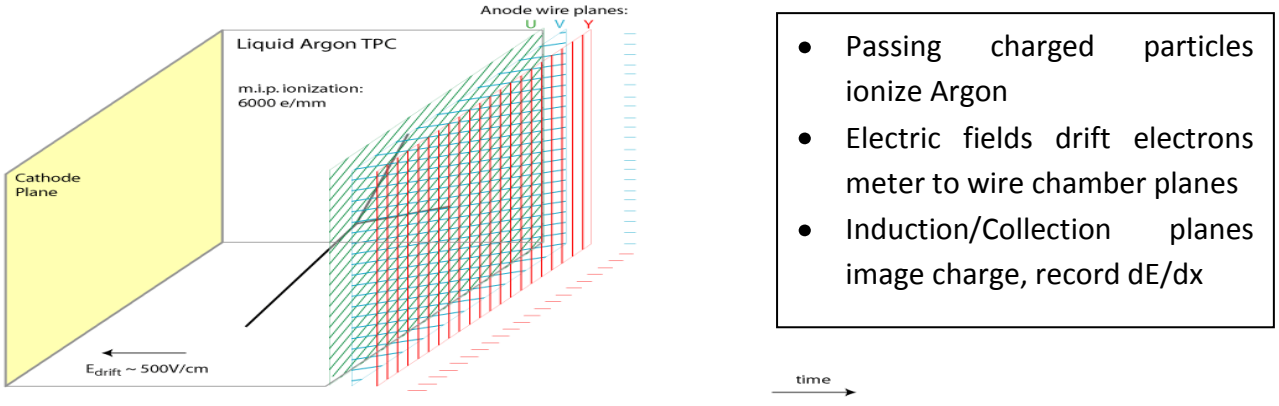


Fig. 2: Detector Mechanism

Data Acquisition

Data from the detector is fed to an analyzing system for interpretation and control of the detector. This entire process of conveying information for the detector to the analyzing device is called "data acquisition". The Data acquisition plan adopted is inarguably crucial to the performance of the detector; hence there is a need to implement the most efficient Data acquisition scheme.

The detector design supports readout for approximately 10k channels. The readout channels are distributed on two induction planes (i.e. U, V planes) with wires running at +/- 60° with respect to the beam direction (z-axis) and one collection plane (Y-plane) with wires running perpendicular to the beam. Fig 3 shows a single readout channel information flow.

This readout scheme has several short falls including:

- Noise interference to signal
- Inefficient long analog signal cable run

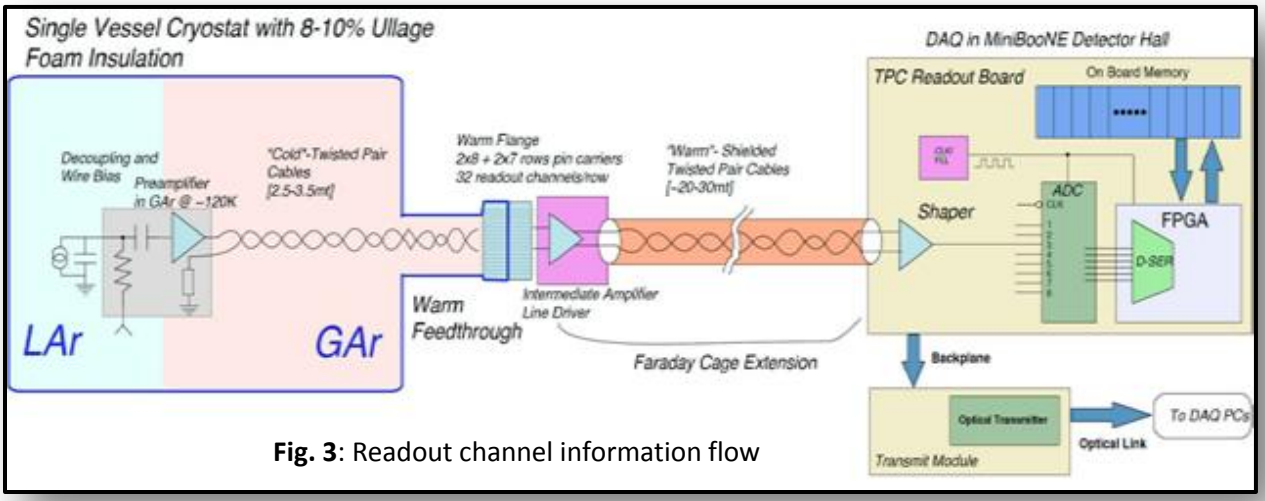


Fig. 3: Readout channel information flow

Source: MicroBooNE Conceptual Design Report , Feb 2010

To tackle this problem, we are proposing implementing a "Digitization at Feed through" scheme. This will allow digital data to be sent over a long distance, thereby cutting out noise interference and allowing an efficient cable run. The possible problems with our implementation are power and compatibility with the current card slot. The illustration diagrams below better explains our design.

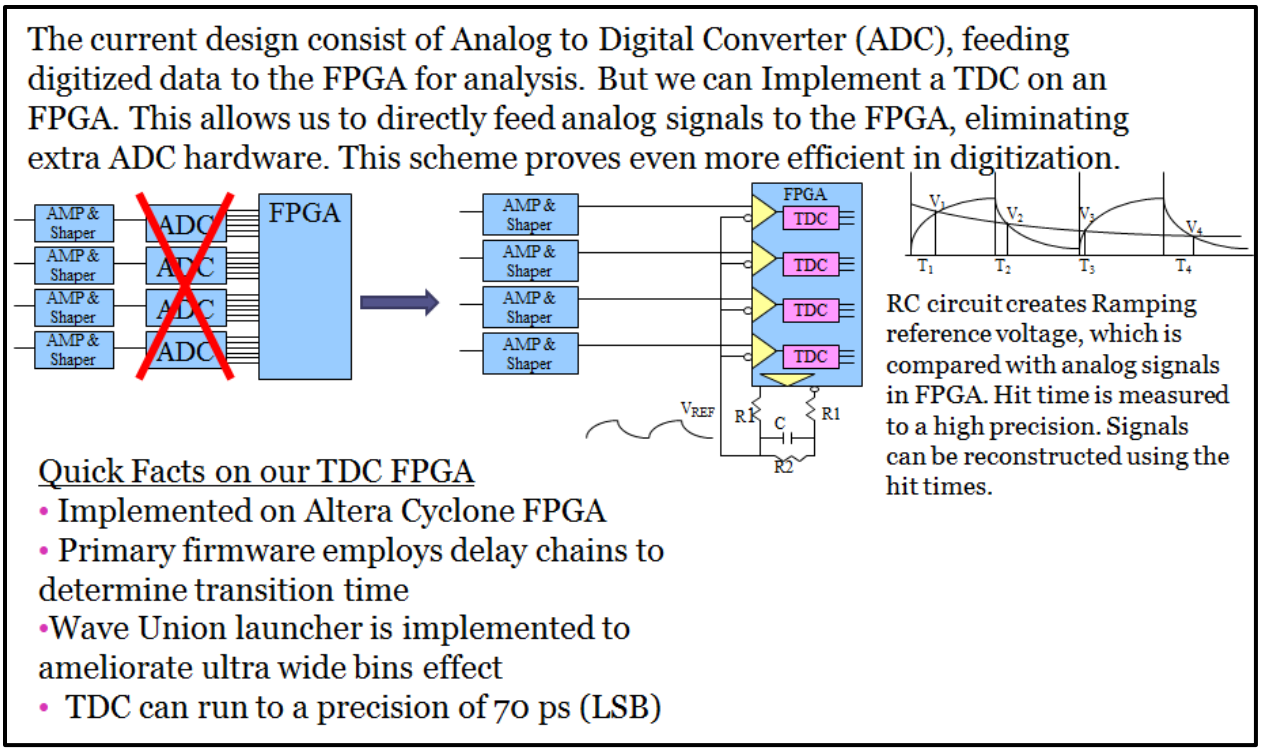


Fig. 4: Single Slope TDC

ADC or TDC on an FPGA?

A change from the conventional Analog to Digital Converter (ADC) to FPGA signal path is made to a more efficient Time to Digital Converter (TDC) which will be implemented in an FPGA. FPGA is characteristically a digital device, but with suitable circuitry, it can be implemented to digitize multi-channel analog waveforms. The digitized waveforms can then be directly processed in the FPGA. There are several possible schemes of digitizing analog signals.

One of the schemes we used in our FPGA TDC study is based on the ramping-comparing approach.

In today's FPGA devices, differential input buffers are good comparators within a sufficiently large range of input voltage levels, since they are designed to be compatible with various differential signaling standards. Comparator-based ADC schemes can be implemented with FPGA.

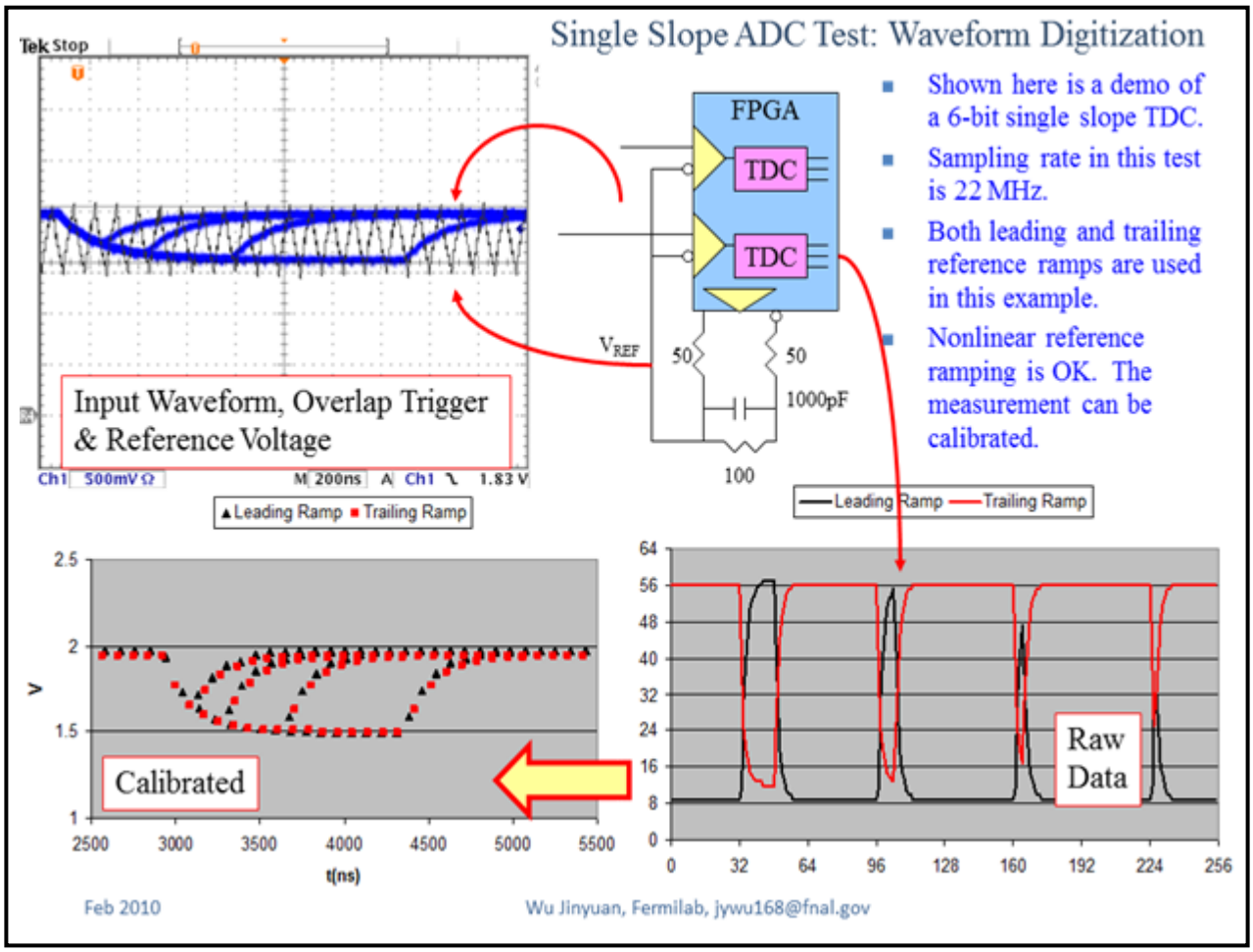


Fig. 5: TDC Scheme

In our design, the analog inputs are directly connected to the FPGA input pins. A passive RC network is connected to the FPGA output pins so that a periodic reference voltage ramp can

be generated. The differential input buffers are used as comparators to generate logic transitions inside the FPGA when the reference voltage ramps across the input voltage levels. The transition times are digitized by the TDC block implemented in the FPGA. Since the period, the RC network parameters, and the starting time of the ramps are known, then the input voltage levels can be derived from the transition times. (In some references, the single-slope scheme is mistakenly referred as Wilkinson ADC that is based on dual-slope principle.)

The illustration in Fig. 4 above summarizes the scheme.

Time Counting Architecture

The primary component of the TDC is the array of buffers that delay hit time recorded in the comparators. The transition times are latched by registers into an encoder which records the time. A simplified firmware diagram describes this.

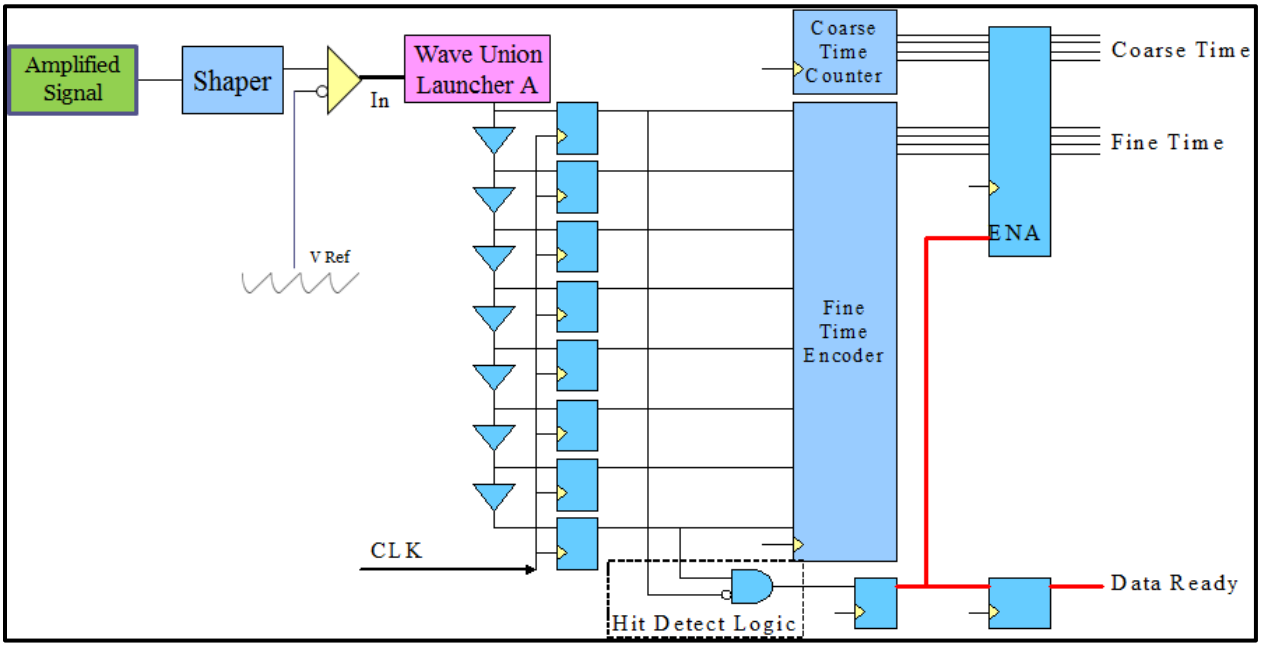


Fig. 6: TDC FPGA architecture

The architecture of FPGA TDC causes the delay of the HIT and the CLK is used as the register array clock. In FPGA TDC, the coarse time counter is a plain binary counter and is implemented as shown in Fig. 6.

The input hit is recorded in the register array and the location of the wave union is encoded as fine time. Note that the uncertainty of the relative timing between the hit and the CLK is confined in the register array which is the value to be measured by the TDC. All other signals are derived from the output of the register array and their timing is well-defined by the CLK and they are staged into the process pipeline.

While the fine time is being encoded, a hit valid signal is being generated by the hit detect logic. The simplest hit detect logic senses the logic level difference between both ends of the register array so that a hit valid signal is generated for the clock cycle when wave union is inside the array. This hit valid signal, eventually being derived as the data ready signal, is used to enable latching of the coarse time. The setup and hold time are guaranteed since both the coarse time counter and the register are drive by the same clock signal CLK.

Wave Union

We used the carry chain structure of the Altera Cyclone FPGA to implement the Time to Digital Converter (TDC). Due to imperfections in the individual components of the carry chain, an unequal delay of HIT time will be observed. This phenomenon in the FPGA TDC is defined as

large differential nonlinearity (DNL). The plot in Fig. 7 explains this.

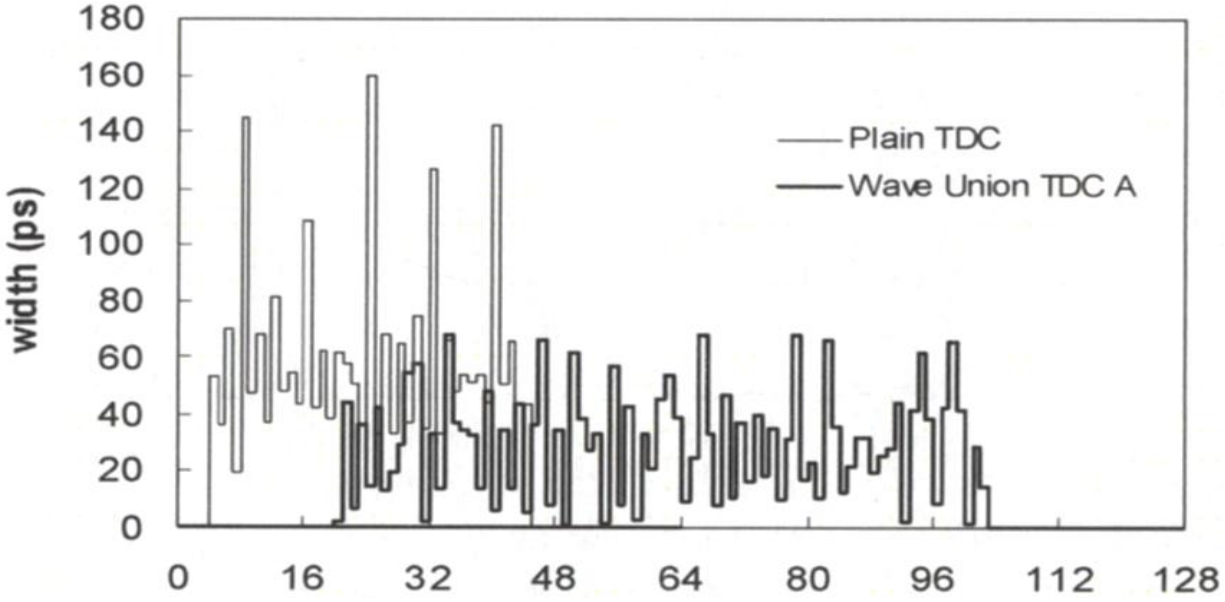


Fig. 7: Differential nonlinearity plot

The most significant origin of DNL is the logic array block (LAB) structure. When the input signal in the carry chain passes across the LAB boundaries (and also the half-LAB boundaries in some FPGA families), extra delays added cause periodic "ultra-wide bins".

To minimize the effect of ultrawide bins, we can subdivide the ultrawide bins and increase their range, this scheme is termed "wave union TDC" and it proves to improve the resolution of the TDC. The key part in the wave union TDC is the "wave union launcher". A wave union launcher creates a pulse train or "wave union" with several 0-to-1 or 1-to-0 logic transitions for each input hit and feed the wave union into the TDC delay chain/register structure, making multiple measurements.

Testing TDC-FPGA Card

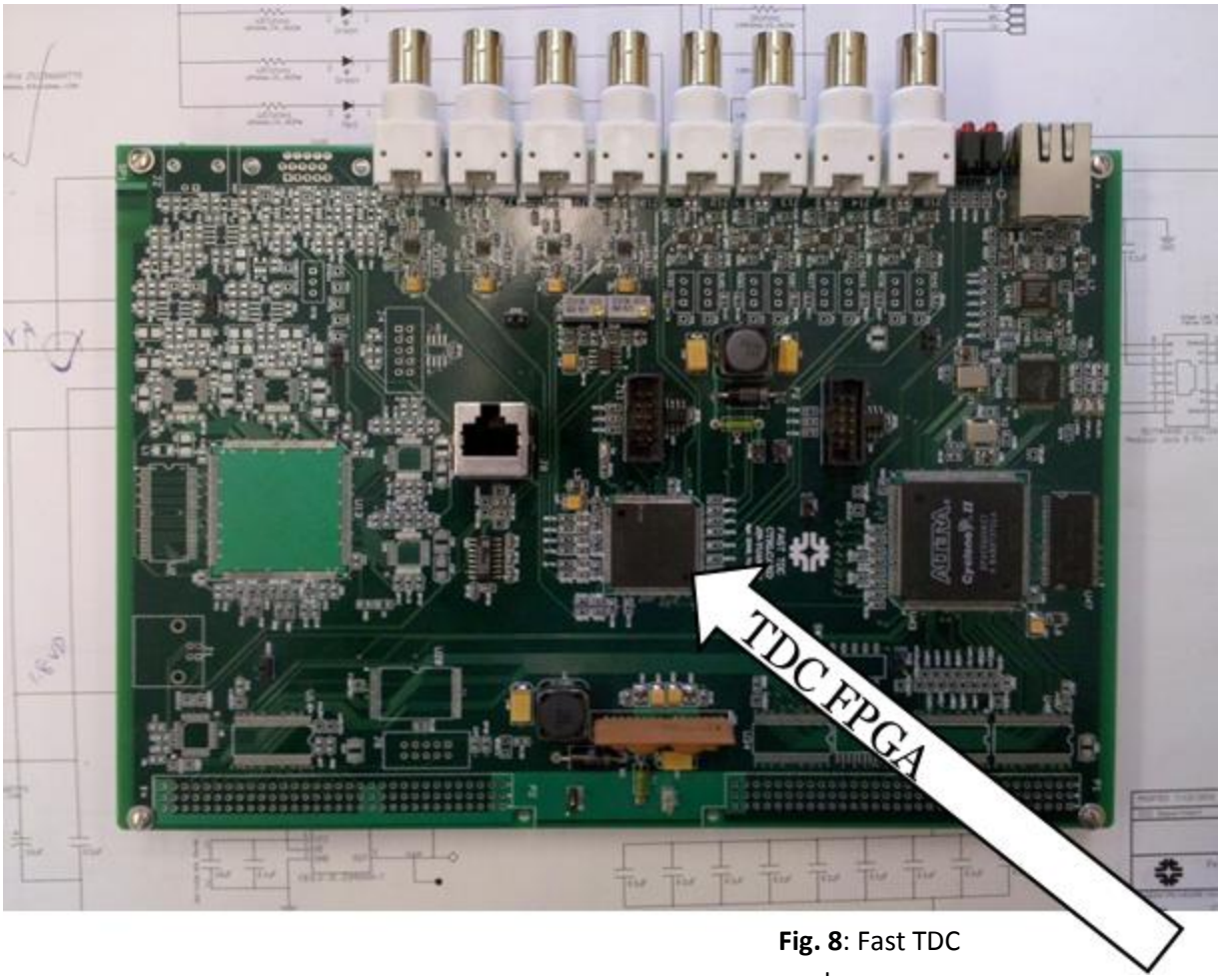


Fig. 8: Fast TDC

A picture of the current board is shown above and the design is to fit the card slots in the feed through. The basic component of the board are labeled in the diagram and they include the power supply, TDC FPGA, DAQ FPGA,USB Blaster, Serial Port , Crystal Oscillators, Ethernet port, BNC Connectors, Configuration Chip and other circuitry.

The device operates in with a 5V power which is further manipulated to produce 3.3V and 2.1V power for other functions in the board. The board is on a test mode, so test signals are mostly internally generated. The device is also currently controlled through the serial port for test

purposes. Hyper Terminal connection is used in a remote computer to send control signals and retrieve data from the device. Input data are alphabets "A-Z" and occasional numbers "0-9". Output is read out as stream of hexadecimal or binary numbers. A detailed manual on the test controls of the board is available in the

Testing the digitization board is very important at this stage to evaluate characteristics and shortfalls of the board and make necessary changes in subsequent devices. Tests ranges from sampling various test signals to acquiring histogram plots.

Results and Discussions

Wave patterns at several points in the boards are investigated using the Oscilloscope. The differential ramping reference volt is verified. The reference voltage runs at 1MHz and ramps up and down. The reference voltage is obtained from a 500ns pulse clock using an RC circuit as shown below.

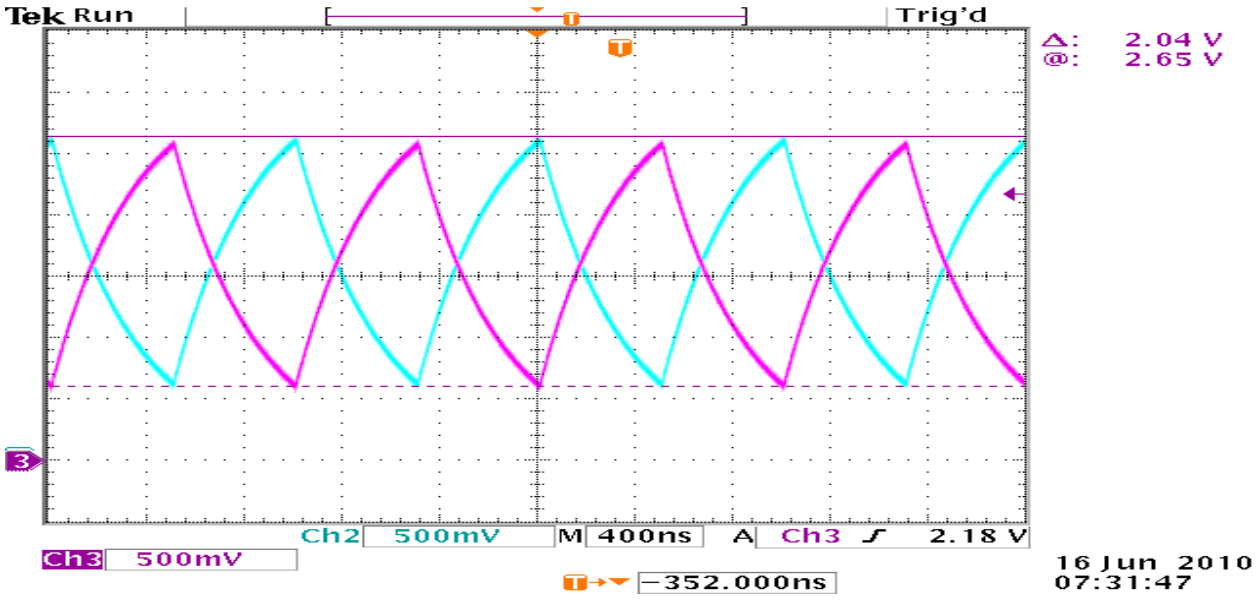


Fig. 9: Ramping Differential Reference Voltage

The TDC FPGA detects the time the test signal hits the ramping ref. signal to a very high resolution. A low amplitude slow ramping test signal 1MHz is fed to channel 3 in the picture below. The times of hit are recorded in hexadecimal numbers and retrieved through a hyper terminal window. After suitable calibrations and conversions, we can reconstruct the test signal at a high precision (70ps LSB). We saved important data from Hyper Terminal as text files and imported them to Microsoft Excel for data formatting and making plots.

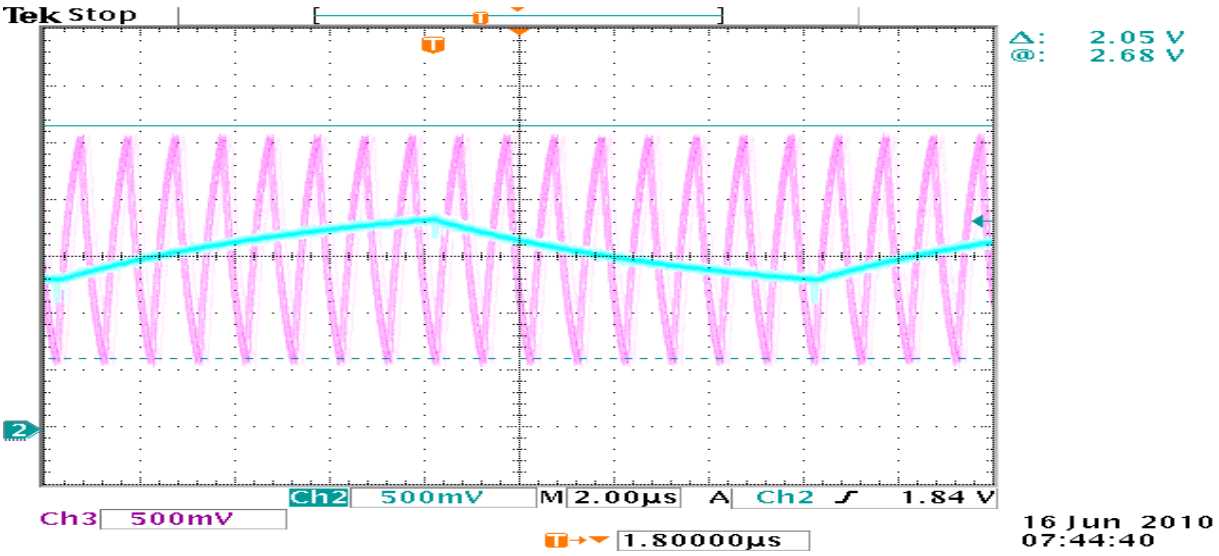


Fig. 10: slow Ramping signal is sampled

Several internal factors affect the performance of the TDC FPGA, including the temperature, noise, voltage and structural imperfections of chip. To verify the optimal performance input amplitude voltage rage, we varied the offset voltage of the differential input while keeping the differential input constant. This common mode signal input is exploited and the goal is to find ranges of input within which TDC performance is optimized. The test results are illustrated below.

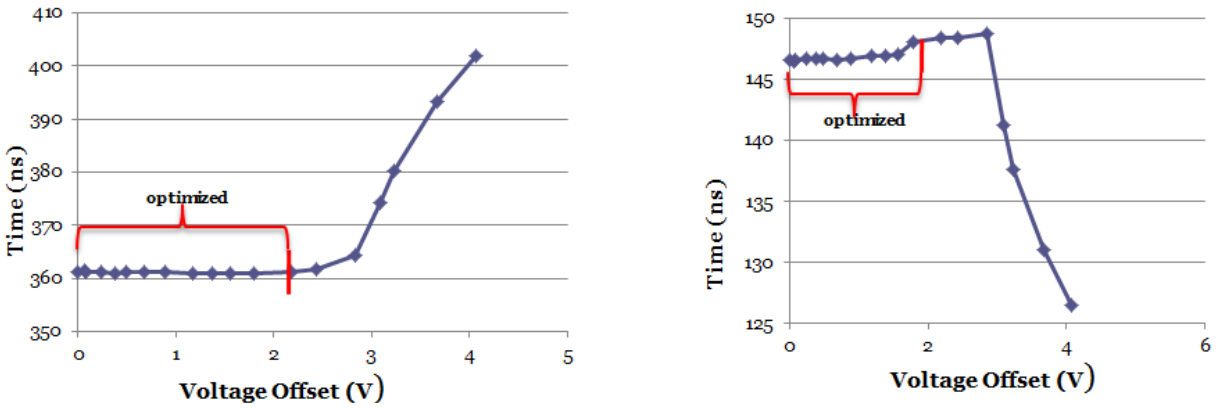


Fig. 11: Optimizing common mode signals for ramping up and ramping down signals. An offset range of 0 – 2 Volts allows for optimal performance of our fast TDC

When the card is fully functional, an important software component needs to be applied to analyze the data collected from the TDC. Hit times need to be converted into the original signal. The conversion scale is the look-up table. To obtain a lookup table, we supplied known signals to the TDC and matched it up with corresponding hit times detected. We also simulated the TDC card performance using the circuitry analysis. Comparing the two plots will show the accuracy of the device.

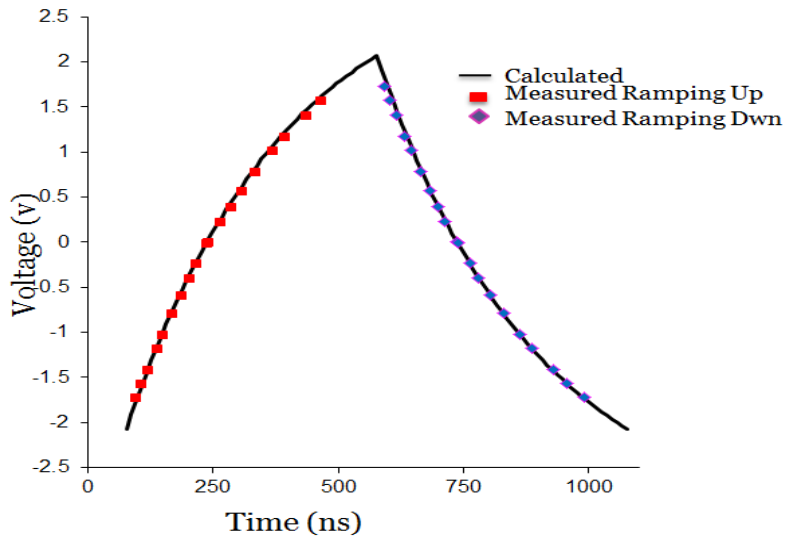


Fig. 12: Calibration of TDC.

Note that measure and calculated sample points match.

Also note the range of the sampled points.

The calculated lookup table expression can hence be applied to test signals

With this lookup table we can reconstruct signals. To show this we regenerated test signals. All input signals are supplied on a differential mode. The test signal can be first viewed on an oscilloscope and later compared with the regenerated signal. The TDC is controlled from the serial port and all analyses are made on a remote computer using Microsoft Excel®. The test will verify the wave form, the amplitudes and signal times. The ramping-up reference voltage samples separately from the ramping down voltage, therefore it will be important that both samples match in the regenerated signal output.

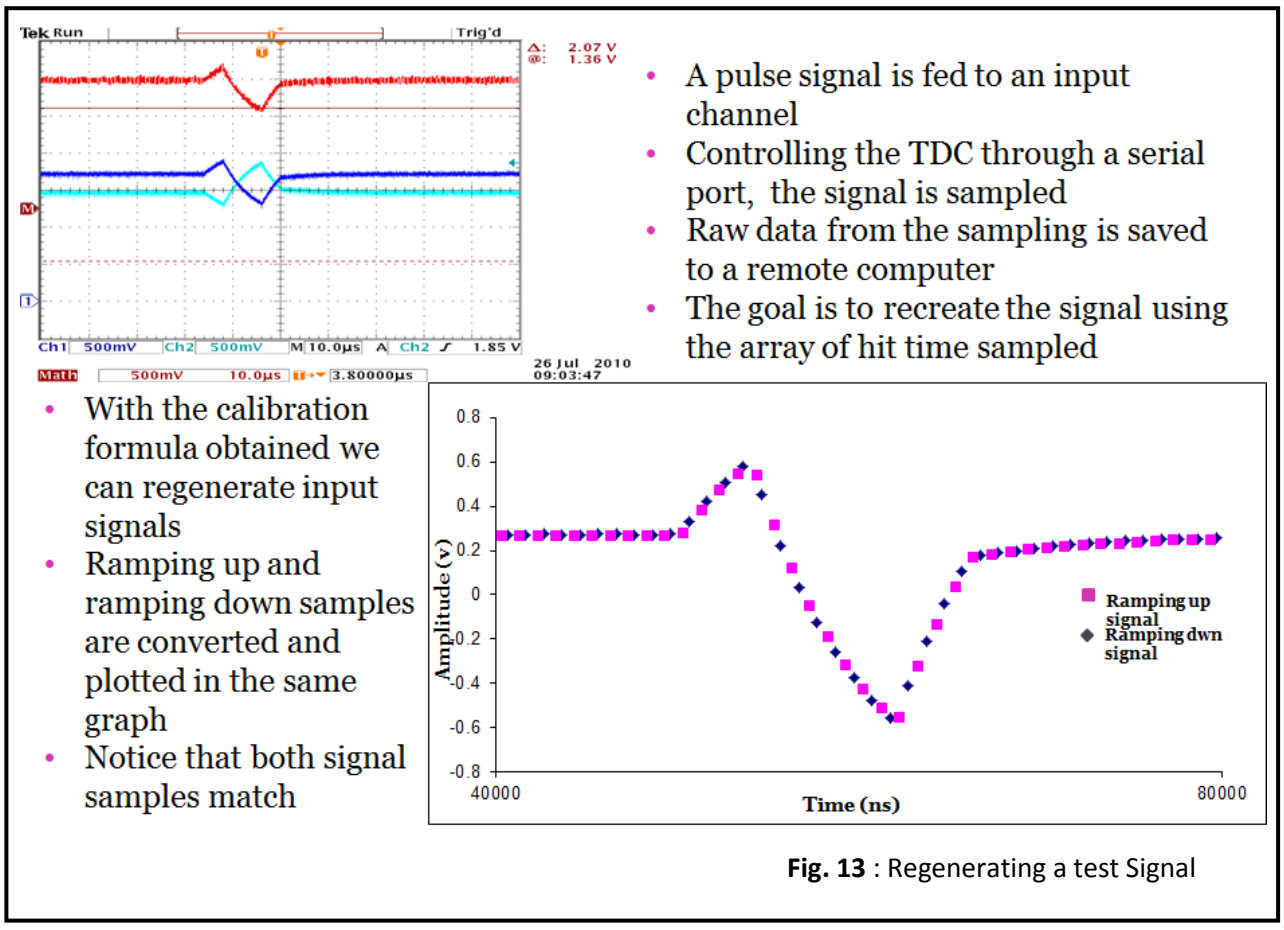


Fig. 13 : Regenerating a test Signal

The fast TDC is a high precision device. Precision can be pictorially evaluated using histograms. Histograms count number of hits obtained from the several input channels. The hits are grouped in the "bins" where they occur. Bins in our case are obtained from LSB time hits. The time is a counted as a hexadecimal number therefore we have 16 bins to accumulate hits in. This implies that TDC card firmware accumulates hits on each bin. From the Hyper Terminal window, we can upload the hits and import them into a suitable software (MS Excel®) to generate a histogram. Histograms from different signals give an insight to how well the TDC precisely detects time of hit.

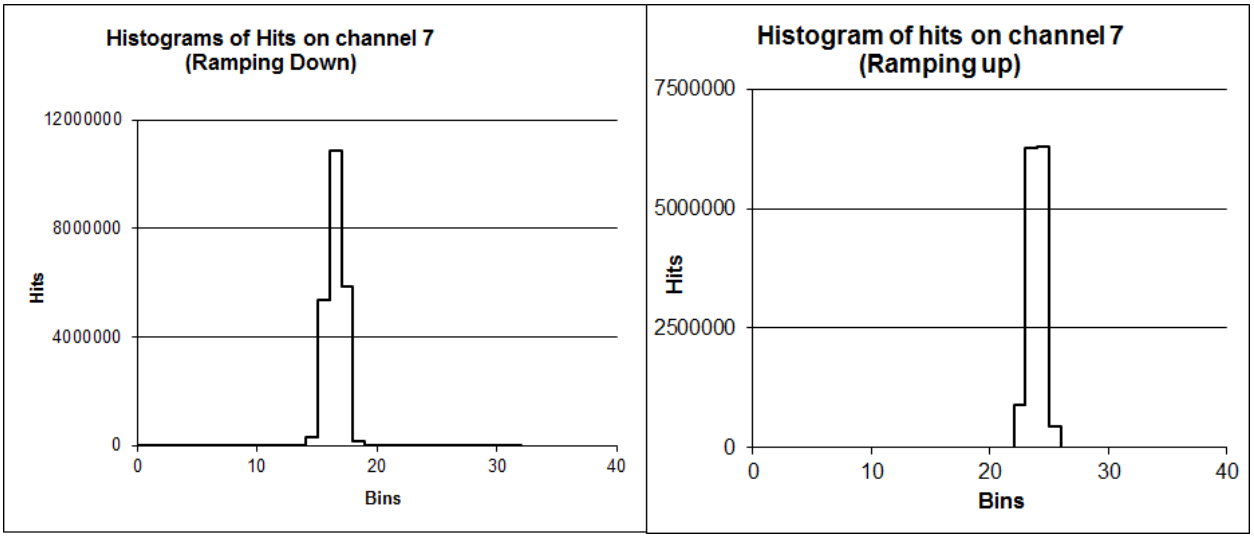
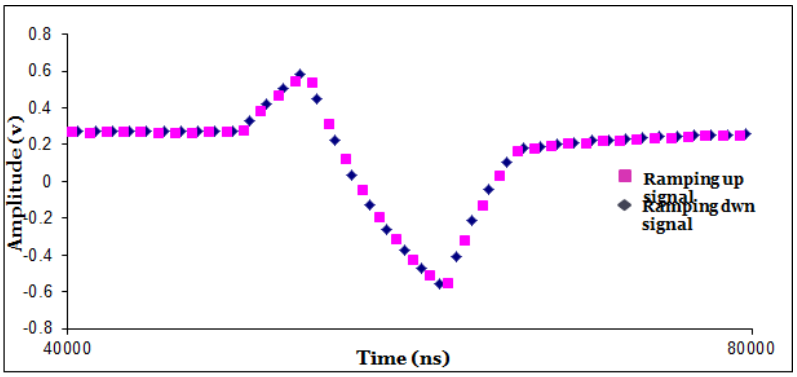
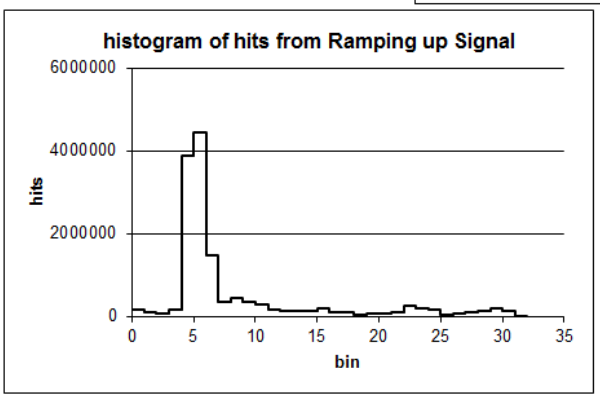


Fig. 14: Histograms for a constant amplitude signal

- With a constant amplitude signal, we expect a sharp pic and little variance
- Channel 7 is supplied with a constant amplitude signal.
- Histograms of both ramping up and ramping down samples confirms our prediction

- A varying amplitude like the pulse signal will be interesting to analyze on a histogram.
- Observe the noticeable peak and the smaller bumps.





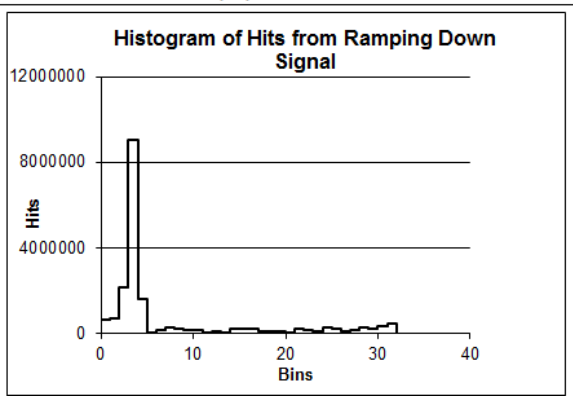


Fig. 15: Histogram on test pulse signal

Conclusion

There is no doubt that digitization is plausible at feed through. The only concern is the perfection of the digitization scheme. Precision, noise handling and efficiency are all important in choosing a digitization design. Delay chain TDC FPGA has a high precision in hit time detection. The current design shows promise of even better precision. Delay chain TDC is therefore suitable to replace the ADC digitization scheme. Extra work needs to be done in calibration of TDC FPGA. Extra work on calibration should include study of effects of temperature, noise and voltage on TDC digitization. Imperfections on the delay buffers have thus been a limitation to the precision of the TDC, so it is natural; to seek better improved FPGA buffers. After our work this summer I think it is wise to develop software that can make histograms or regenerate sampled signals at the request of the user. It is an arduous task to work through excel® for the purpose of getting a single histogram or a signal recreation, therefore a simple software can make things a lot easier. Moving forward I recommend that all channels be tested and compared with each other for discrepancies. I also recommend sending signals externally through the input ports.

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