# Optical Link R&D Activity and Plan

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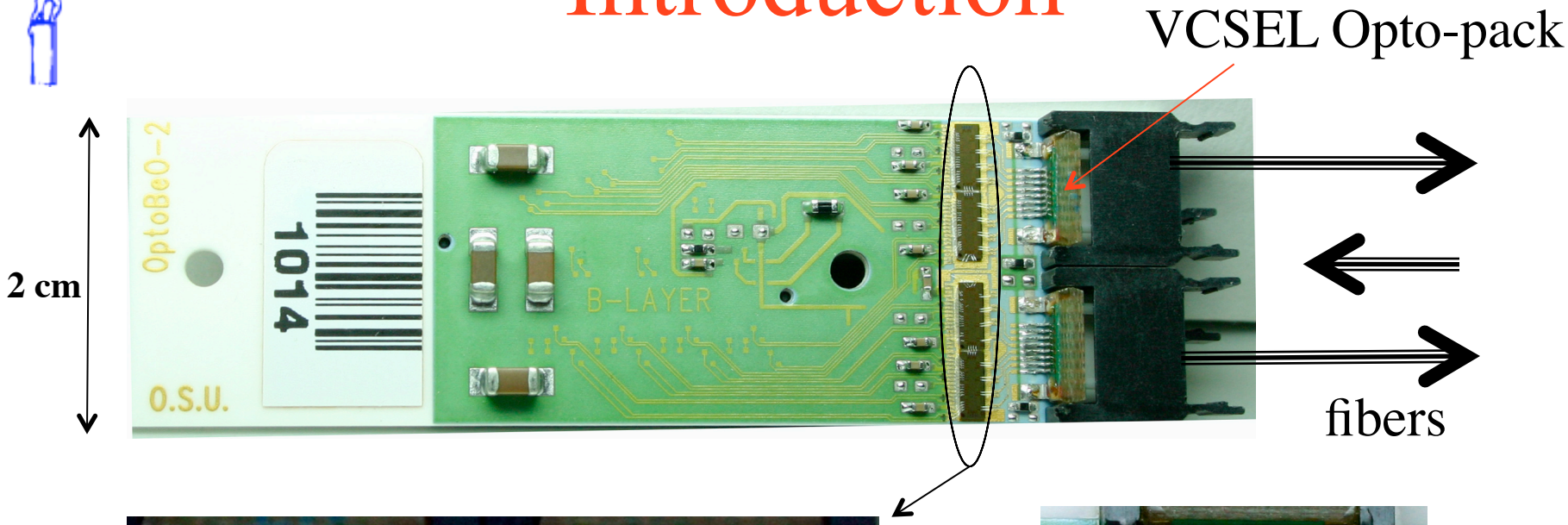
# Outline

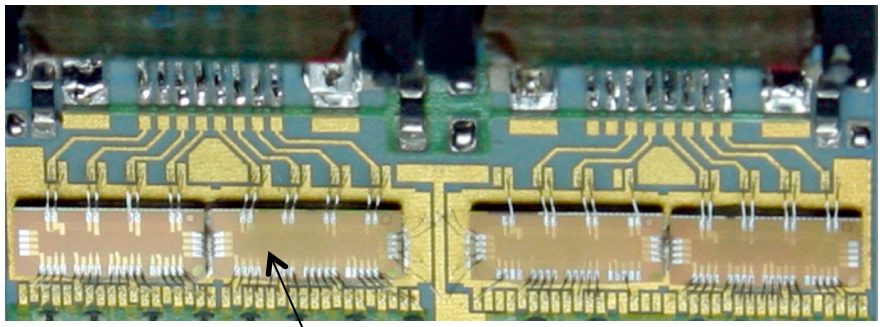
- Past Activity
- Present Activity
- Plan

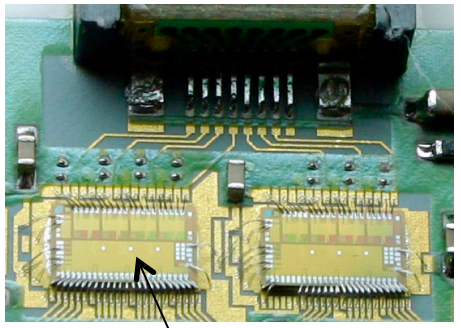
# Past Activity

- Lead the R&D and production
  of on-detector optical links of the ATLAS Pixel detector:
  - collaborator: Siegen
  - 1744 receivers (PIN) and 1788 transmitters (VCSEL)ps:
  - design, prototype, irradiation, and QA of chips:
    - use IBM 0.25 μm process
    - VCSEL driver array operating at 80 Mb/s
    - PIN receiver/decoder array to decode
      bi-phase mark (BPM) signal encoded with 40 MHz clock
    - a collaborative research between Siegen and Ohio State
  - design, prototype, irradiation, and QA of optical modules:
    - 272 opto-boards in final system

# Introduction





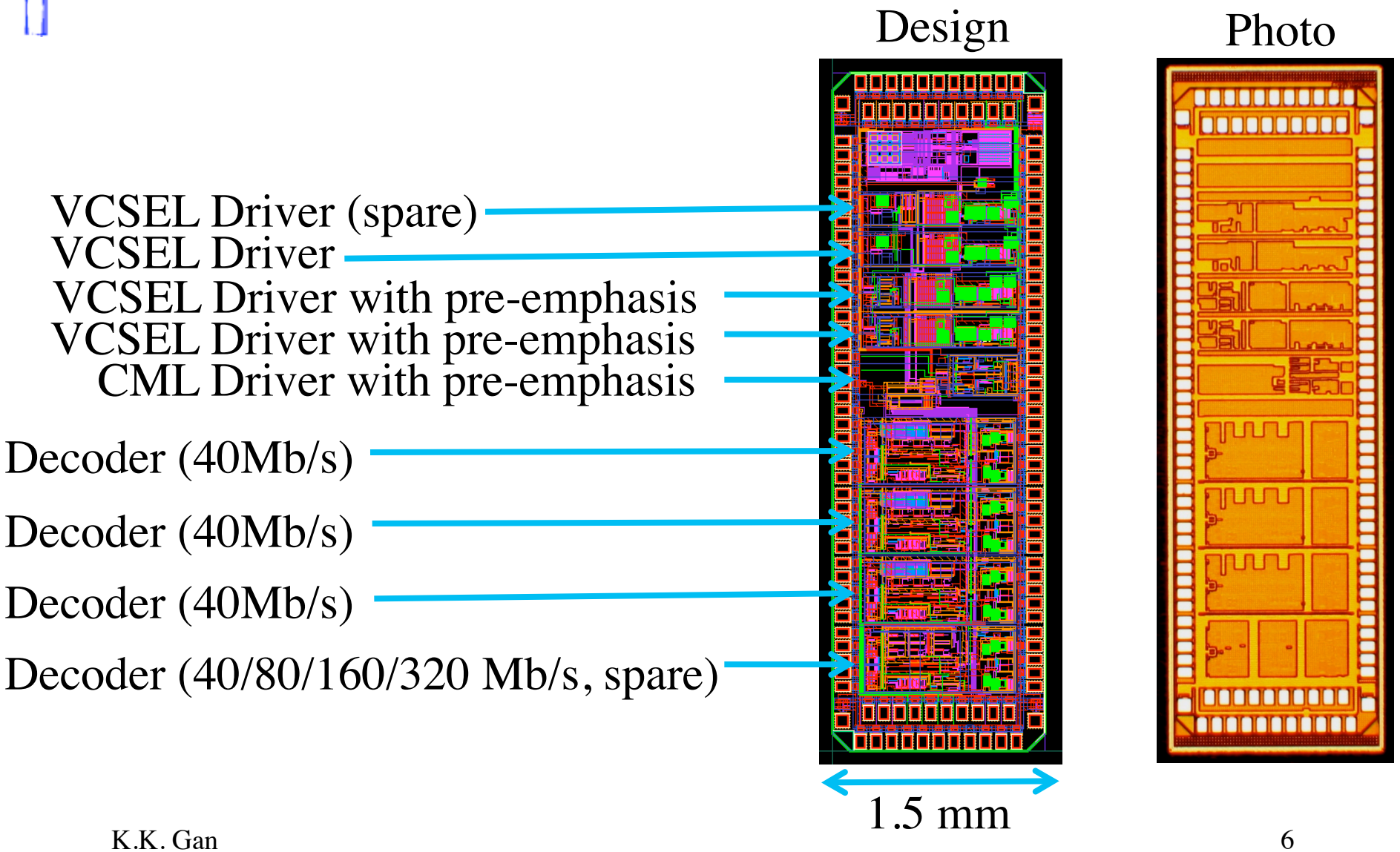
VCSEL Driver Chip (VDC)

PIN Receiver (DORIC)

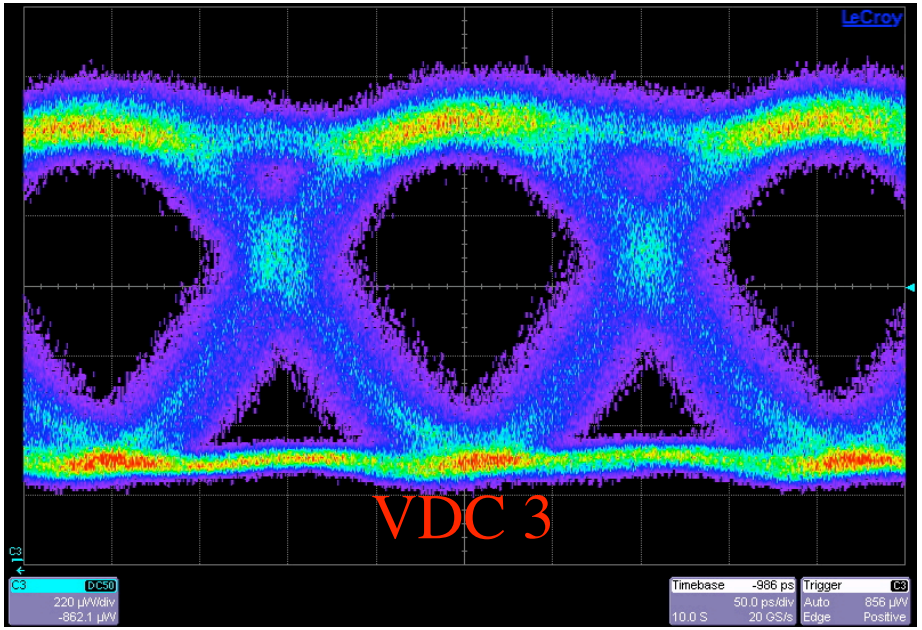
# Current Activity

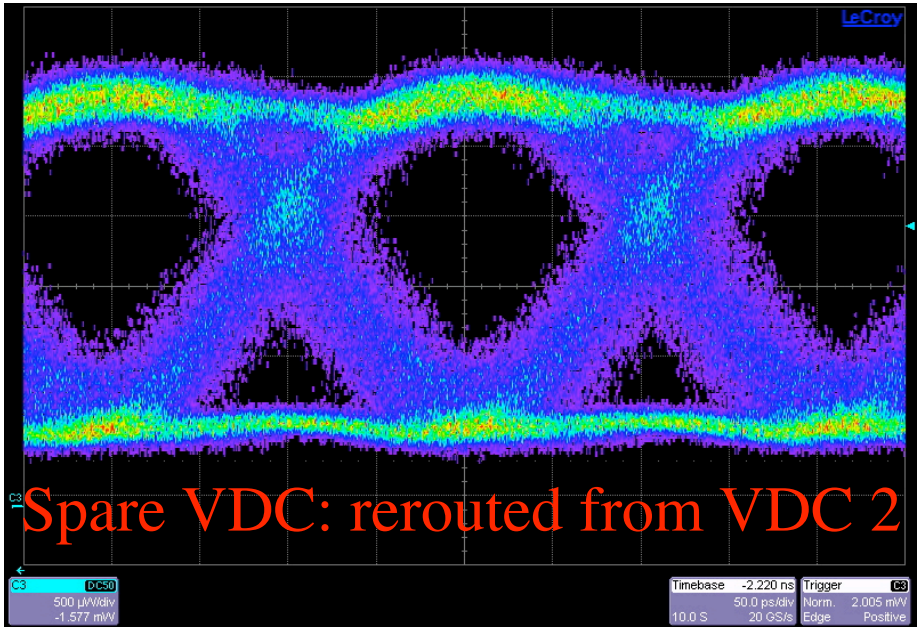
- ATLAS proposed to add one more layer to the current pixel detector:
  - "Inner B-Layer" or IBL
  - installation ~ 2016
  - optical links will use VCSEL/PIN array as in current pixel detector
  - design an updated version of current driver and receiver with redundancy and individual VCSEL current control
    - experience gained from the development/testing of such new chips would help the development of on-detector array-based opto-links for SLHC
      - ⇨ submission of 1st prototype chip (130 nm) in 2/2010
    - a collaborative research between Siegen and Ohio State

# Chip Content



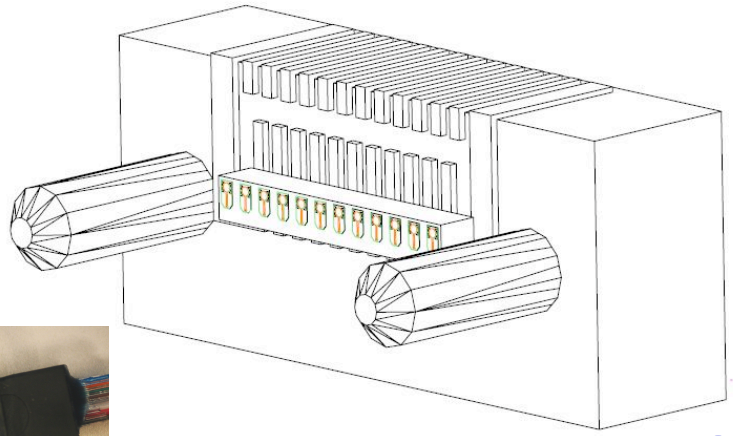
# Eye Diagrams @ 4.8 Gb/s




- No pre-emphasis
- Rise/fall times: ~60-90 ps
  - Measured with 4.5 GHz optical probe
- Bit error rate < $5 \times 10^{-13}$

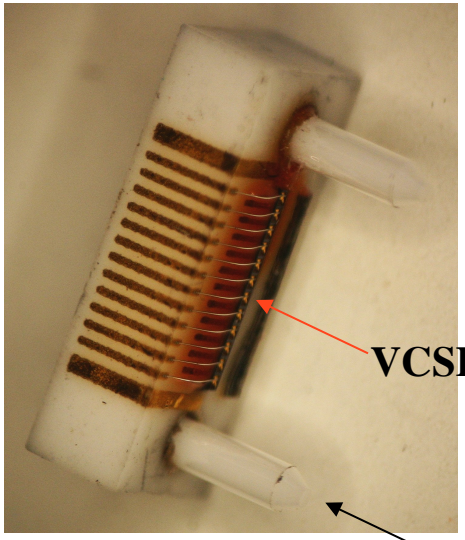
# Opto-Packs



OSU

BeO


MT ferrule

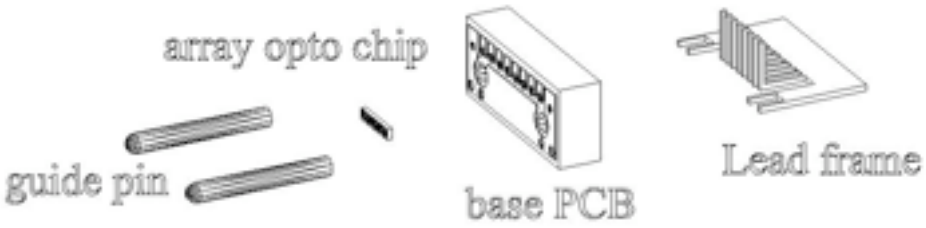


VCSEL array

Ceramic guide pin

opto package

Taiwan



# Proposal to Develop On-Detector Array-based Optical Link

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November 11, 2009

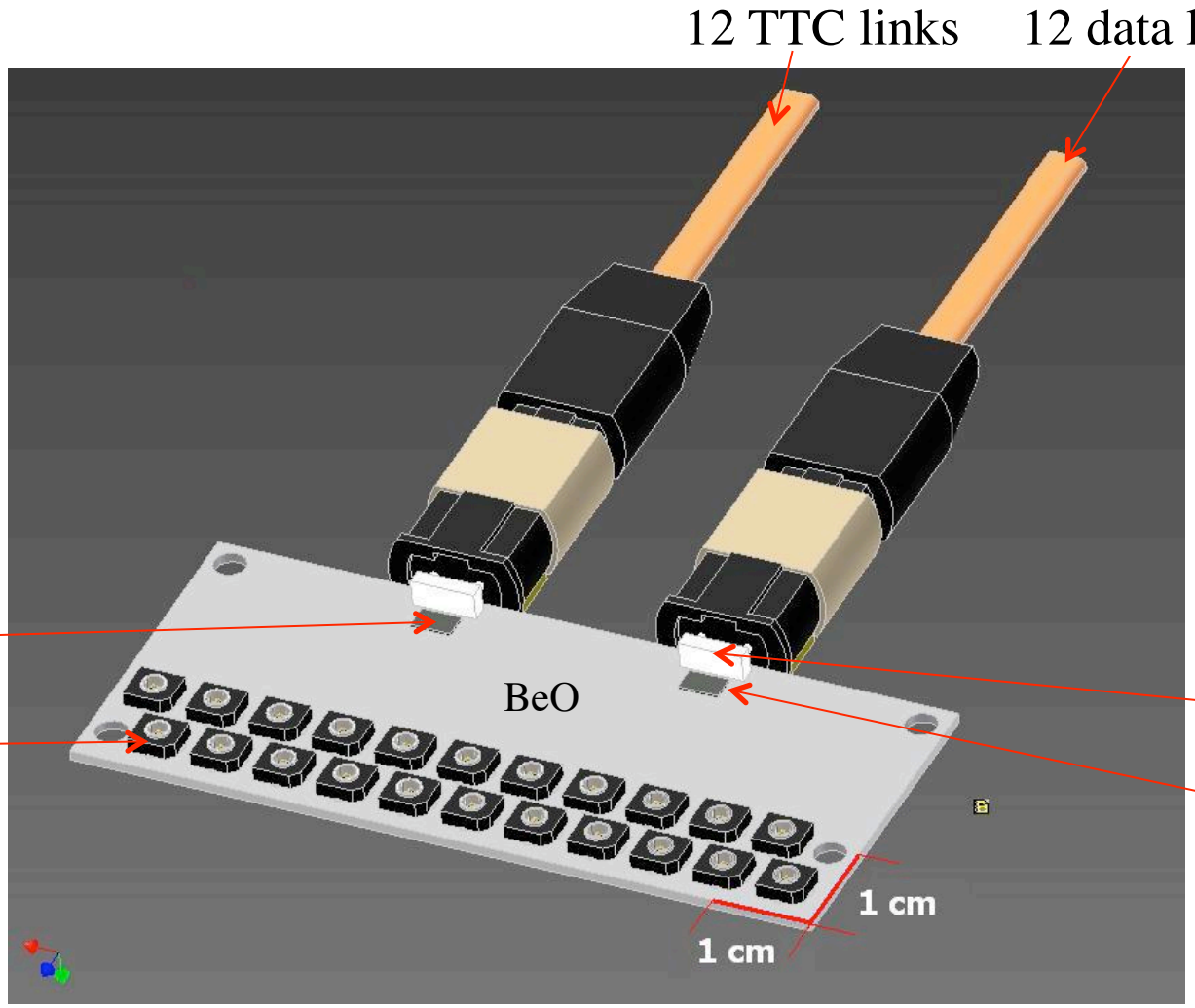
# Motivation

- VCSEL and PIN are available in three forms:
  - single channel or 4 or 12-channel array
    - array: can reserve 1 in 12 channels for redundancy
    - single channel: double the number of channels for redundancy
      - ⇨ array solution reduces the number of opto-modules to be built by a factor of 22

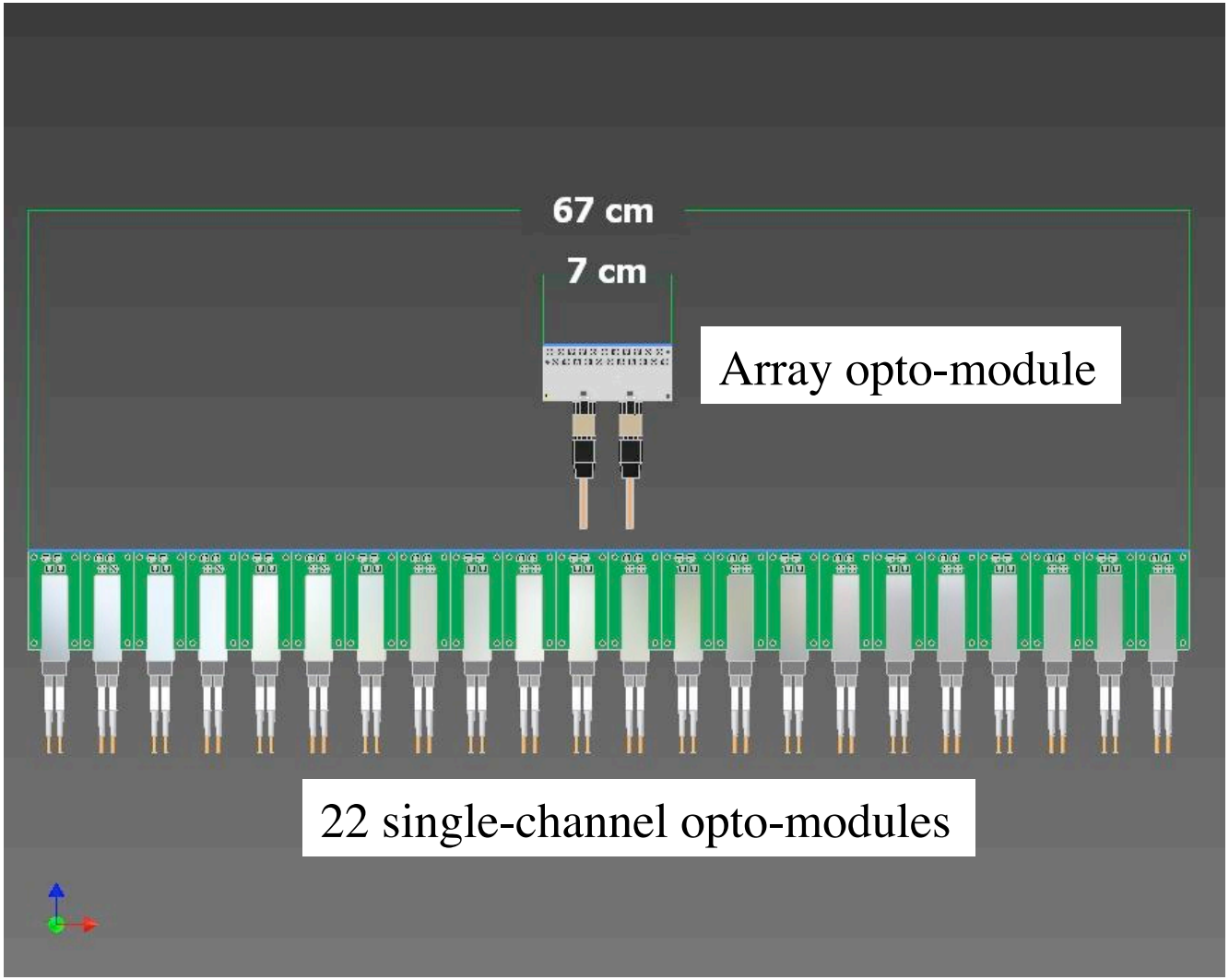
# Pros of Array-Based Optical Link

- highly compact
  - much less material in front of LAr
- simplify fabrication/installation
  - 22 times less opto-modules to build, test, and install
- no ribbon to LC fanout
  - reduce optical power loss
  - simplify installation
- reduce electrical services
  - single power line for receiver/driver ASICs instead of 11 individual power lines
  - single power line for a PIN array instead of 11 individual lines
- simplify cooling
  - cool a small area rather than much larger area
  - consume half as much power

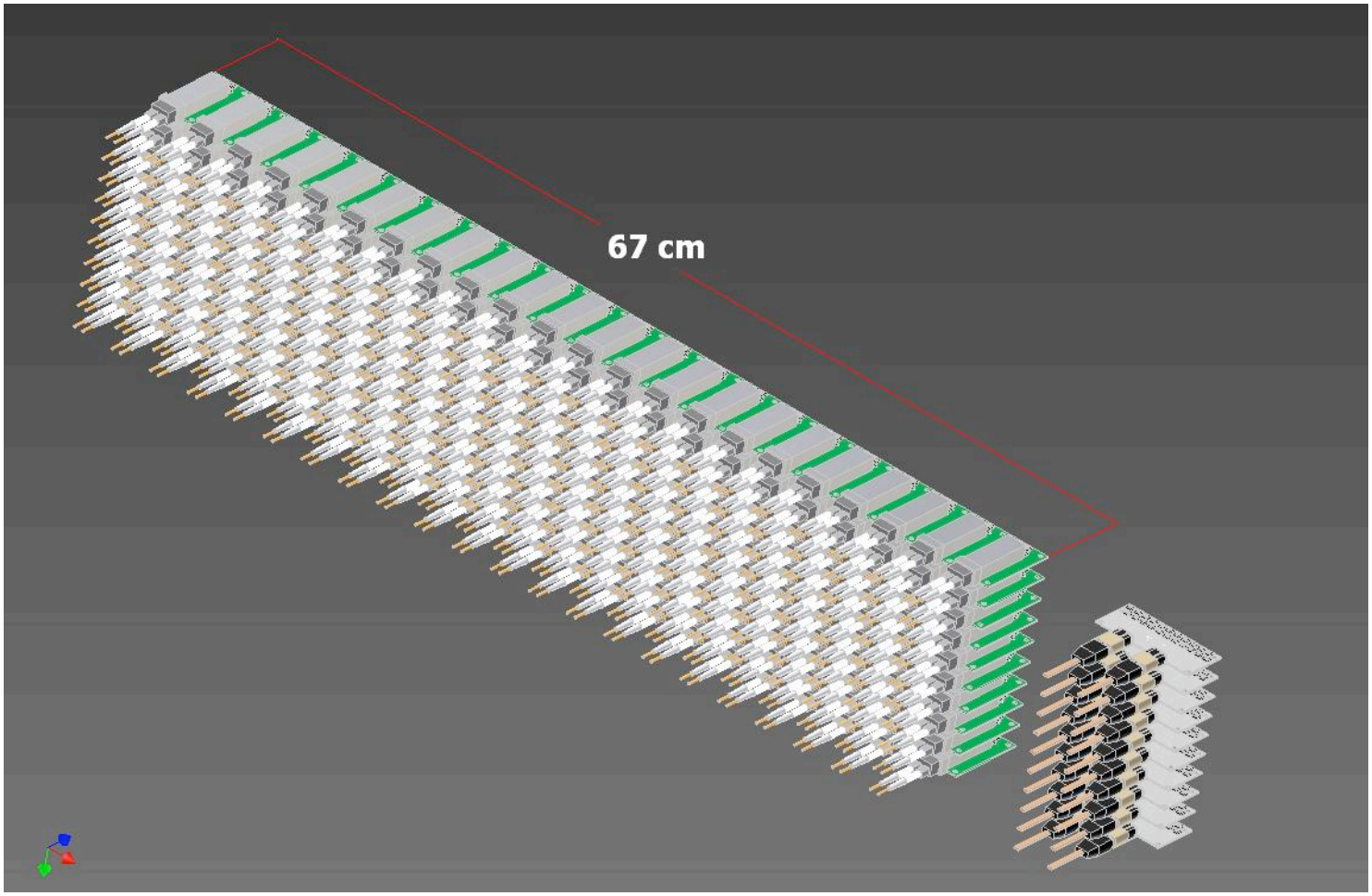
# Array-Based Opto-module



# Array/Single-Channel Opto-Module



# Array/Single-Channel Opto-Module



# Cons of Array-Based Optical Link

- single point connection failure in power to ASIC or PIN could disable an opto-module
  - opto-modules will be accessible every 1-2 years

# Array ASIC R&D Plan

- VCSEL driver/PIN receiver developed by GBT/VL must be laid out as an array
  - will work closely with GBT/VL groups
  - special thanks to P. Moreira for thoughtful advice

# Summary

- Significant experience in array-based opto-links
- Developing arrays-based opto-links for the 2016 and 2020 upgrades
- NIKHEF/Ohio State/Siegen/Wuppertal proposal for array-based solution for SLHC has been accepted as official SLHC R&D