Research Activities on Optical Links at SMU

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Southern Methodist University

Optical Data Transmission Workshop

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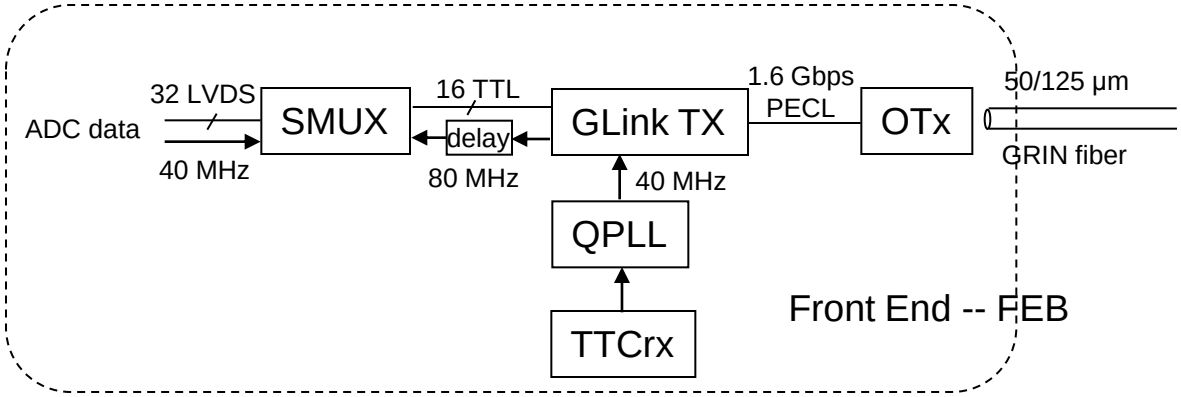
Outline

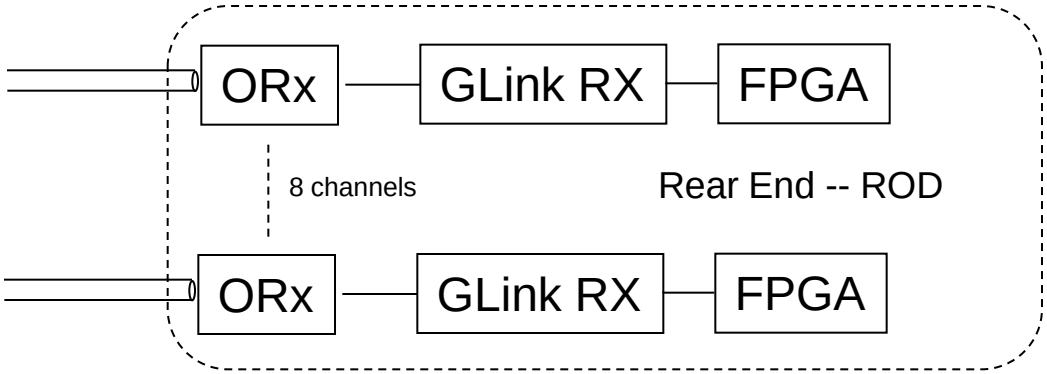
1. ATLAS LAr optical links
2. Optical links for ATLAS upgrade
   - ASIC development
   - Optical Interface development
3. Cryogenic test of optical links
   - Transistors, Ring oscillators, Serializer
   - Optical fibers, Lasers
4. Summary

ATLAS LAr Optical links

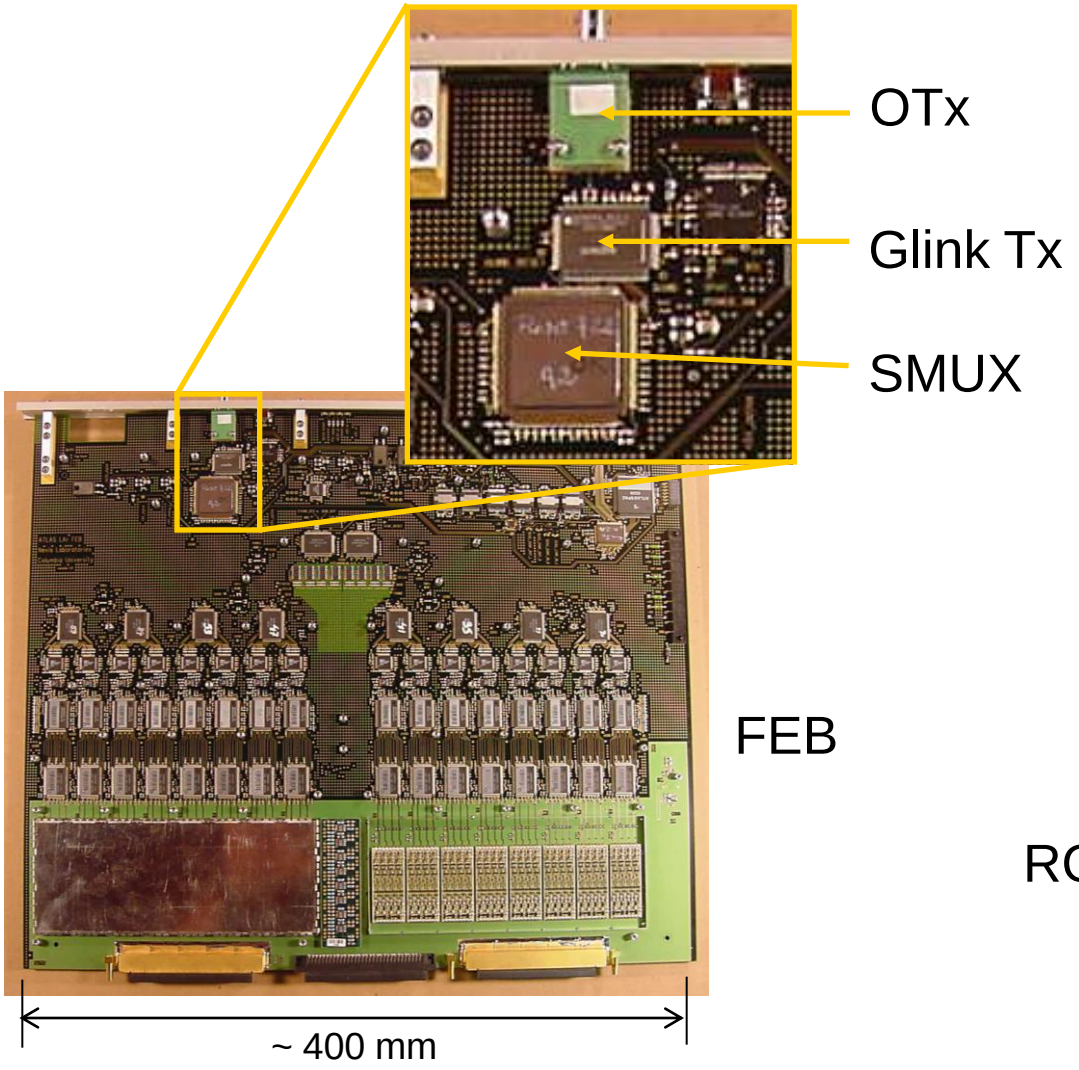


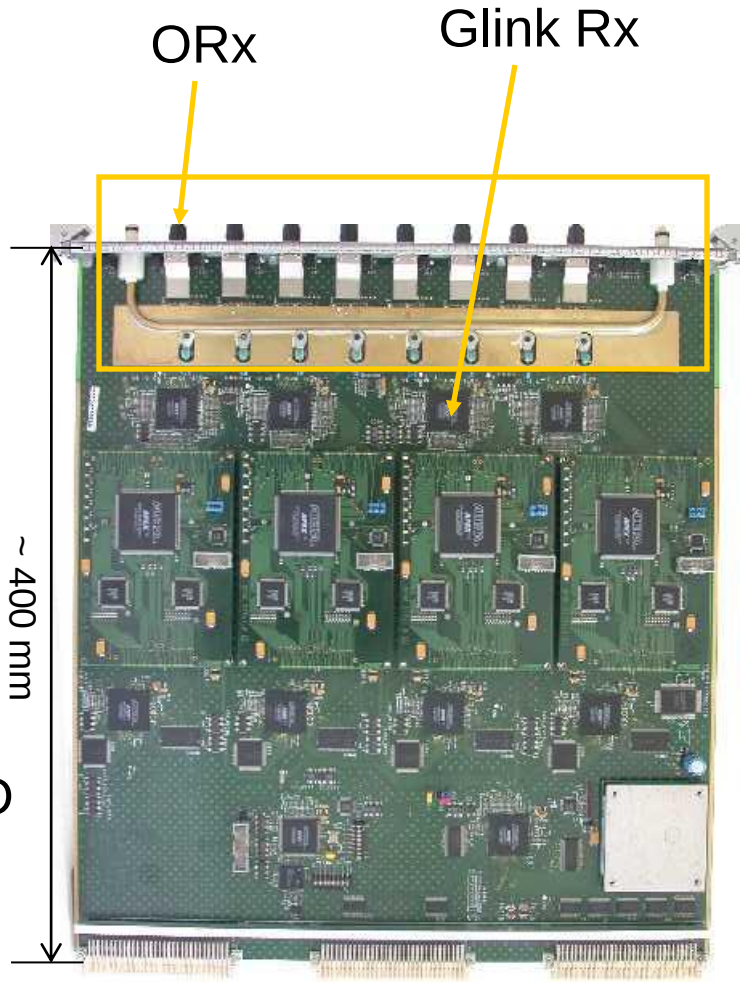
- 1524 optical fibers in total, 1.6 Gbps per fiber, 2.4 Tbps total data rate
- All front-end components were qualified for 360 krad(Si)
- SMU chose Glink and tested OTx/ORx and Jignbo Ye was the coordinator

- SMUX: an ASIC based on DMILL, level translating, 2:1 multiplexing
- GLink: COTS, operates outside of spec, specially ordered from Agilent
- OTx, ORx: VCSEL/PIN based, assembly produced by IPAS in Taiwan, with COTS driver and amplifiers



ATLAS LAr Optical Links





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Optical links for ATLAS Upgrade - Requirements

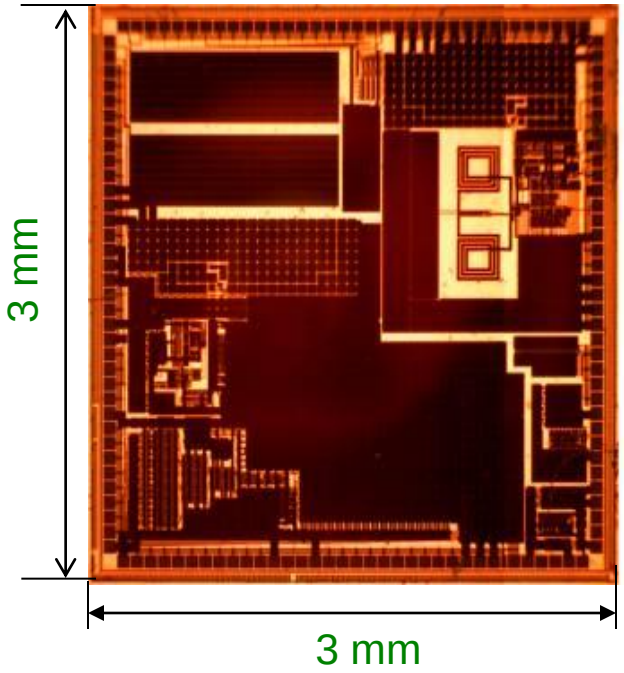
- Upgrade requirements

	Present	Upgrade
Data rate per FEB (Gbps)	1.6	100
Power consumption per Gbps (mW)	1188	90
Redundancy	NO	YES
Radiation Tolerance	360 Krad	3.6 Mrad

- SMU participates in two parallel tasks:
  - ASIC development
  - Optical interface development

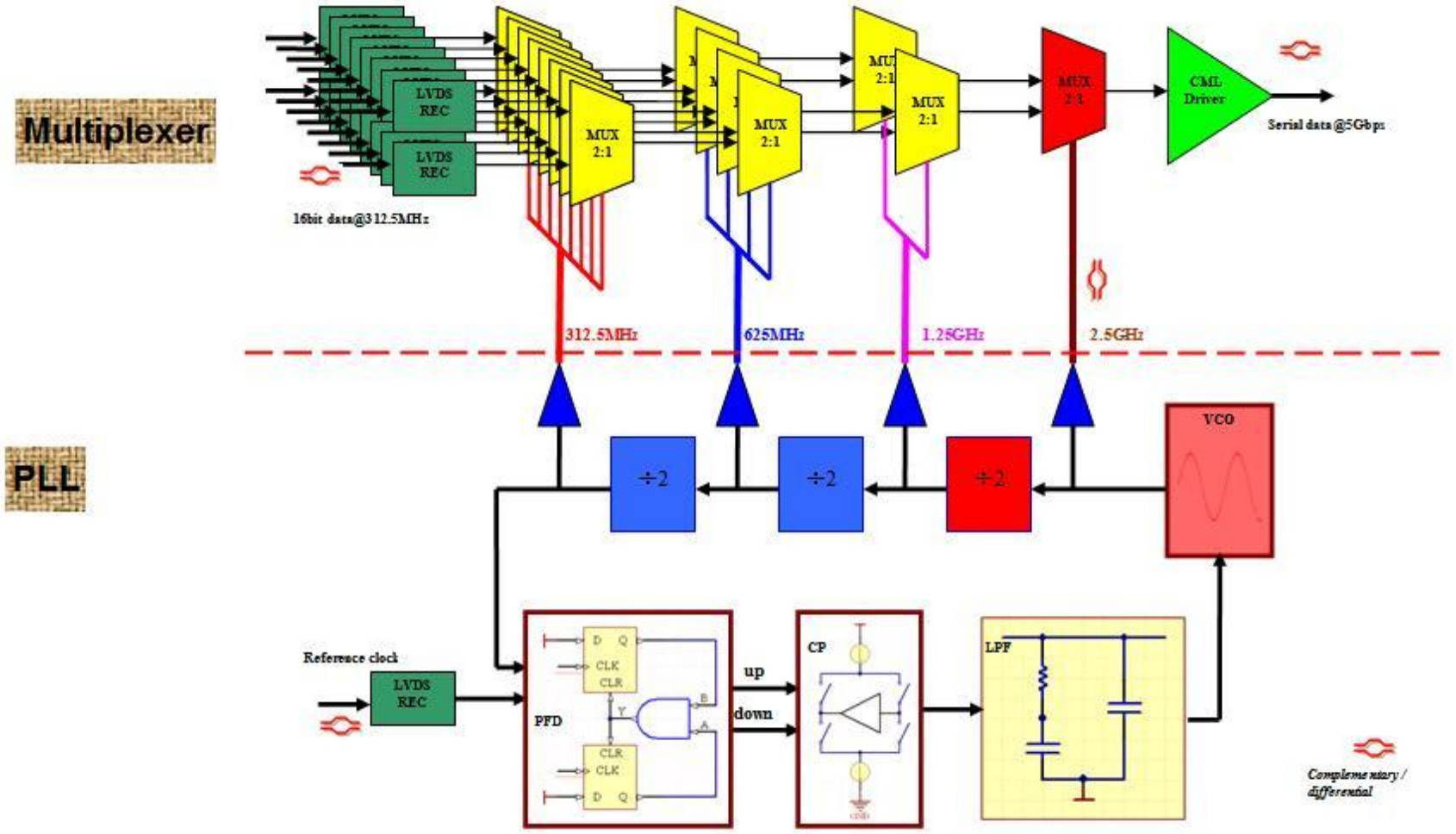
Optical Links for ATLAS Upgrade - ASIC Prototype

- Submitted in Aug. 2009
- Delivered in Nov. 2009 (143 dies)
- Implemented in area 3 mm × 3 mm
  - LOCs1: 5 Gbps 16:1 serializer
  - LCPLL: 5 GHz LC VCO based phase locked loop used to generate the clock of the future 10 Gbps serializer
  - CML driver up to 8.5 Gbps
  - divide-by-16 divider
  - Varactor (voltage controlled capacitor)
  - SRAM



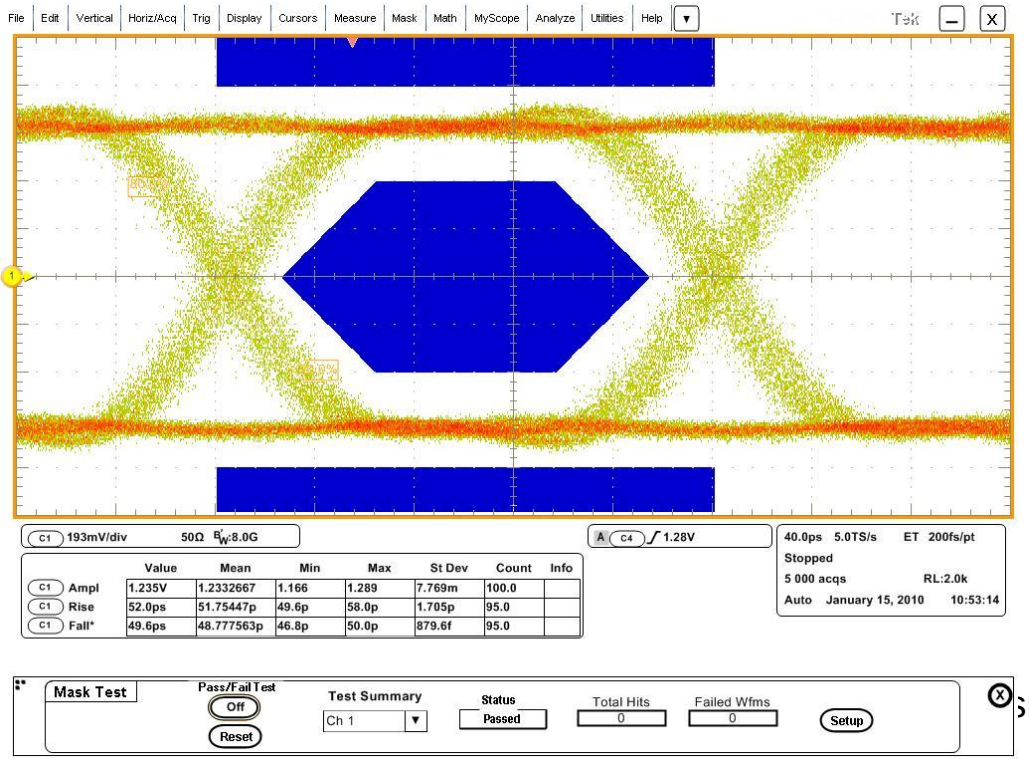
Optical links for ATLAS Upgrade - 16:1 5-Gbps Serializer

Block diagram

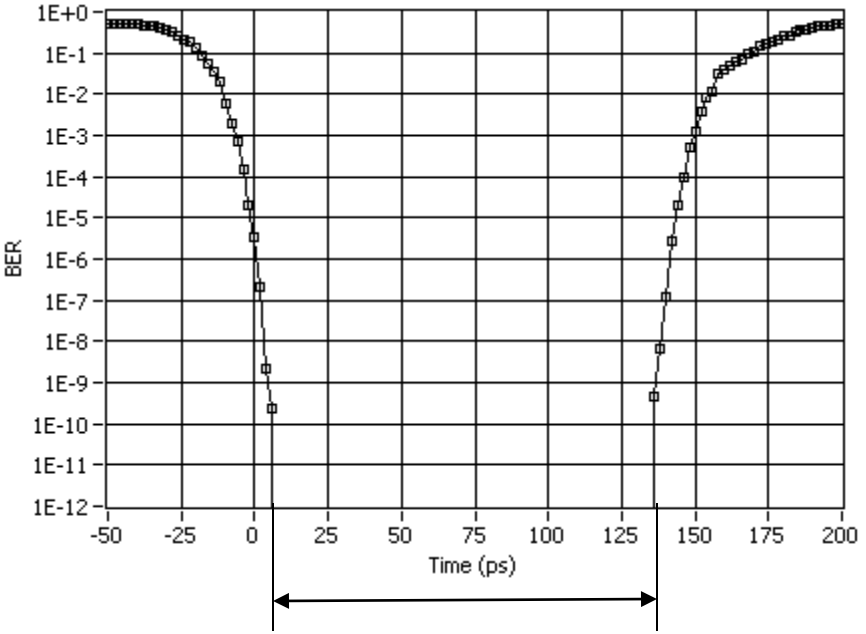


Optical links for ATLAS Upgrade - Serializer Test

Eye diagram at 5 Gbps and eye mask adapted from FC 4.25 Gbps and scaled up to 5 Gbps



Bathtub curve at 5 Gbps

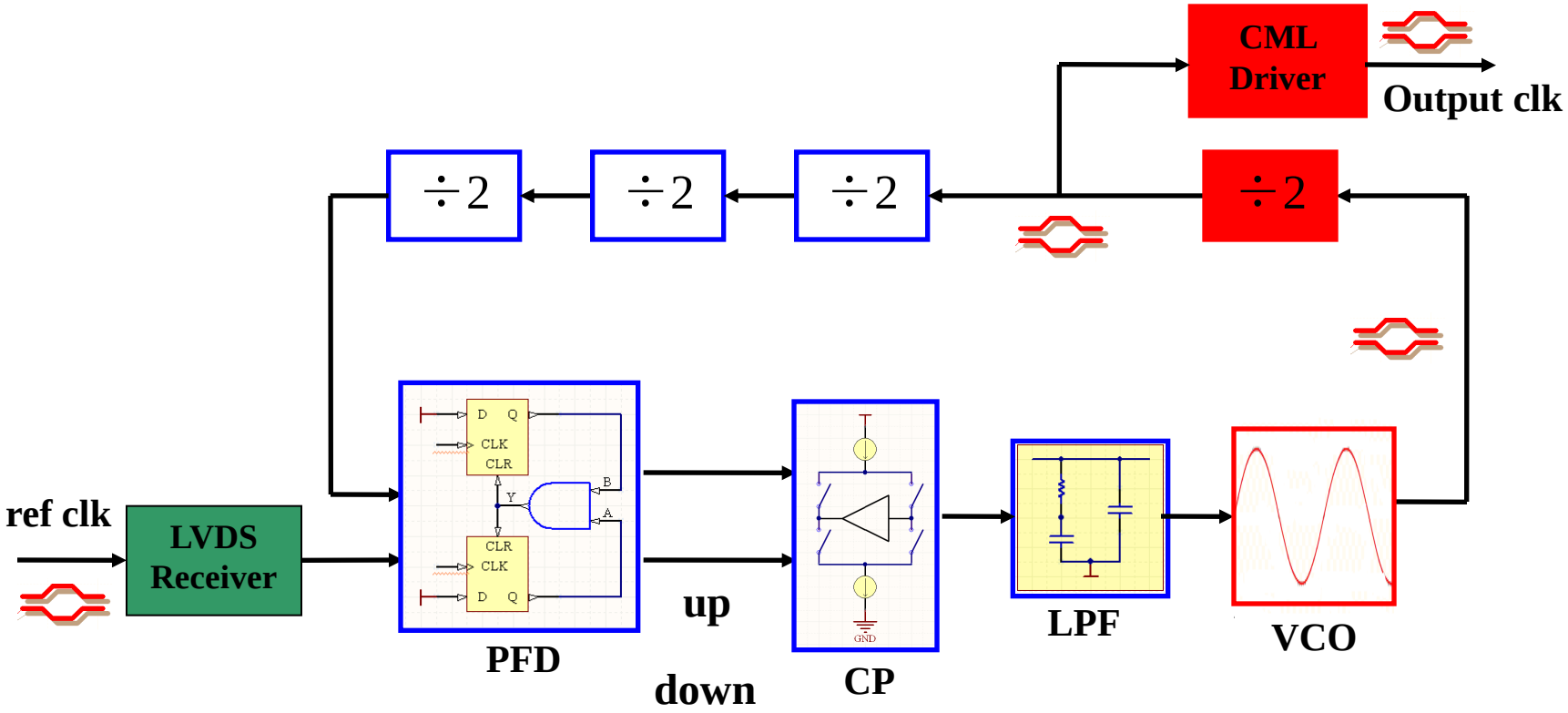


Optical links for ATLAS Upgrade - Serializer Performance

- Test results summary:
  - 12 chips wired bonded to PCBs for testing. Five boards have problems: 2 Vcc shorts, 2 Vcc open, 1 with a stuck bit. They are all traced to the place where the chip is encapsulate: chip problems? Wire bonding problems? Tests on more chips will tell.
  - For the 7 chips/PCBs that are working:
    - Range (Gbps): min: 3.8 – 4.0, max: 5.7 – 6.2.
    - Power (based on 1 chip): 507 mW at 5 Gbps.
    - Output signal at 5 Gbps:

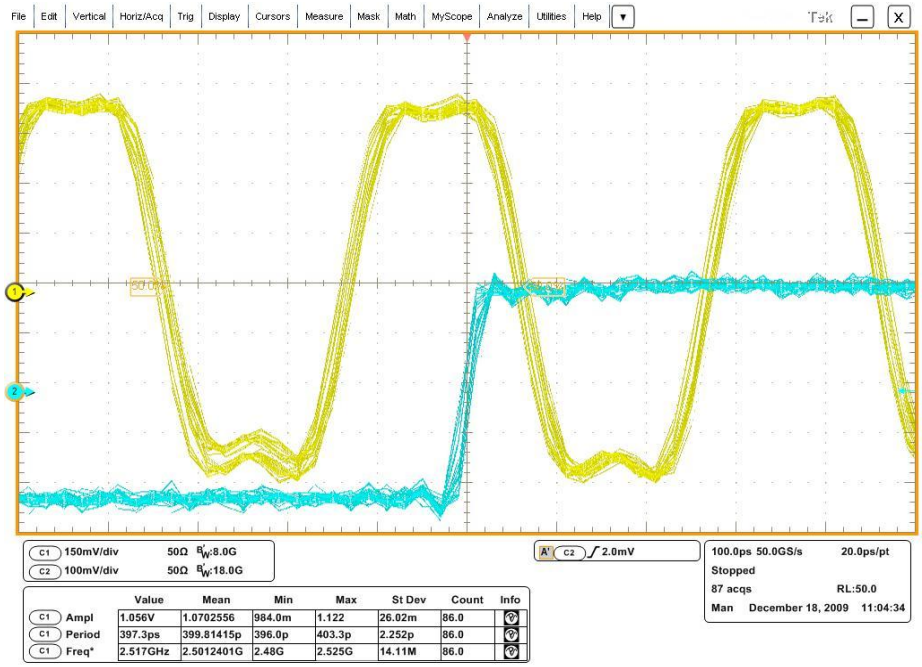
amplitude (V)	1.16 ± 0.03
Rise time (ps)	52.0 ± 0.9
Fall time (ps)	51.9 ± 1.0
Random jitter (ps)	2.6 ± 0.6
Total deterministic jitter (ps)	33.4 ± 6.7
DJ: periodic (ps)	15.1 ± 3.4
DJ: data dependent (ps)	3.0 ± 2.3
DJ: duty cycle (ps)	15.2 ± 3.8
Total jitter at BER@1E-12 (ps)	61.6 ± 6.9
Eye opening at BER@1E-12	(69.3 ± 3.7)%
Bathtub curve opening at BER@1E-12 (ps)	122 ± 18

Optical links for ATLAS Upgrade - Block Diagram of 5 GHz LCPLL



Optical links for ATLAS Upgrade - PLL Test

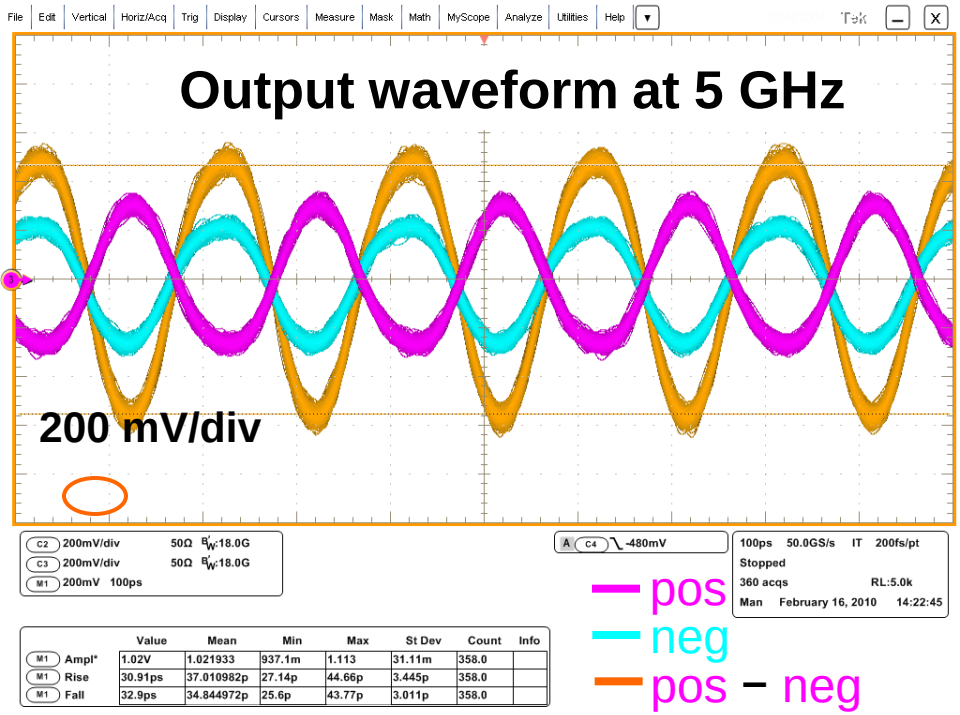
- Tuning range: 4.7 to 5 GHz.
  - Simulation: 3.79 to 5.01 GHz. Cause understood and will be fixed in next iteration.
- Power consumption: 121 mW at 4.9 GHz.
  - Compare: ring oscillator based PLL, 173 mW at 2.5 GHz
- Random jitter: 1 - 2.5 ps (RMS)
- Deterministic jitter: < 17 ps (pk-pk)

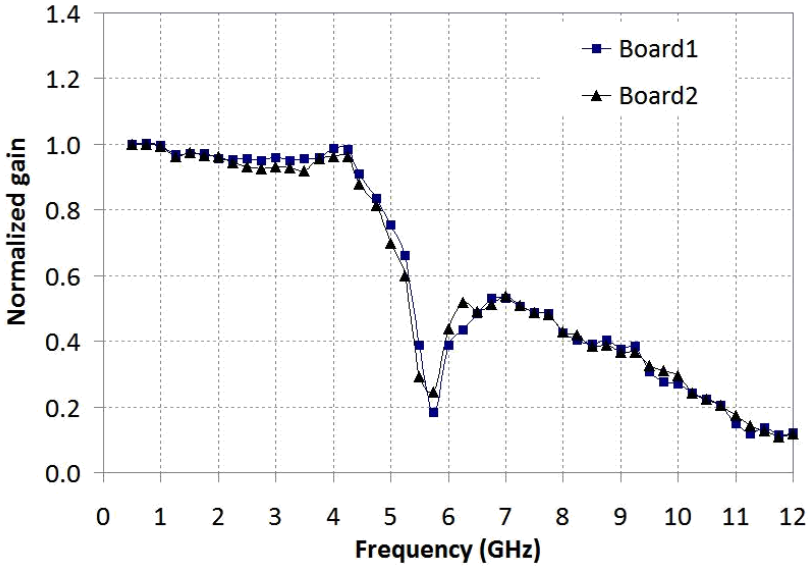


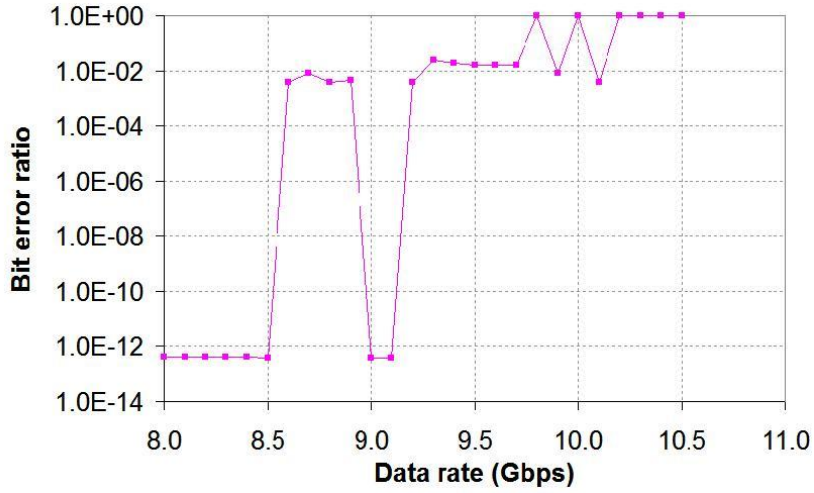
output clock locks to input clock

Optical links for ATLAS Upgrade - CML Driver Performance

- Power: 96 mW at 5 Gbps
- Bandwidth: about 5 GHz
- We single out this driver to study the possibility of a 10 Gbps link. Not yet optimized.







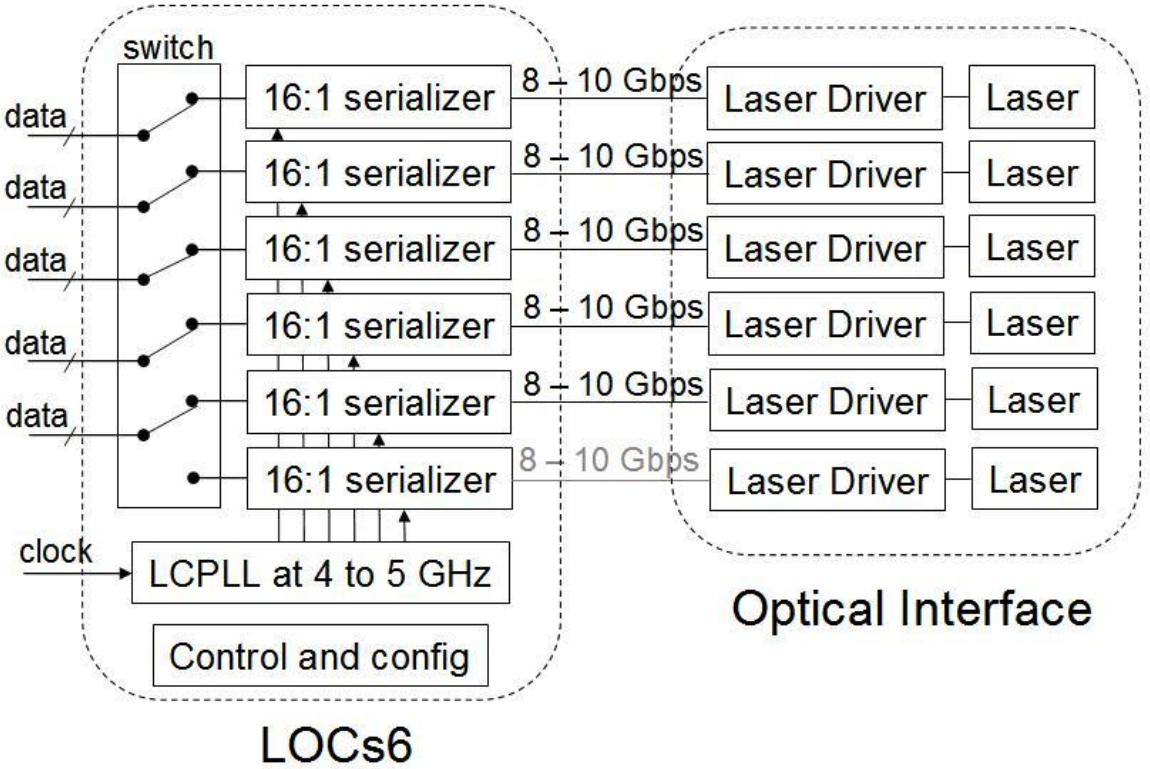
Optical links for ATLAS Upgrade – LOCs1 Proton Test

- Proton beam: 200 MeV at IUCF
- Flux: stepped from 1.3×10^{7} to 1.4×10^{10} proton/cm^2/sec. Fluence: 2.3×10^{14} proton/cm^2, corresponding to 13 Mrad(Si) total dose.
- Two LOCs1 chips inside the beam continue to function throughout the test.
- The maximum change of IDD is around 6% during the irradiation. This increase anneals quickly after the beam is stopped
- No error was observed with flux up to 3.0×10^{9} proton/cm^2/sec.
- When the flux was increased to 1.4×10^{10} proton/cm^2/sec, a few errors occurred which is equivalent to sLHC LAr BER < 6×10^{-18}, or cross section < 7.3×10^{-14} cm^2.

Optical links for ATLAS Upgrade - Future ASIC Work

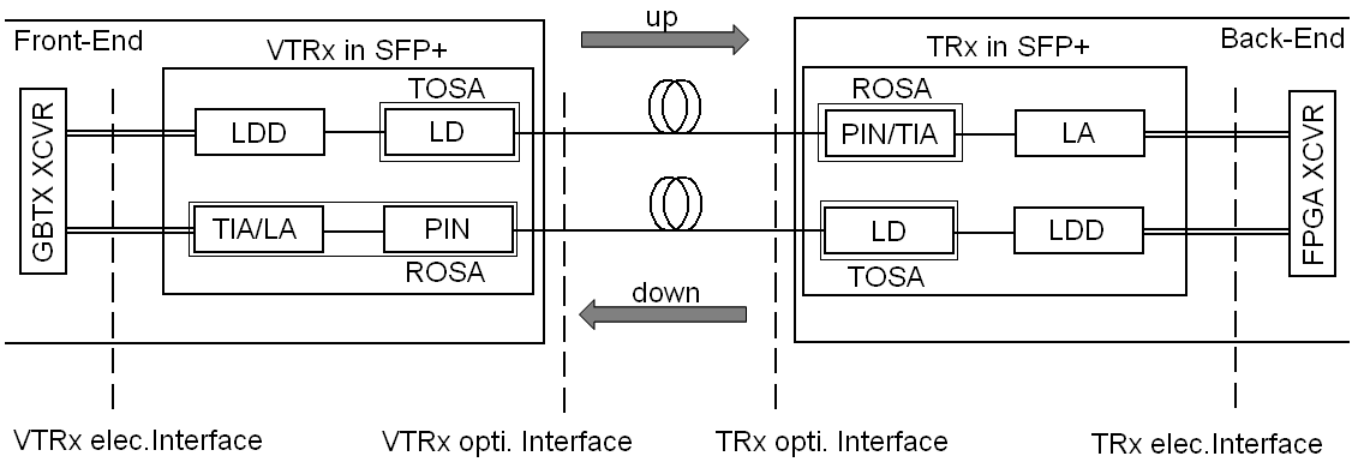
- LOCs6: 6-channel 16:1 serializer operating 8 – 10 Gbps (2010 – 2011)
  - Two serializer chips per FEB with a 12-way fiber ribbon: > 100 Gbps per FEB
  - 20% redundancy
  - Clock sharing to reduce the power consumption
- Laser driver operating at 8 – 10 Gbps
- Multiplexer including low speed multiplexing, encoding and scrambling

Block diagram of optical links for half FEB



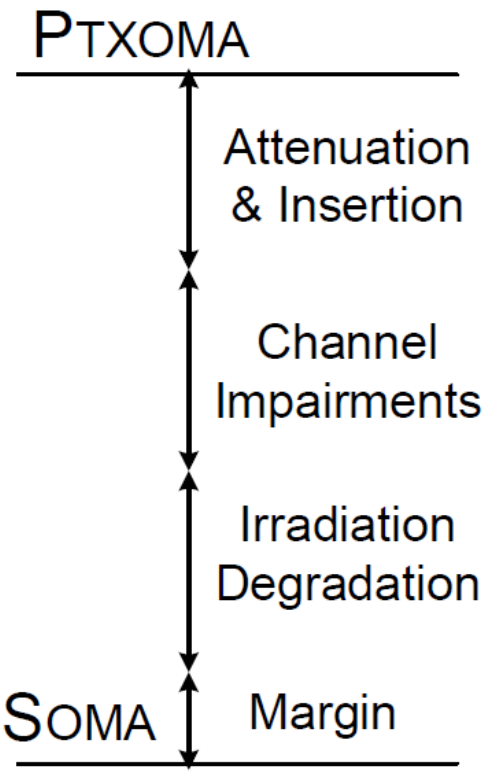
Optical Links for ATLAS Upgrade – Optical Interface Development

- SMU is one of four teams on the ATLAS-CMS common project --- Versatile Link Project
- Under this development:
  - VTRx transceivers operating at 5 Gbps (CERN)
  - Passive components, i.e., fibres, connectors and splitters (Oxford)
  - System specification, prototypes and evaluation platform (SMU)
  - COTS SFP+, parallel optics and high power components for back-end system (Fermi Lab)



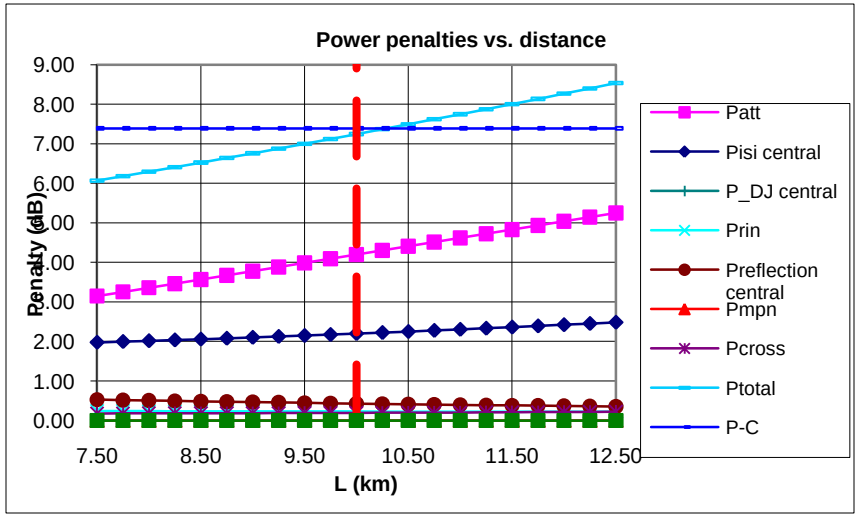
Optical Links for ATLAS Upgrade – System Specification

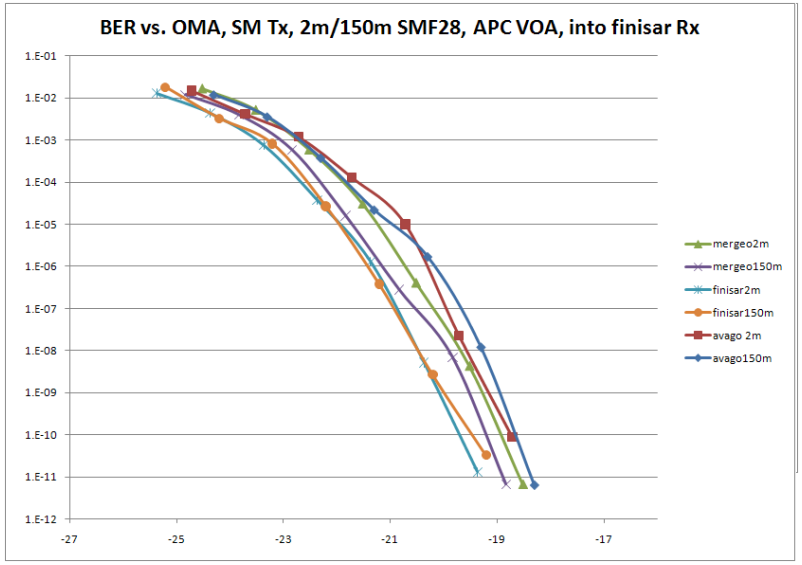
- Versatile Link applications (4.8Gbps, 150 meter) fits the market segments of 10GBASE-SR and 4GFC in both SM and MM configurations.
- At component level, standard specifications apply at interfaces to ensure inter-operability among independently developed components.
- At system level, trade-offs can be made to tolerate the weaker components.
- Power budget calculates losses, link impairments and margins, which vary configuration to configuration.
- On top of that, irradiation degradations also need to be accommodated.



Optical Links for ATLAS Upgrade – System Specification

- A 10GbE link model has been developed by IEEE 802.3ae working group as a tool to facilitate optical physical layer specifications for laser-based links using both SMF and MMF.
- The model assumes Gaussian impulse response for laser and fiber, raised cosine response for receiver; and calculates the vertical eye closure in term of power penalty.
- Apply this model to Versatile Link configuration, power penalty estimates are 1.0dB for MM and 1.5dB for SM.



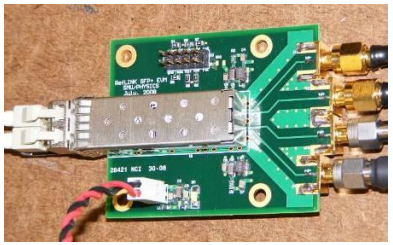


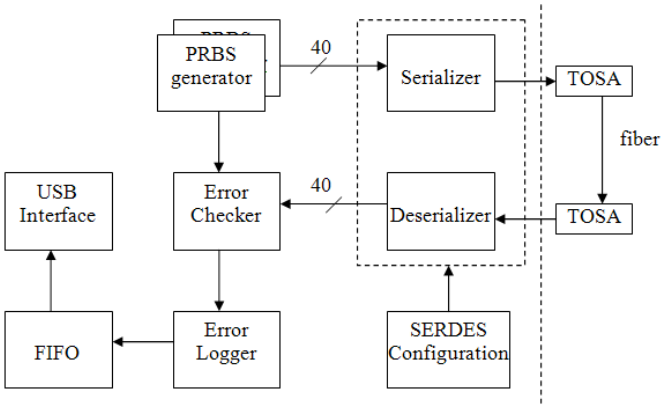
Optical Links for ATLAS Upgrade – System Specification

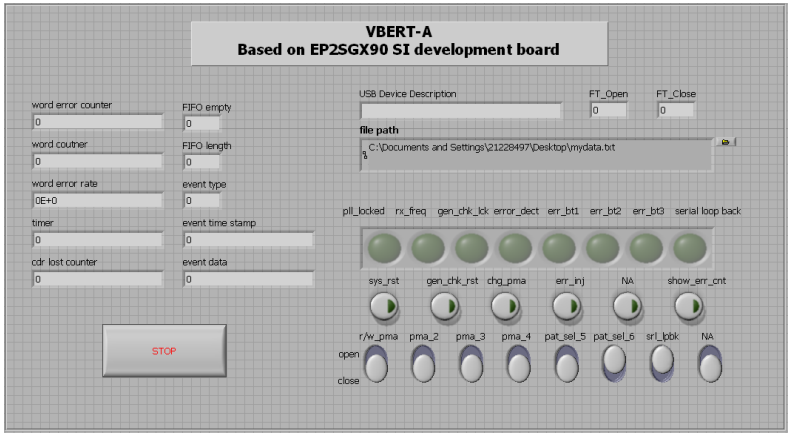
configuration/parameter	(MM) VTx - Rx	(MM) Tx-VRx	(SM) VTx - Rx	(SM) Tx - VRx
Transceiver power level				
Transmit OMA min	-4.0dBm	-2.9dBm	-4.0dBm	-3.4dBm
Receiver sensitivity OMA	-11.1dBm	-14.0dBm	-12.6dBm	-16.0dBm
Power budget (line 2- line 1)	7.1 dB	11.1 dB	8.6 dB	12.6dB
Fiber attenuation	0.6dB	0.6dB	0.1dB	0.1dB
Connection and splice loss	1.5dB	1.5dB	2dB	2dB
Allocation for penalties and margin	5.0 dB	9.0 dB	6.5 dB	10.5 dB
TDP and other penalties	1 dB	1 dB	1.5 dB	1.5 dB
Tx irradiation degradation	-	-	-	-
Rx irradiation degradation	-	7 dB	-	9 dB
Fiber irradiation degradation	1 dB	1 dB	-	-
Safety margin	3.0dB	0dB	5.0dB	0dB

Optical Links for ATLAS Upgrade – Evaluation Platform VBERT

- What is VBERT
  - Evaluation platform for test drive versatile link components and validate system design
  - Currently implemented on Altera Stratix II GX signal integrity development board and in-house SFP+ carrier boards
  - Constitute VHDL and LabVIEW codes
- VBERT release 0.2 functions
  - 4 duplex channel of 5Gbps
  - Un-framed PRBS7, 23,31 transmission
  - Run-time analog setting control
  - Comprehensive error logging with time stamp
  - Bit error rate statistics and link status monitoring







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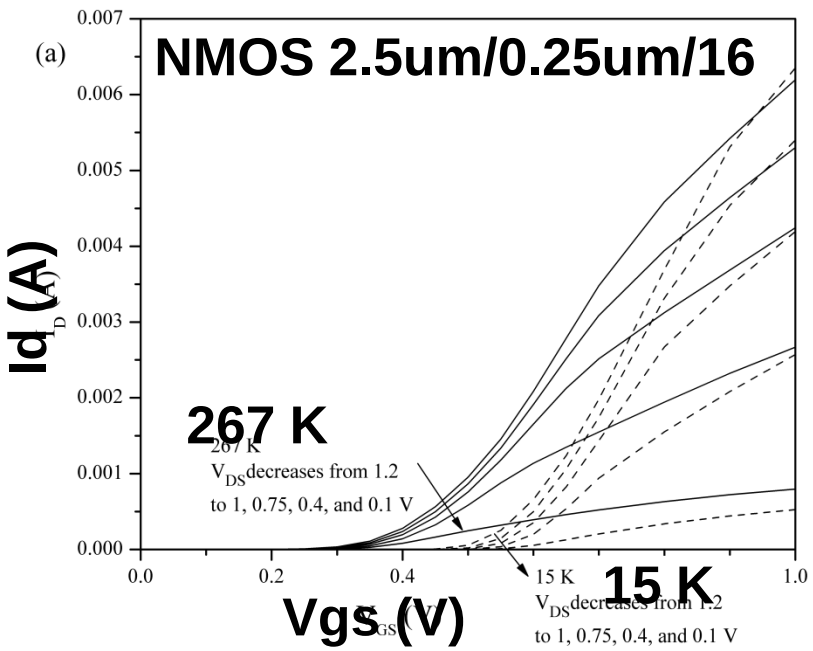
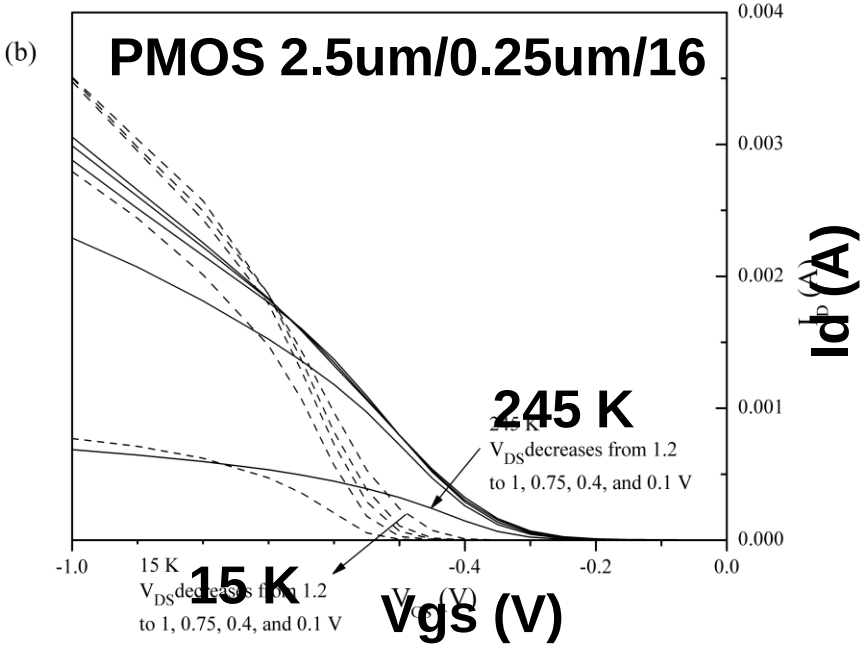
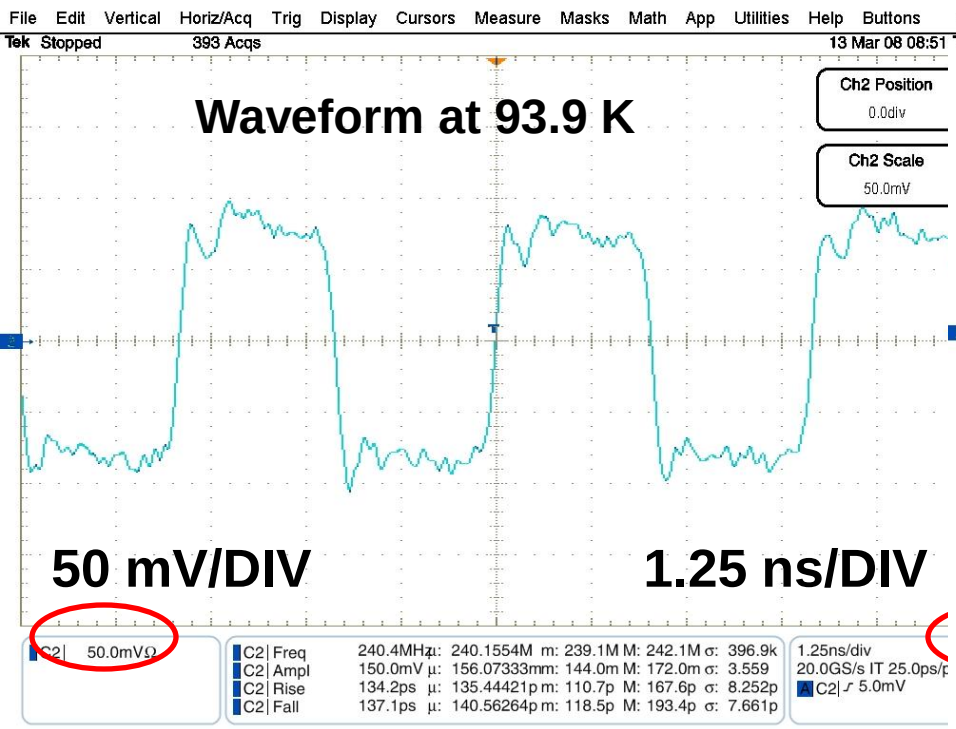
Cryogenic test of optical links – I-V Curves of Transistors

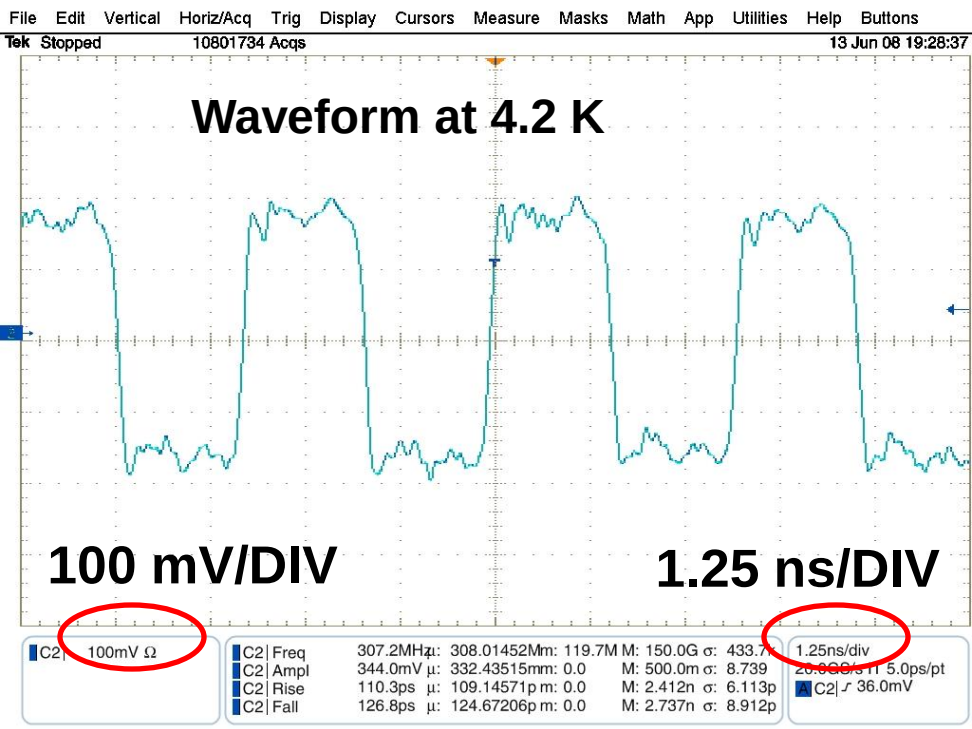
- I_D-V_{GS} curves at 15 K shift and become steeper





Cryogenic test of optical links – Ring Oscillators - Results

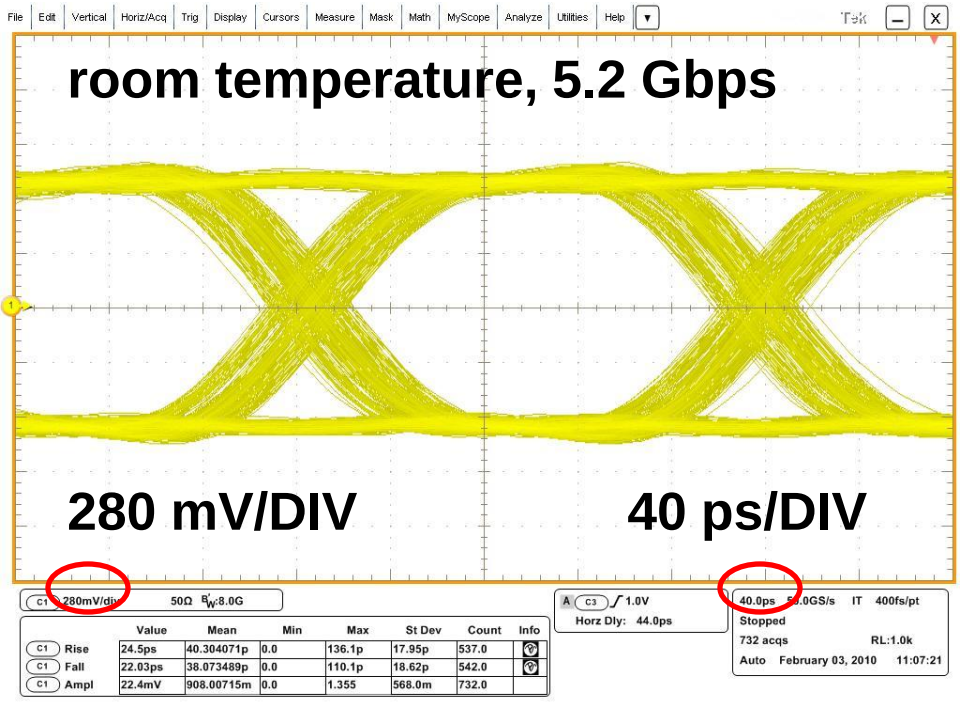


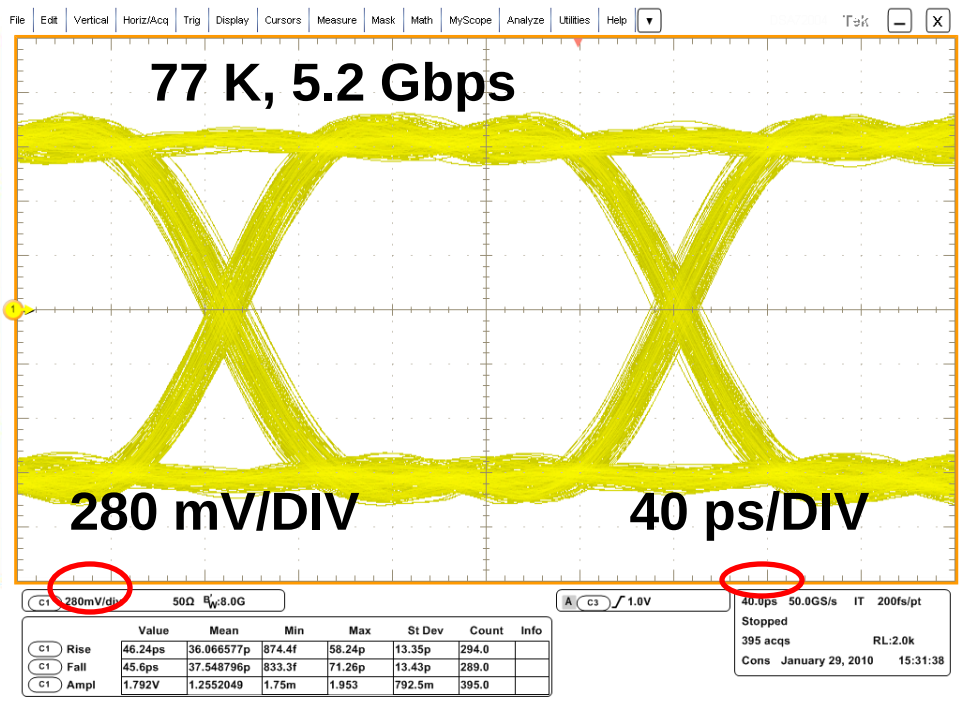


Cryogenic test of optical links – Test of Serializer – Eye Diagrams

When temp decreases

- Amplitude increases
- Jitter decreases



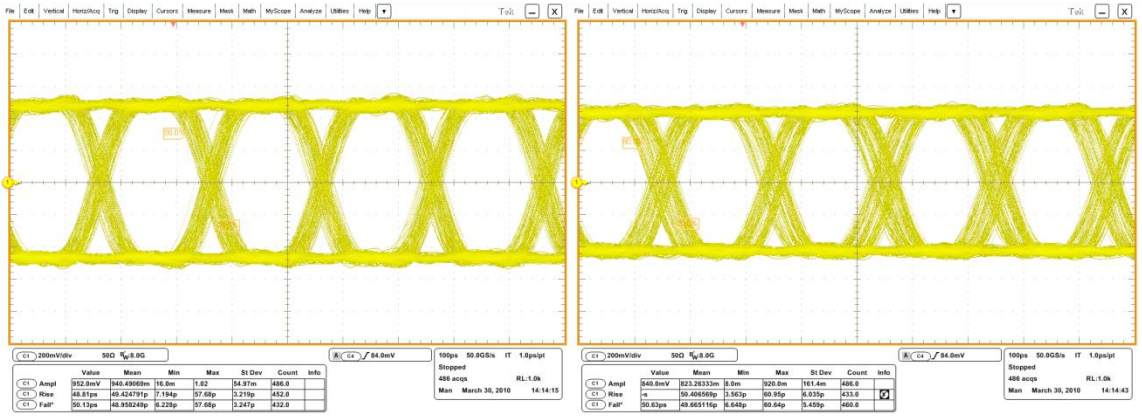


Cryogenic Test of optical links – Serializer - Results

Temperature	Room temperature	77K
Amplitude (pos – neg) (V)	1.26	1.74
Rise time (ps)	54.4	44.0
Fall time (ps)	51.2	44.0
Random jitter RMS (ps)	2.4	1.2
Deterministic jitter pk-pk (ps)	41.0	24.6
Total jitter @ 1E-12 (ps)	65.2	36.2
Eye opening @ 1E-12 (% UI)	66	81
Date rate low limit (Gbps)	3.76	5.10
Date rate high limit (Gbps)	6.00	6.19 (limited by FPGA)

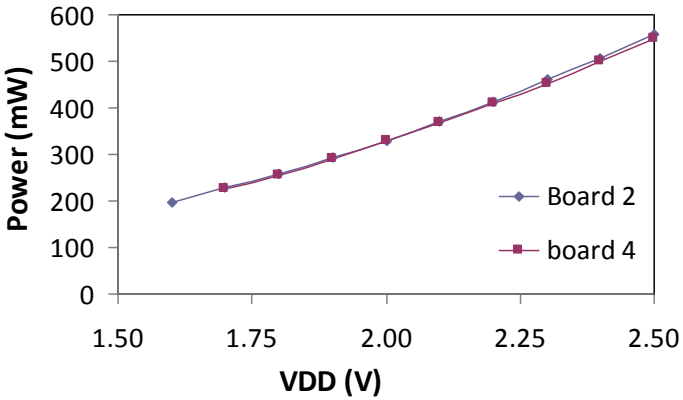
Test results: the 5 Gbps serializer

- At reduced V_{DD} (room-T for now):
  - Suggested by Gianluigi to probe the reliability of the chip.
  - The power supply voltage V_{DD} was lowered from 2.5 V to 1.4 V. The chip functions well with V_{DD} = 1.8 V. Below this the bit error rate goes above 1E-12. The chip stops functioning at all at 1.4 V.
  - At V_{DD} = 2.0 V, power consumption is 300 mW, and can be further reduced.



V_{DD} = 2.0 V

V_{DD} = 1.8 V



- Conclusion on the serializer:
  - This serializer ASIC may be a good candidate for a 5 Gbps optical link operating at LAr temperature.

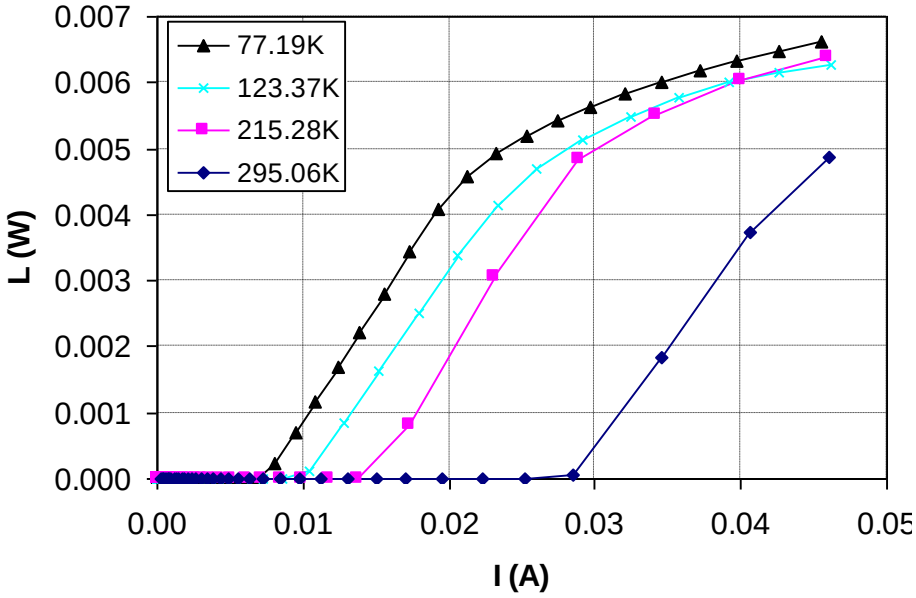
Cryogenic Test of Optical Links – Optical Fibers and connectors

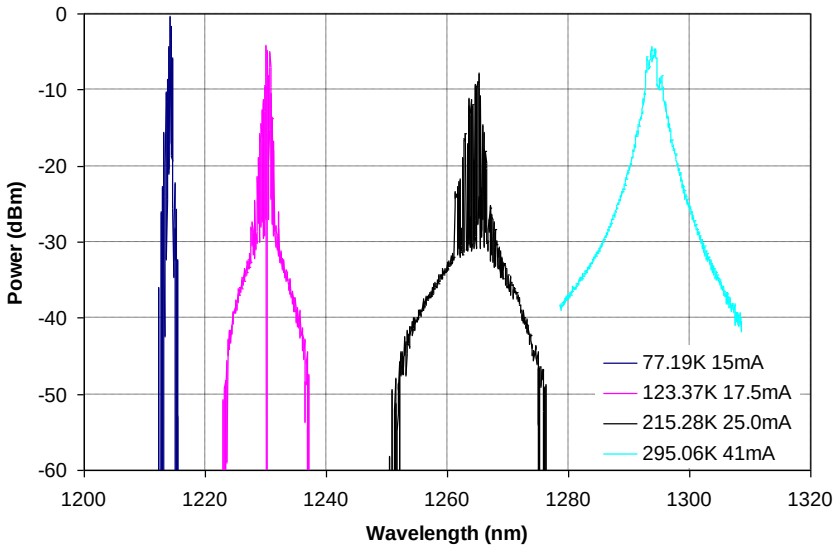
- Fiber and connectors:
  - Two fibers, one single-mode, one multi-mode, are tested at 77 K. Both experience small attenuation increase:
    - SM: 0.005 ± 0.004 (sys) ± 0.002 (meas.) dB/m.
    - MM: 0.034 ± 0.004 (sys) ± 0.015 (meas.) dB/m.
  - LC type connectors, 3 SM, 7 MM, are tested at 77 K. Again both types of connectors experience small attenuation increase:
    - SM: 0.012 ± 0.013 (sys) ± 0.009 (meas.) dB/connector
    - MM: 0.183 ± 0.011 (sys) ± 0.012 (meas.) dB/connector

- Conclusions on them:
  - Given a usual optical power budget in a link system is usually 10 dB or greater, the small attenuation increase in fiber and connector at 77 K can be easily accommodated.

Cryogenic Test of Optical Links – FP Lasers

- Two Fabry-Perot lasers have been tested down to 77K. Both are lasing with acceptable operation conditions.





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Summary

- SMU team took a major role in the development of ATLAS LAr optical links and is making solid progress in the development of optical links for ATLAS upgrade.
- SMU team successfully designed and verified LOCs1 (5Gbps serializer) and is in the process of designing LOCs6 (8-10Gbps array serializers).
- SMU team has proved that major components of optical links can operate at cryogenic temperature