DUNE_DAPHNE_Power

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Power Supply Design

- Board power supply design based on:

  - Mu2E CRV FEB

  - Nexys Video Artix-7 FPGA: Trainer Board

  - Documents available on EDMS

    - DUNE DAPHNE POWER PRESENTATION_5_11_2020.pdf

    - DUNE_DAPHNE_FEB_Schematic_5_14_2020.pdf

    - DAPHNE_Power_5_11_2020.pdf

    - Mu2E_CRV_FEB_Production_Main.pdf

    - nexys_video_schematic.pdf

Power Consumption

- Estimated Board consumption - 26W

- FPGA - 3W

- AFE – 150mW/channel
  - 40 channels -> 6W

Supply (V)	FPGA	Micro	CDR	GTPs	DRAM	Flash	AFEs	ADC	FRAM	Cold Elect	DACs	opamps	Fan	TOTAL (A)	Power (W)
1	3			0.5										3.5	3.5
1.2				0.5										0.5	0.6
1.8	0.2				0.21		3.3	0.5						4.21	7.578
2.5	0.3		0.1											0.4	1
3										0.5				0.5	1.5
3.3	0.5	0.3	0.1			0.2	0.25		0.1					1.45	4.785
5			0.05				0.05				0.05	0.2	0.32	0.67	3.35
10												0.3		0.3	3
-5												0.3		0.3	1.5
													TOTAL POWER		26.813

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Power Distribution Diagram
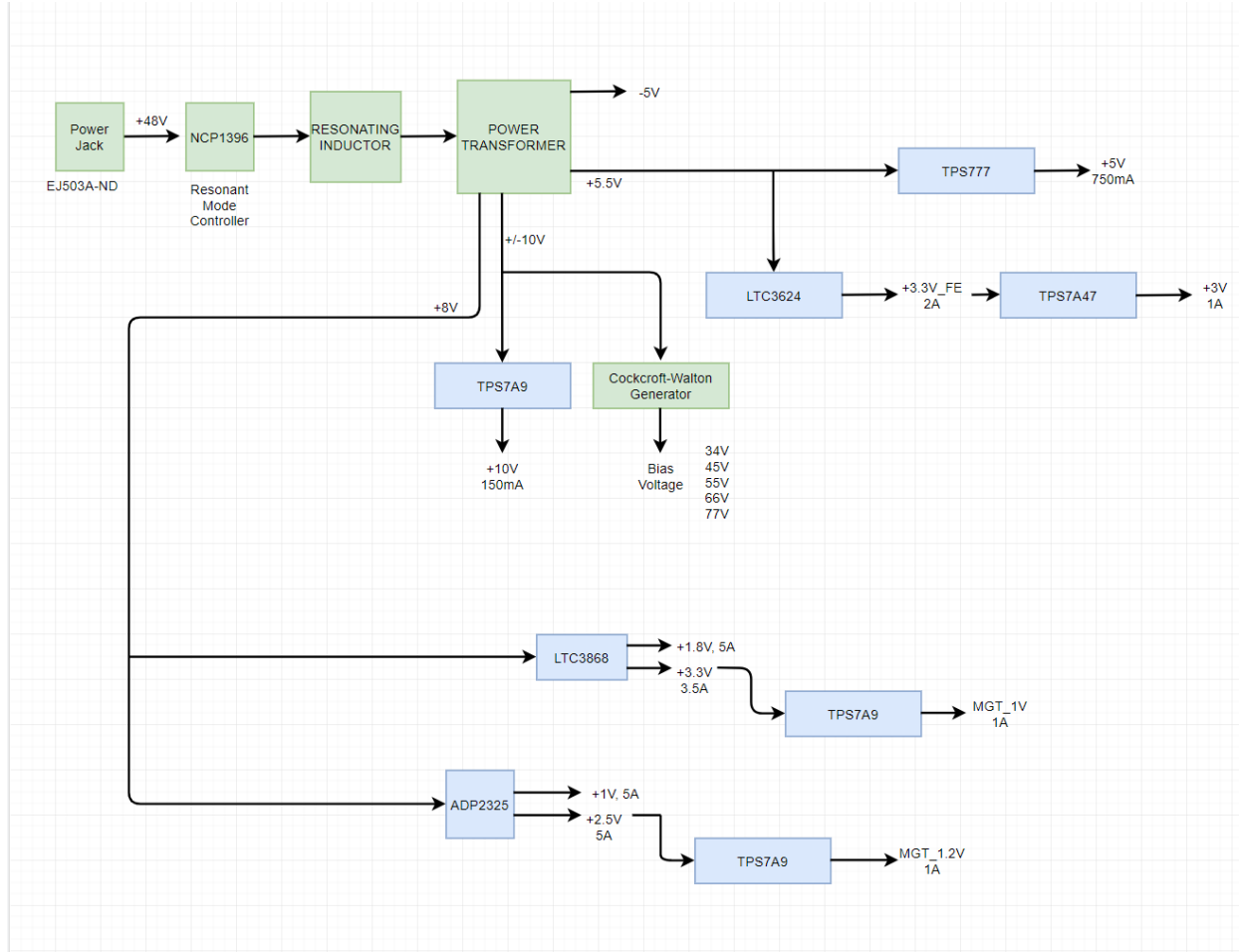
Power Distribution Diagram

- Using Isolated 48V scheme from Mu2E CRV FEB

  - Custom Transformer

    - Lowest coupling between the primary and secondary winding

  - Custom Inductor

   - Optimized for low magnetic losses
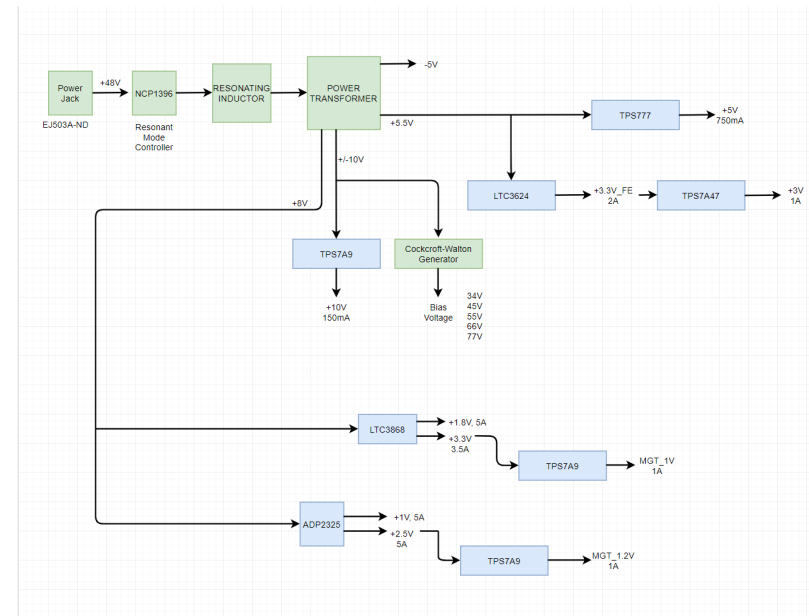
GTP Transceiver

- Artix-7 FPGA GTP Quad requires two analog power supplies:

  - MGTAVCC at a nominal 1.0 VDC

  - MGTAVTT at a nominal 1.2 VDC

- Pins for each of these analog power supplies are tied to a plane in the package

- Low noise requirement of 10mV pk-pk at input of pins

  - Linear Regulators used to reduce noise

  - TPS7A91: Low-Noise LDO Voltage Regulator

    - 4.7 µVrms output noise

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Startup Sequence

- For GTP there is a required power up sequence of :

  - The recommended power-on sequence to achieve minimum current draw for the GTP transceivers is:

  - VCCINT (1V) - Internal Supply Voltage of FGPA

  - VMGTAVCC (different 1V) - Analog Supply for the GTP circuits

  - VMGTAVTT (1.2V) - Analog Supply for the GTP termination circuits

- Other power rails:

  - VCCBRAM (1V) – Supply Voltage for FPGA block RAM memories

  - VCCAUX (1.8V) – FPGA Auxiliary Supply Voltage

  - VCCO (1.8V, 2.5V, 3.3V) – FPGA Output Drivers Supply Voltage For I/O Banks

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Startup Sequence

- Simulation made in LTSPICE
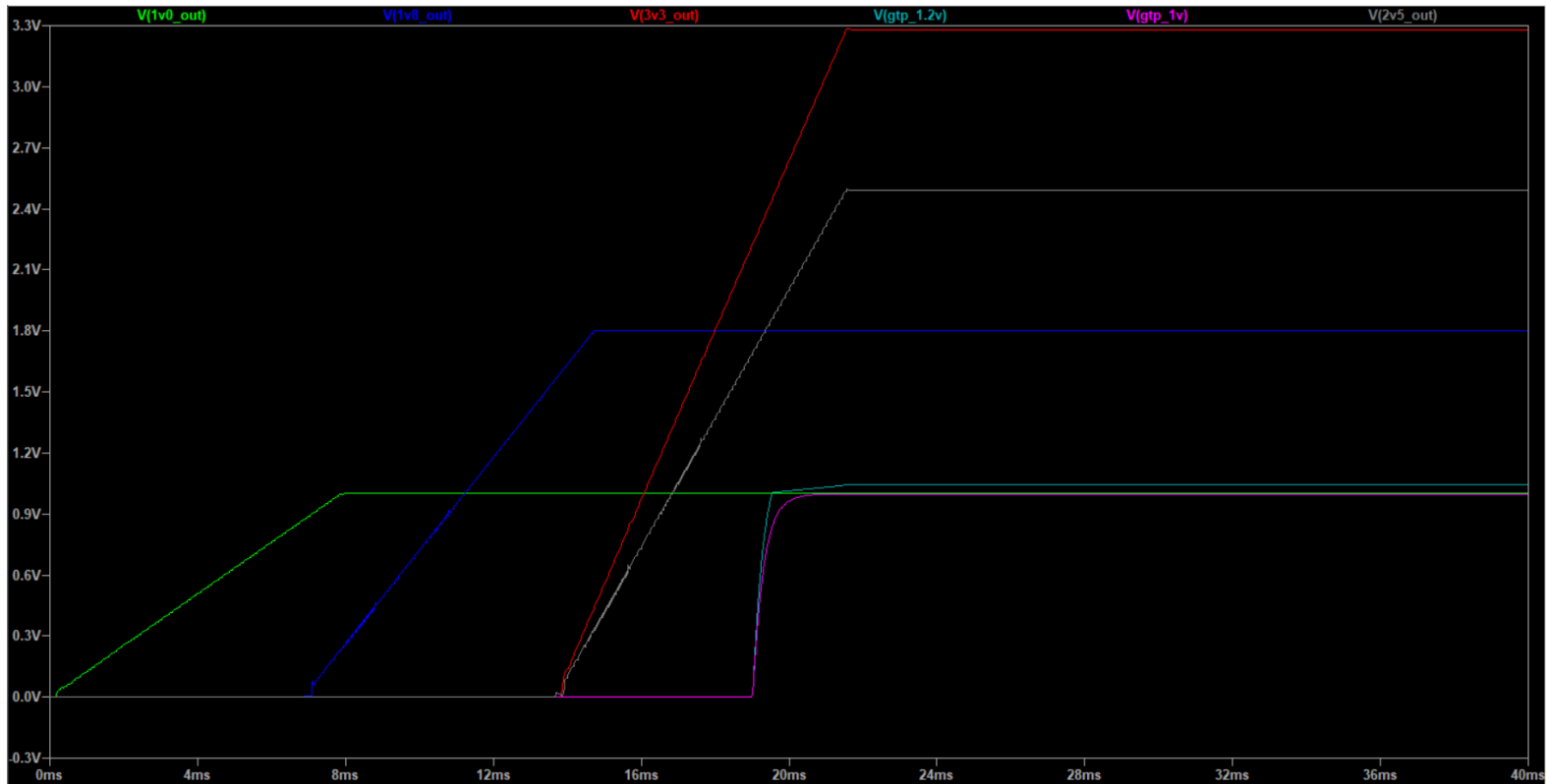
Cooling Fan

- EFB0405VHD-F00 by Delta Electronics

  - brushless axial ball bearing flow 5V fan

  - 3 Pins: +5V, GND, and Frequency Generator (FG)

  - FG produces a square wave signal with a frequency that is proportional to the fan speed

  - signal allows for detection of low supply voltage or blocked airflow

  - life expectancy - 70,000 hours (7.99 years)

In the Works

- Power Supply
  - WIENER MPV8060 8-channel power supplies

- Power connector
  - MOLEX 430450610 and mate
    - Two pins for power (+48v, return)
    - Two pins for sense and return (48v sense, 48v sense return)
    - Two pins for redundant power (48v, return)
    - 6 moderate power conductors in appx 11mm of space

- Power Cable
- Fusing