REPORT ON DAPHNE DEVELOPMENT

GATEWARE AND SOFTWARE

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Outline

Documents prepared for the mini-review

Fundamental ideas

Requirements for DAPHNE

Documents for the mini-review

https://edms.cern.ch/document/2342785/1

- DAPHNE General Report. Late February.
- DAPHNE Firmware - Gateware description.
- DAPHNE Hardware description.
- Cold Interface Document.
- DAPHNE - Flange Cables.

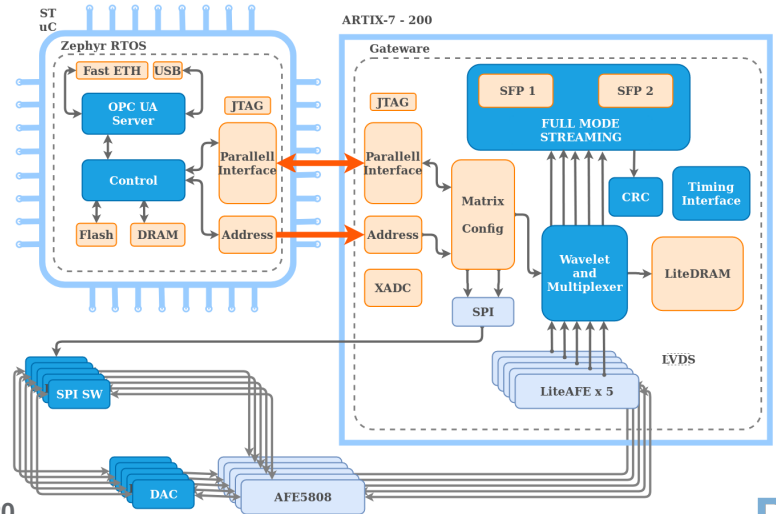
Ideas to understand documentation

- It is not an upgrade.
- We are working with RTL automatized output.
- We are implementing gateware and firmware that will not be used in DUNE.

Requirements for DAPHNE - on the paper

- 14 bit resolution.
- 62.5 MSPS.
- 40 channel granularity.
- Low dark noise rate.
- Power support for the cold electronics.

Block diagram



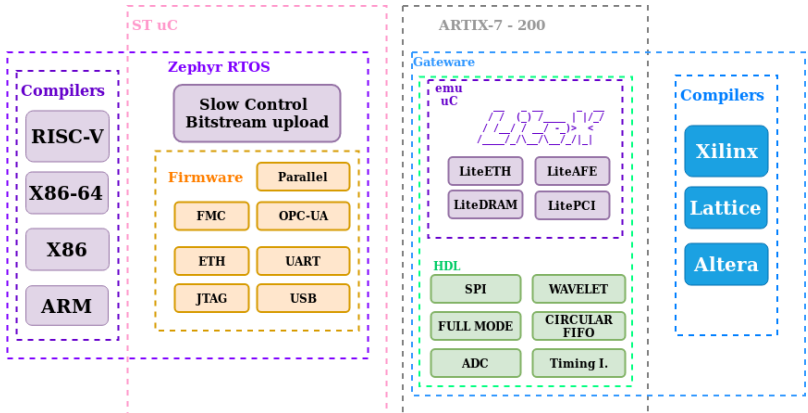
Status of the development

We need to prepare to use the Vivado transceiver debugger.

- AFE Not yet able to test the link
- Gb ETH Gb ETH over PHY SFP
- RAM (Checked with both packages)
- CRC (Clock Recovery Circuit for the inner use)
- SPI (All DACs, AFES, and ADC use it)
- SoC has been tested.


DEEP UNDERGROUND
NEUTRINO EXPERIMENT

Support


ST uC
Zephyr RTOS
Compilers
RISC-V
X86-64
X86
ARM
Slow Control
Bitstream upload
Firmware
Parallel
FMC
OPC-UA
ETH
UART
JTAG
USB
ARTIX-7 - 200
Gateware
emu
uC
LiteETH
LiteAFE
LiteDRAM
LitePCI
HDL
SPI
WAVELET
FULL MODE
CIRCULAR
FIFO
ADC
Timing I.
Compilers
Xilinx
Lattice
Altera

Wavelet and zero suppression