DAPHNE documentation

Deywis Moreno L. on behalf of the warm electronic group

DAPHNE Mini Review Kick-off

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DAPHNE document repository

- EDMS schematics and documentation available in: https://edms.cern.ch/document/2342785/1

- In following there is a brief description of the documents available in the mentioned folder

- The work that this documentation support have contributions for different groups.

- Special thanks to Sten Hansen

DAPHNE DAQ/Interface

- DAQ-Slow Control/PDS interface document available in: https://edms.cern.ch/document/2088726/2
- Document setting the agreements between DAQ consortium and PDS

DAPHNE_Overview

- Description of DAPHNE physical requirements that guided the DAPHNE design
- The DAPHNE Interfaces are described in detail in this document
- Main authors:
  - Matt Toups (toups@fnal.gov)
  - Deywis Moreno (deymoreno@uan.edu.co)
  - Javier Castano (jfcastanof@uan.edu.co)
  - Manuel Arroyave (matheos.mc2@gmail.com)
  - Miguel Marchan (marchan@fnal.gov)

DAPHNE_Hardware_description

- Hardware description of the DAPHNE front-end board.
- The DAPHNE schematic design is presented in individual sections.
- The document presents technical aspects of the hardware design and detailed description of each functional device and connections
- Main authors:
  - Javier Castano (jfcastanof@uan.edu.co)
  - Miguel Marchan (marchan@fnal.gov)
  - Manuel Arroyave (matheos.mc2@gmail.com)
  - Juan Vega (jvega@conida.gob.pe)

DAPHNE_DUNE_DAPHNE_FEB_Schematic_5_14_2020

- Updated version of DAPHNE Schematic
- Main authors:
  - Javier Castano (jfcastanof@uan.edu.co)
  - Miguel Marchan (marchan@fnal.gov)
  - Manuel Arroyave (matheos.mc2@gmail.com)

DAPHNE_Firmeware_-_Gateware_description

- Firmware/Gateware description of the DAPHNE front-end board
- Main aspects of DAPHNE design are presented and related with the physical requirements.
- Main authors:
  - Javier Castano (jfcastanof@uan.edu.co)
  - Manuel Arroyave (matheos.mc2@gmail.com)
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Cold_Warm_PDS_Interface_4_27_2020.pdf

- This document describes the interface between the Sing
  Phase Photodetector System (PDS) front-end board.
- Components and requirements that the interface should
  accomplish is described
- Main authors:
  - Javier Castano (jfcastanof@uan.edu.co)
  - Manuel Arroyave (matheos.mc2@gmail.com)
  - Claudio Gotti (claudio.gotti@unimib.it)

Photon_Detector_Cable_Harness_Document_Rev_5.pdf

- A description of cable connecting the cold electronics and DAPHNE
- A scheme of the grounding can be find in this document
- Main authors:
  - Dave Warner (david.Warner@colostate.edu)
  - Claudio Gotti (claudio.gotti@unimib.it)
  - Matt Toups (toups@fnal.gov)

DAPHNE_Power

- DAPHNE Power consumption, voltage regulator and voltage requirements and startup FPGA
- Main authors:
  - Miguel Marchan (marchan@fnal.gov)

Additional documentation in the EDMS

- nexys_video_schematic.pdf
- Mu2E_CRV_FEB_Production_Main.pdf
- DAPHNE_BOM_FEB2020.xlsx
- DUNE_DAPHNE_Review_Requirements-4.pdf
- DUNE_DAPHNE_POWER_PRESENTATION_5_11_2020.pdf