Engineering Note

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Project: Microboone PMT to Laser PS Interlock System
Doc. No: B060514PMT_Laser_Inltk

Subject: Microboone PMT High Voltage to Laser Power Supply Interlock design specifications.

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Introduction:

The calibration system for the Microboone experiment consists of a Continuum I-10 UV Laser and associated electronics. Laser light is introduced into the cryostat during a Calibration run. The PhotoMultiplier Tube (PMT) system is also housed inside the cryostat. Light emitted from the Laser can damage the PMT system if high voltage is applied to the PMT tubes while a calibration run is being conducted. This document identifies the requirements of an interlock system design which prevents damage to the PMT system during Laser calibration runs.

PMT System Safety Interlock Requirements:

While the BiRA High Voltage system is providing power to the PMTs, the Laser Calibration system may not be activated. This is accomplished by modifying the BiRA High Voltage Mother boards such that they provide a status indication of the state of a given channel. This status signal will be logically ORed for each of the eight channels on a given mother board. There are six mother boards in the crate. Another logical OR of the six mother boards is used to drive a dry contact relay providing the appropriate condition to the Laser Power Interlock Loop input, labeled External on the Laser power supply.

The PMT bases can fail if operated in gaseous argon. Therefore, an interlock indicating that the liquid argon level is of such a height that the bases are completely submerged is required by the PMT system. The liquid level status is provided to the Mother Board Level backplane interlock, labeled INT2.

Discharges from the field cage to ground cause significant amounts of light in the cryostat. It may be possible to diagnose pre-cursors to these discharges by monitoring fluctuations in the Drift High voltage power supply current. If a device is built to spot these discharges before they happen, they should activate an interlock signal that can be used to shut off the PMT HV at the Mother board level. Provisions for a Drift High Voltage interlock is logically ANDed with the liquid level status.

The Trig/PMT crate in the Trig/PMT rack is interlocked to the temperature of the ambient air within the rack. The PMT High Voltage crate should also be powered off in the event of an over-temperature indication of the Mother boards within the BiRA crate. This interlock is at the crate level using the interlock input to the Lambda power supply. The temperature interlock is provided by the Slow Control chassis within the rack and is not a part of this Interlock chassis design.

A block diagram of the system connections is shown in Figure 1.

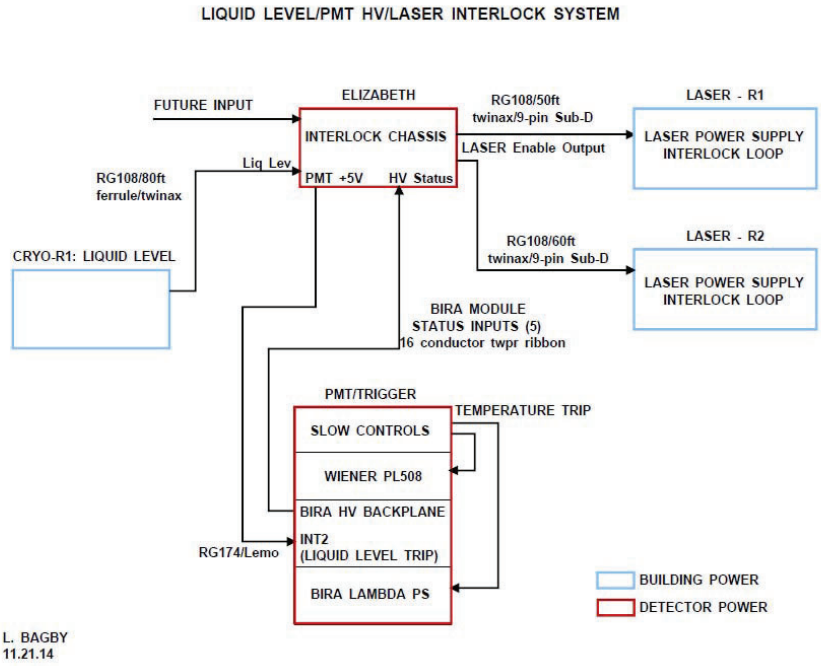

Figure 1: Interlock Block Diagram

Design Requirements:

The interlock will

1. Inhibit the Laser power supply while the PMT high voltage is applied to the bases.

2. Deactivate PMT high voltage if

a. the LAr liquid level falls below a specified threshold.

b. the Drift high voltage power supply experiences current fluctuations indicative of an imminent spark condition. (This is considered a future feature.)

Interfacing Specifications:

Laser Input Details

The Laser Power supply has a front panel interlock input, labeled EXTERNAL, via a 9-Pin Sub D female plug connector. The interlock uses pins 1 and 9. +5 volts is provided on pin 9 and returned on pin 1, Figure 2. The power supply requires a CLOSED contact connection between these two pins to operate when the interlock is activated. An OPEN contact disables the power supply. The Laser rack electronics are powered from the Building side of the experiment. This requires that the contacts from the interlock are dry and the cable used should not have the shield connected at the Laser end of the cable.

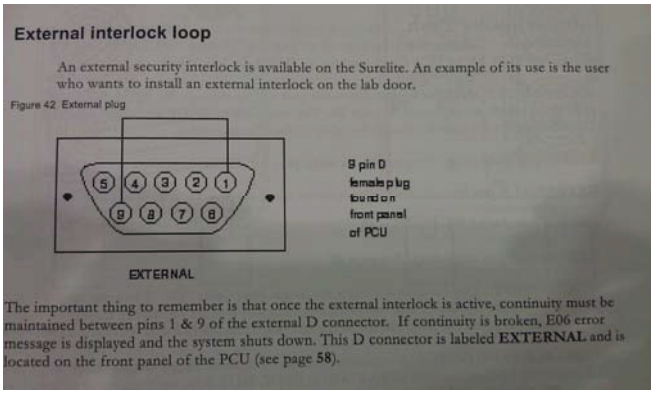

Figure 2: Laser Power Supply Interlock Input

Liquid Level Input Details

(Mike Sarychev)

The cryostat has two identical Liquid Argon level probes – LT124 and LT125, located at both ends of the cryostat. They are AMI capacitive 3/8" O.D. probes, connected to PLCs trough AMI model 175 4-20 mA level transmitters. LT124 is connected to Siemens S7 PLC and LT125 to Siemens S7 Fail Safe PLC. The normal operating Argon level will be between 4" and 5". Both PLCs are programmed to drop the interlock if liquid Argon level drops below 2". Safe S7 PLC digital output (Rail 11 slot 5 channel 0) provides 24 VDC signal that passes through Main S7 PLC relay contact output (Cab 3 term. 208) and operates coils of HV INTLK RELAY 1 and HV INTLK RELAY 2, installed in the cryo relay rack 1 (CRYO-R1) on the platform. Normal Open contacts 5 and 9 of both relays are used for HV interlocks. If LT125 drops below 2", 24 VDC from Safe S7 will turn off; if LT124 drops below 2", relay output contacts will open. In both cases HV INTLK RELAY 1 and HV INTLK RELAY 2 coils will be de-energized, that will open contacts 5 and 9, dropping the interlocks.

The closed contact leads are sent to the Interlock Chassis via a rear panel RG108 twinax connector. As long as the liquid level is within operating parameters, a +5V signal is provide to the INT2 interlock input located on the rear panel, right side, of the BiRa HV crate backplane. If power is lost or either of the cables from the Alarm module to the Interlock Chassis or Interlock Chassis to the BiRa HV crate is disconnected, the interlock is dropped and the high voltage output power is removed from the PMT load, Figure 3.

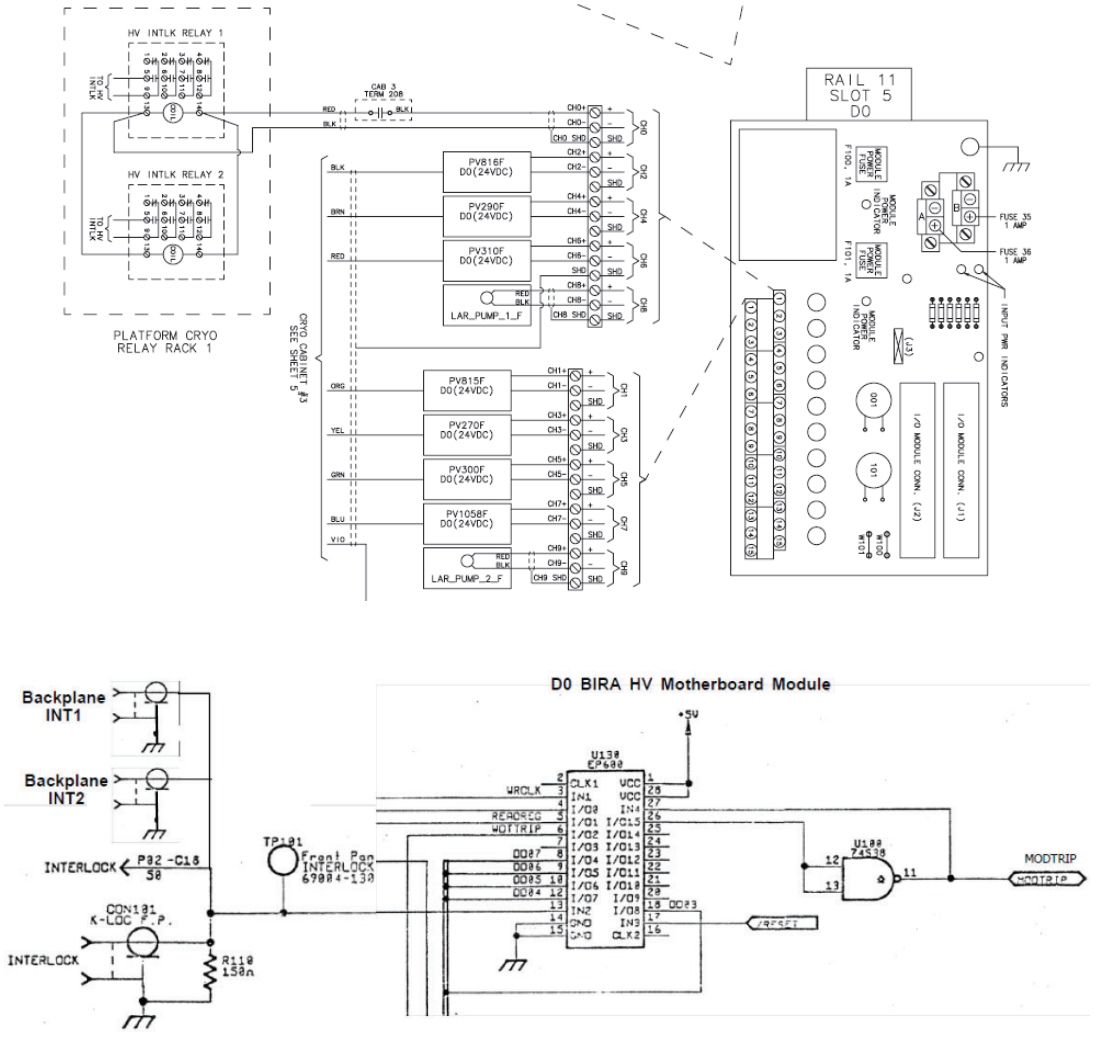

Figure 3: AMI Liquid Level fail-safe Alarm module circuit and BiRa HV crate external interlock circuitry.

Drift High Voltage Current Fluctuation Input Details

Provisions for a Drift High Voltage dry contact input is incorporated into the design by duplicating the circuit for the liquid level and wiring a second set of dry contacts in series with the liquid level contacts. If the interlock is dropped, the LED front panel indicators for both relays will display which input has failed.

BiRa HV Mother board Modification Details:

Eight 28AWG jumper wires are added to the Mother boards to bring the status of a channel to the backplane connector. Figure 4 shows the schematic location of the modification for Channel 0, JHV0D, Pin 6.

. Figure 5 illustrates the connection point of the wires for all channels on a Mother Board.

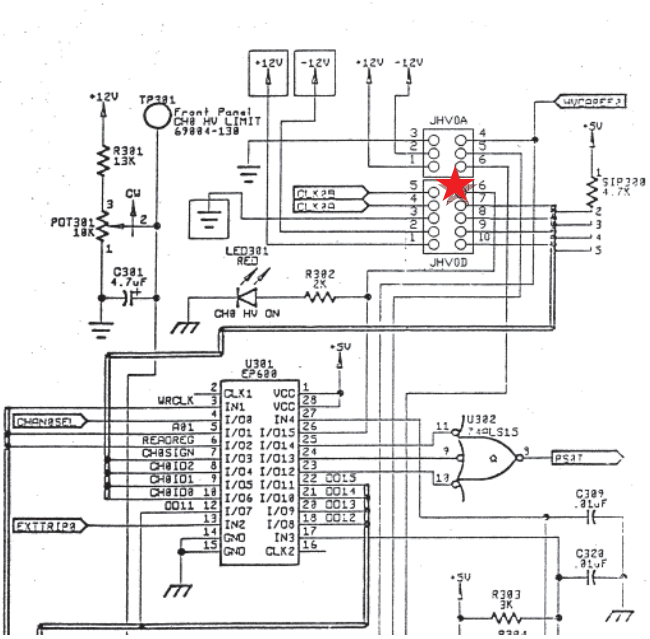

Figure 4: Schematic location of modification wire for channel 0 on JHV0D, Pin 6.

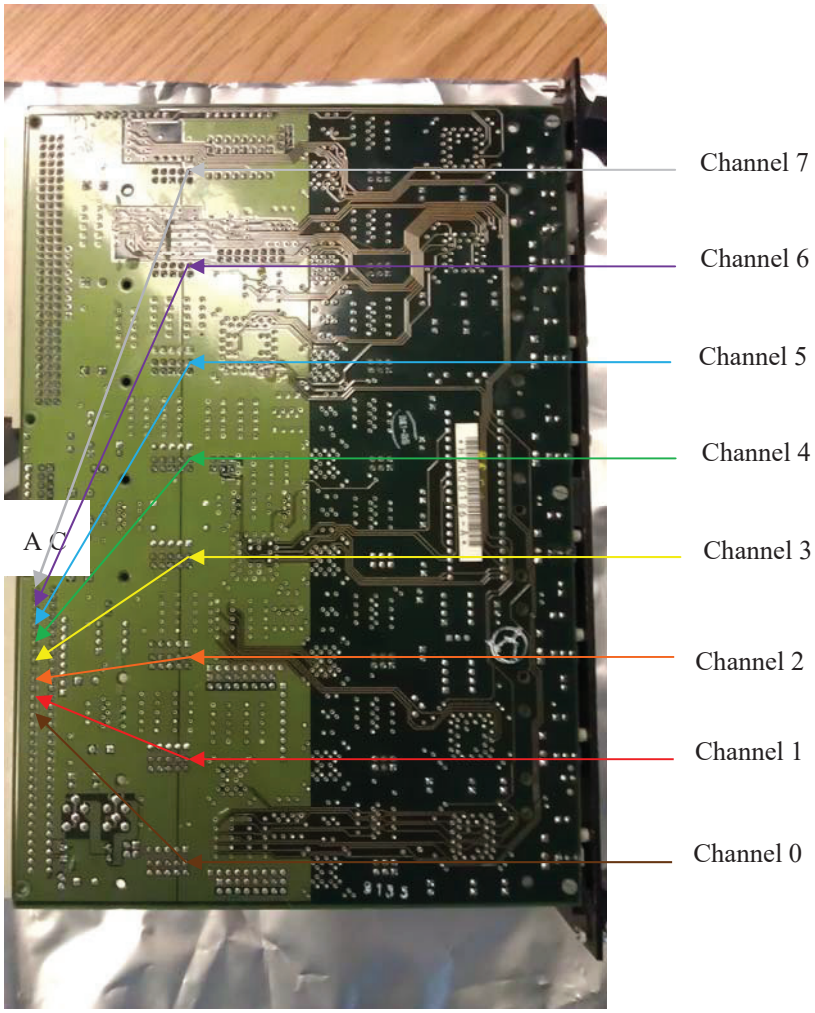

Figure 5: Modification wires on Mother board from JHVxD, Pin 6 to P02, various pins.

An interfacing cable is connected to the J4, 7, 10, 13, 16, 19 backplane connectors, which mates to Mother Board P02 connectors, and brings the status signals into the Interlock Chassis. A list of the spare pins is listed below, Figure 6. The modification uses the P02-A row spare pins. Row C pins are readily available from the component side of the board, Figure 7. However, Row A pins must be used because of spare pin availability so wires will be connected on the back side of the board.

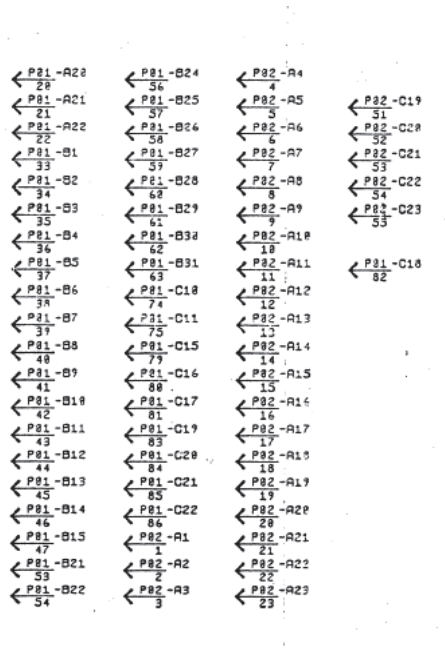

Figure 6: Mother board Spare Pins

Figure 7: P02 Connector, C Row visible

Figure 8 shows the J connector pinout numbering scheme as viewed from the rear of the crate. Black dots indicate the spare pins used and the channel assignments. A 16 pin header board is used to interface between the Mother board backplane and the Interlock chassis. Figure 9 shows the backplane connector.

	AS VIEWED FROM BOTTOM OF BOARD				
Signal	A	P02 on schematics		C	Return
Channel 7	A1 ●	1	33	C1	
	A2	2	34	C2	
Channel 6	A3 ●	3	35	C3	
	A4	4	36	C4	DGND
Channel 5	A5 ●	5	37	C5	
	A6	6	38	C6	
Channel 4	A7 ●	7	39	C7	
	A8	8	40	C8	
Channel 3	A9 ●	9	41	C9	
	A10	10	42	C10	
Channel 2	A11 ●	11	43	C11	
	A12	12	44	C12	
Channel 1	A13 ●	13	45	C13	DGND
	A14	14	46	C14	
Channel 0	A15 ●	15	47	C15	DGND
	A16	16	48	C16	
	A17	17	49	C17	DGND
	A18	18	50	C18	
	A19	19	51	C19	
	A20	20	52	C20	
	A21	21	53	C21	
	A22	22	54	C22	
	A23	23	55	C23	
	A24	24	56	C24	
	A25	25	57	C25	
	A26	26	58	C26	
	A27	27	59	C27	
	A28	28	60	C28	
	A29	29	61	C29	
	A30	30	62	C30	
	A31	31	63	C31	
	A32	32	64	C32	

Figure 8: Jx Pinout Modification Assignments

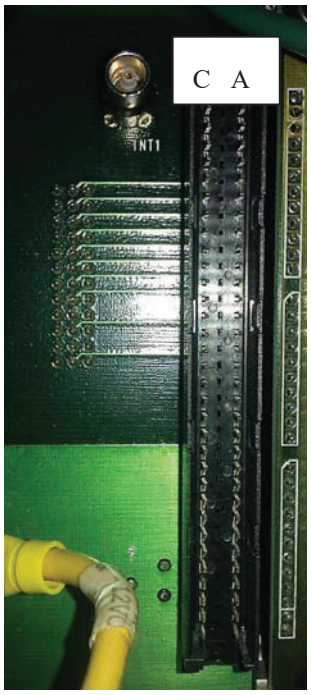

Figure 9: Backplane Jx Connector

System Interconnects:

Header Board

Figure 10 illustrates the header board. The 64 pin DIN, 41612 PL 96, connector plugs directly into the backplane. A 16 pin twisted pair ribbon interfaces from the Header board to the Interlock chassis. The DIN connector is manufactured by Harting, PN:09732646801. Pins are rated at 2A. The 16 pin header is manufactured by 3M, PN:N3408-6303RB. The mate is PN MKC16A, with strain relief, MKSR16.

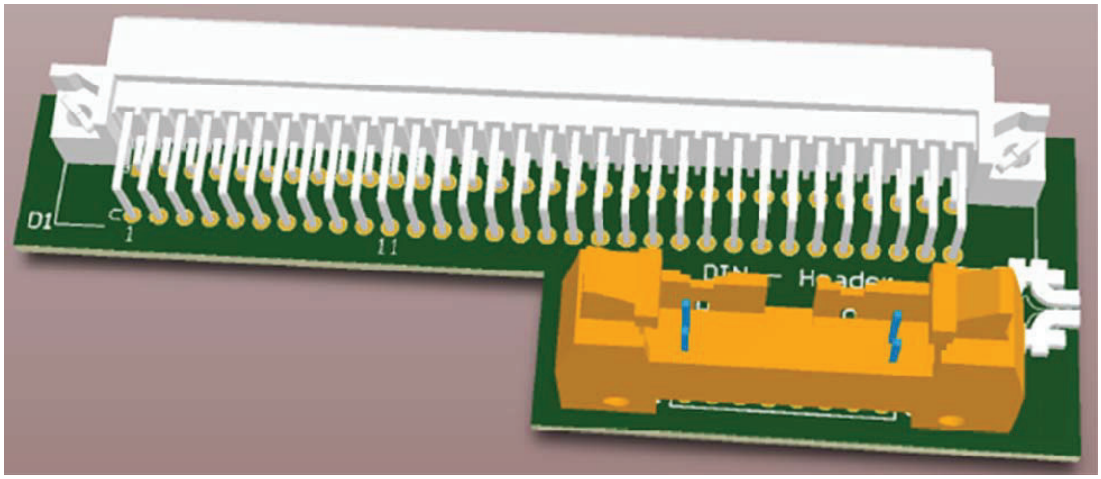

Figure 10: DIN to twist and flat header

Interface cabling

The twist and flat cable is manufactured by 3M, PN:1700/16 100SF, Digikey PN:MC16F-100. The conductors are 28AWG. Figure 11.

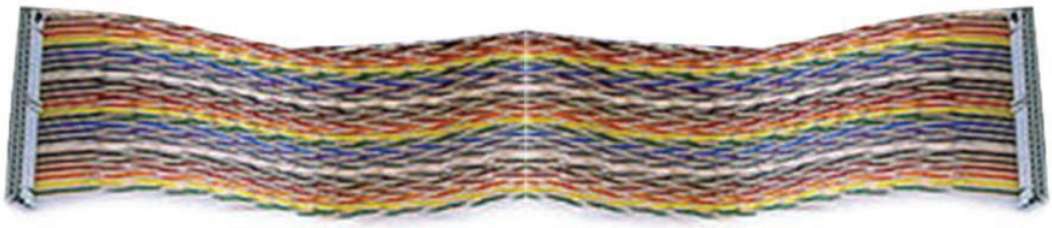

Figure 11: 16 conductor twist and flat jumper example used from crate backplane to Interlock chassis.

The Interlock Chassis has three RG108 interface cables, Figure 12. The Liquid Level input into the Interlock Chassis, Liq. Lel., is terminated with a twinax on the Interlock chassis end and ferrules for the Cryo-R1 rack dry contact compression termination. The input to the chassis is from a set of dry contacts. The Interface chassis presents 12V on the socket side of the twinax rear panel connector. The Laser-R1/R2 RG108 cable to the Interlock chassis presents +5V on the socket side of the twinax from a 9-Pin SUB-D connector. A dry contact within the Interlock chassis completes the circuit. The cable shield is connected at the Interlock chassis rear panel.

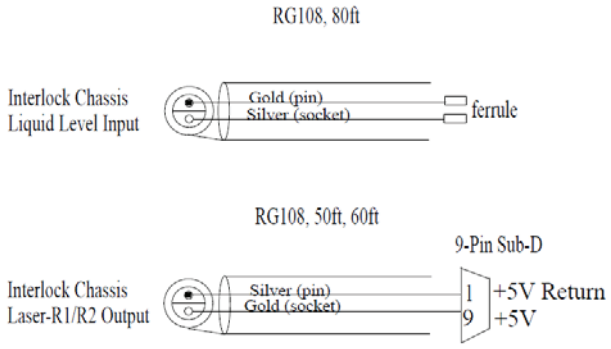

Figure12: RG108 Interlock cabling.