DUNE Far Detector SP Timing System Custom Hardware FDR

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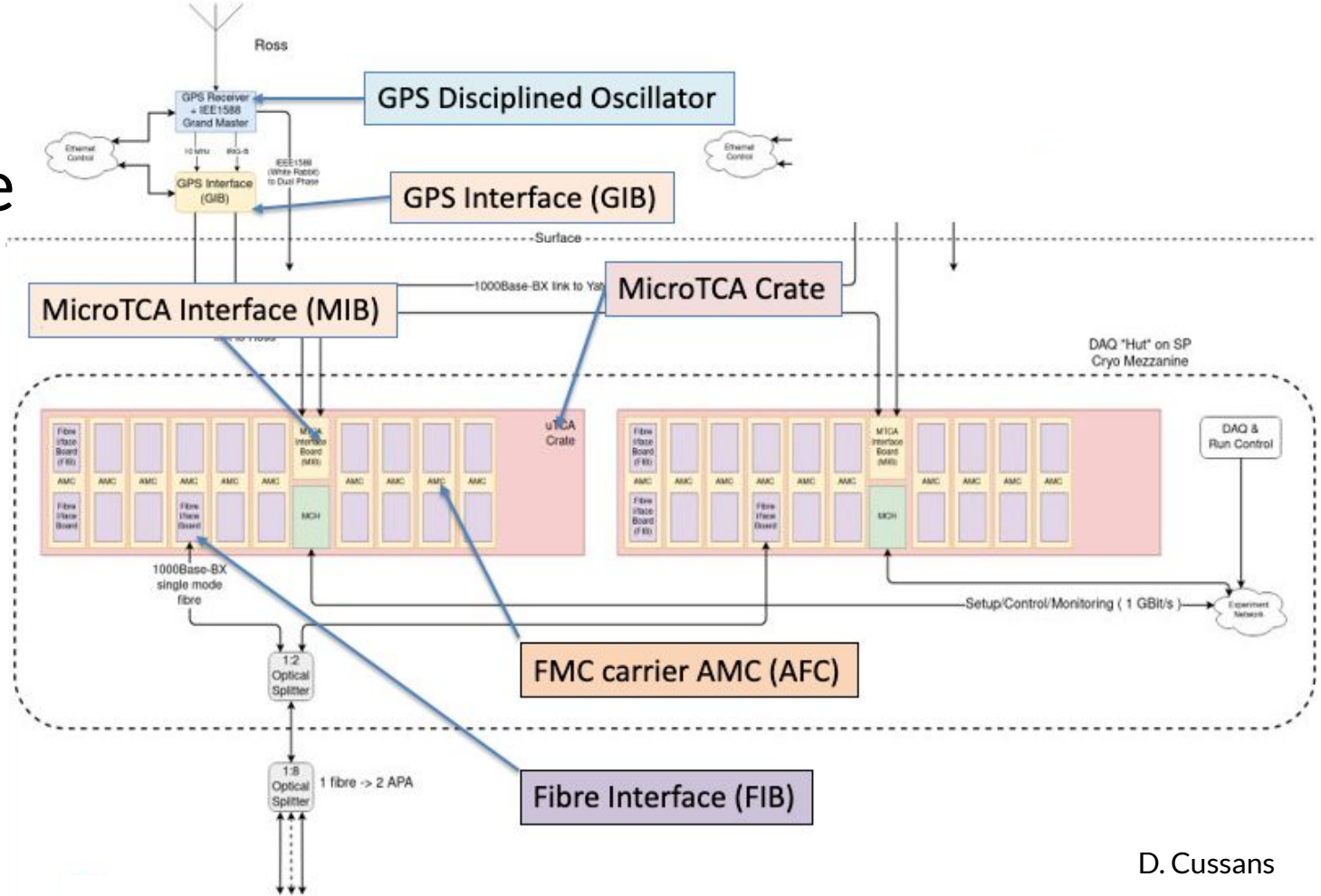
July 21, 2020

Outline

- Brief Timing System Overview
- GPS Interface Board (GIB)
- MicroTCA Interface Board (MIB)
- Fiber Interface Board (FIB)

Timing System Big Picture

- Redundant GPS and GIB on surface.
- MicroTCA, MIB and FIB in cavern on Cryo Mezzanine.



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Timing System: 3 Custom Boards

- **GPS Interface Board (GIB)**

  - Clock and timecodes from GPS receiver

  - Generate DUNE SP timing system timestamp

  - Transmit to MIB using the timing system protocol

- **MicroTCA Interface Board (MIB)**

  - Receive timing data-stream from GIB

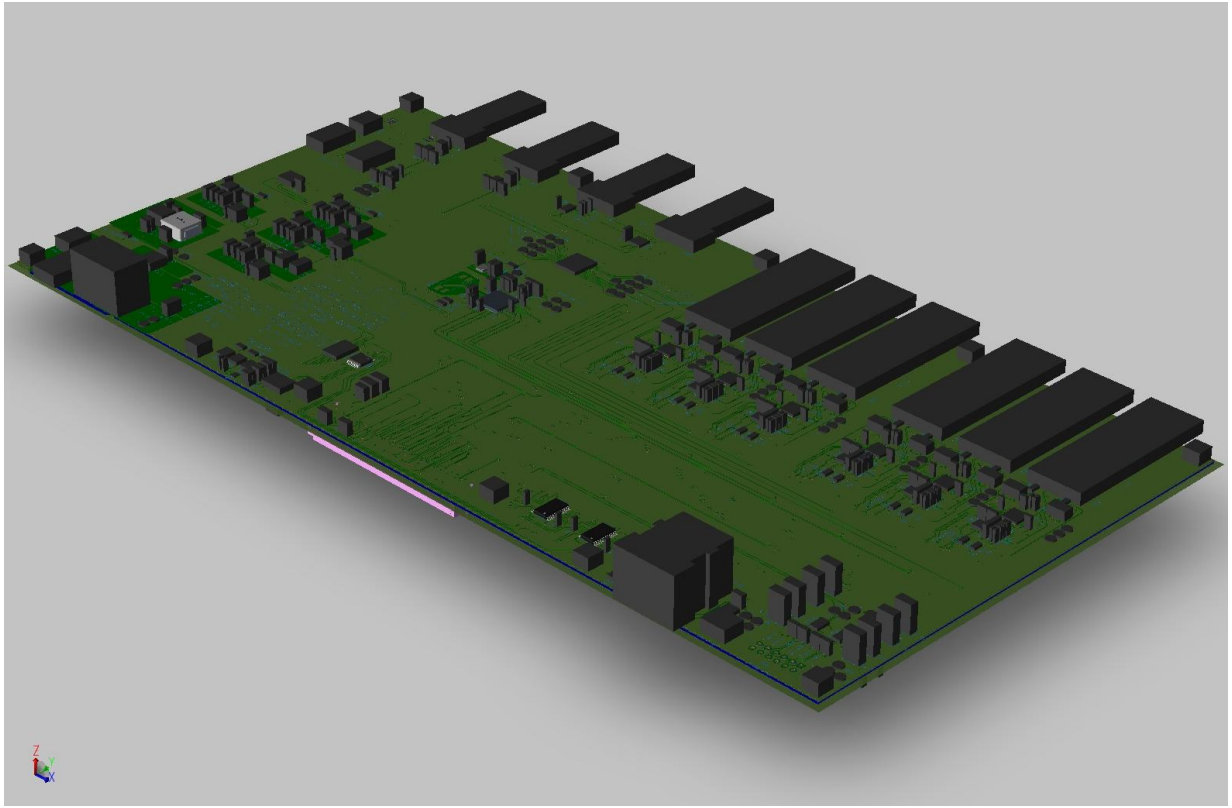
  - Fan out clock and data to FIBs (COTS AMC carrier)

- **Fiber Interface Board (FIB)**

  - FMC with 8 SFP modules, hosted by AMC carrier

  - Fans out timing data-stream to timing endpoints

GPS Interface Board

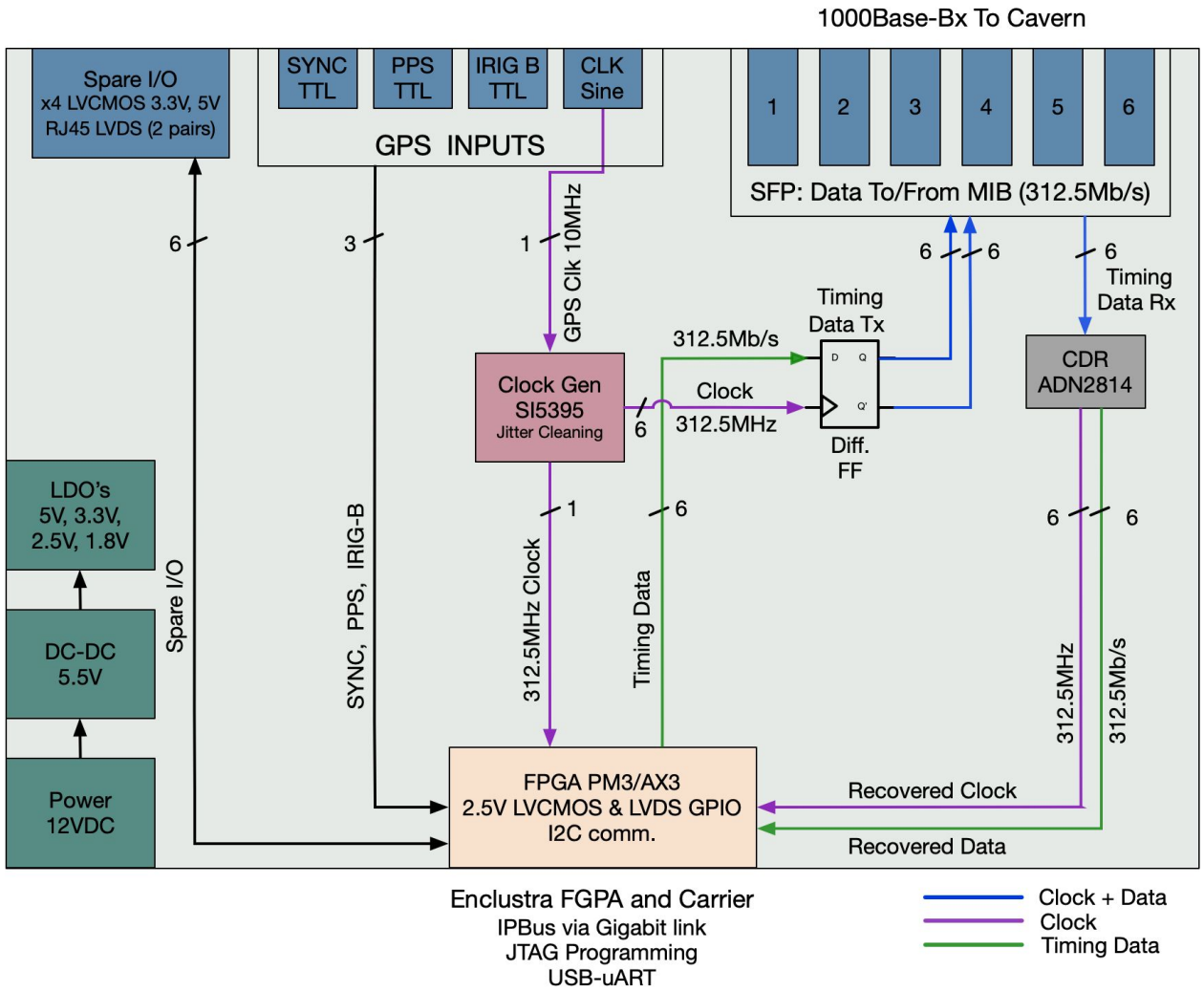


GIB: Functionality

- Derive experiment 62.5MHz clock from 10MHz GPS clock
- Transmit clock + data (312.5Mb/s) to cavern/MIB
- Receive and recover clock and data from cavern/MIB
- Generate DUNE SP 64b timestamp
- Receive GPS timecode in IRIG-B
    - Initialize DUNE SP timestamp ticks since epoch
- Note: Data format uses the timing system protocol.

GIB: Block Diagram

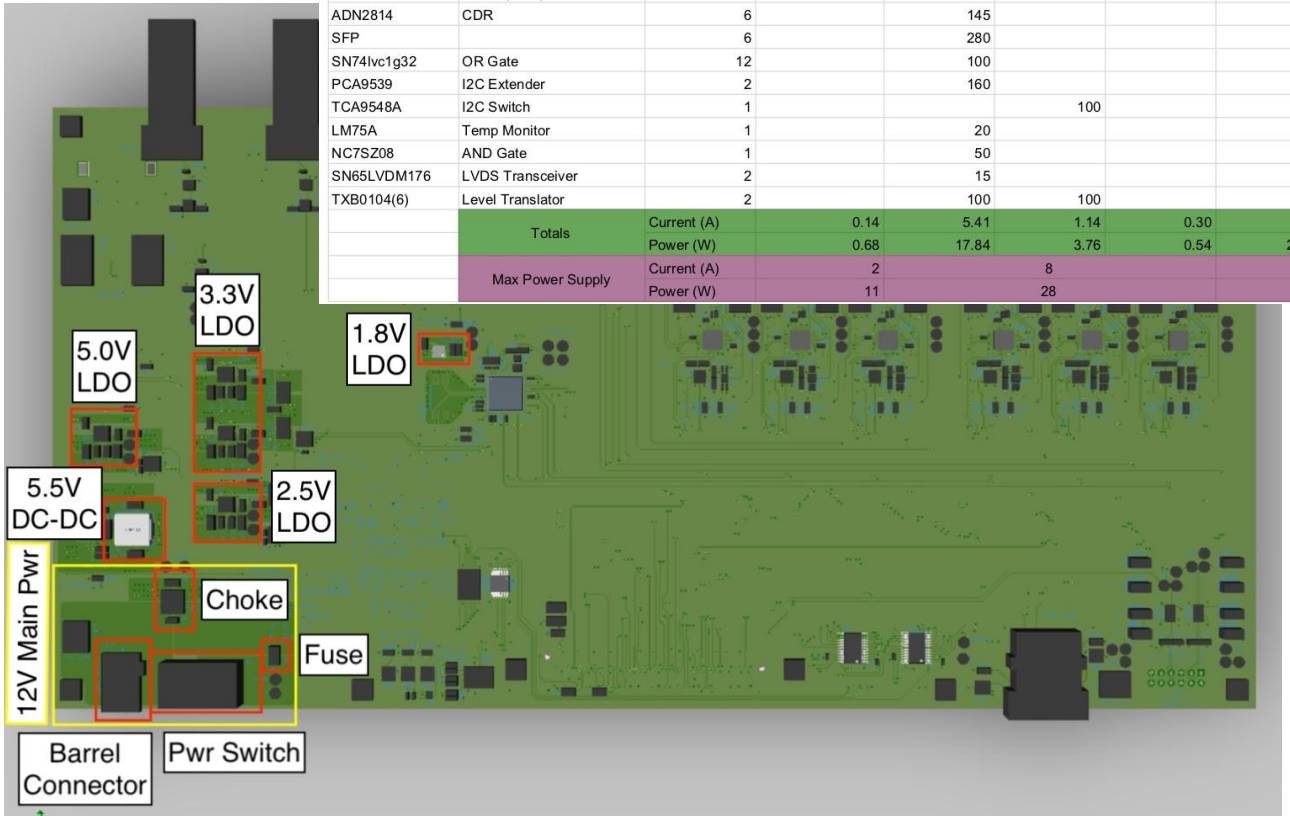
- Receive GPS Clock and Timecode
- Derive experiment clock from GPS clock
- Transmit clock + data *to* cavern/MIB
- Receive clock + data *from* cavern/MIB



GIB: Power

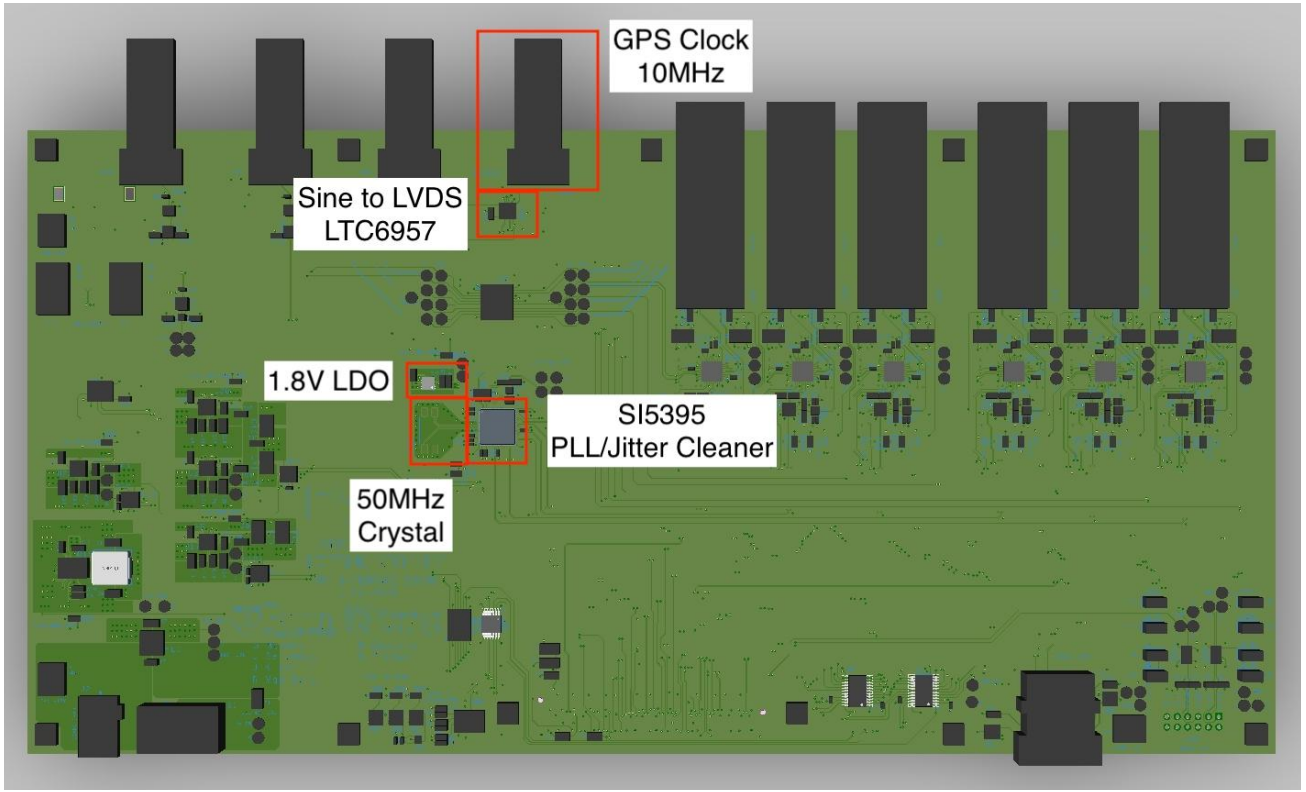
- Main power in: 12 VDC
- Main power fused and choked
- **12V → 5.5V** using DC-DC switching converter
- **5.5V → (5V, 3.3V, 2.5V)** using LDO's
- **3.3V → 1.8V** LDO clock generator (SI5395) only
- Est. Power usage 23W

Power Estimate			Max Current (mA)				
Part	Description	Occurence	VCC5V	VCC3V3	VCC2V5	VCC1V8	12V Main PWR
LTC6957-2	Sine Wave to LVDS	1		72			
MAX9371	Low Jitter 5V TTL to LVDS	2	16				
SN74avc2t45	5V <--> 3.3V	1	100	100			
SN74avc2t45	3.3V <--> 2.5V	5		100	100		
SI5395	Clock Generator	1		302		300	
LTC2945	Power Monitor	4	1.2				
24AA025E48T	Board ID EEPROM	1		3			
LEDs		13		20			
NB7V52M	Diff. Flip-Flop	6			90		
ADN2814	CDR	6		145			
SFP		6		280			
SN74lvc1g32	OR Gate	12		100			
PCA9539	I2C Extender	2		160			
TCA9548A	I2C Switch	1			100		
LM75A	Temp Monitor	1		20			
NC7SZ08	AND Gate	1		50			
SN65LVDM176	LVDS Transceiver	2		15			
TXB0104(6)	Level Translator	2		100	100		
	Totals	Current (A)	0.14	5.41	1.14	0.30	
		Power (W)	0.68	17.84	3.76	0.54	22.83
	Max Power Supply	Current (A)	2		8		4
		Power (W)	11		28		48



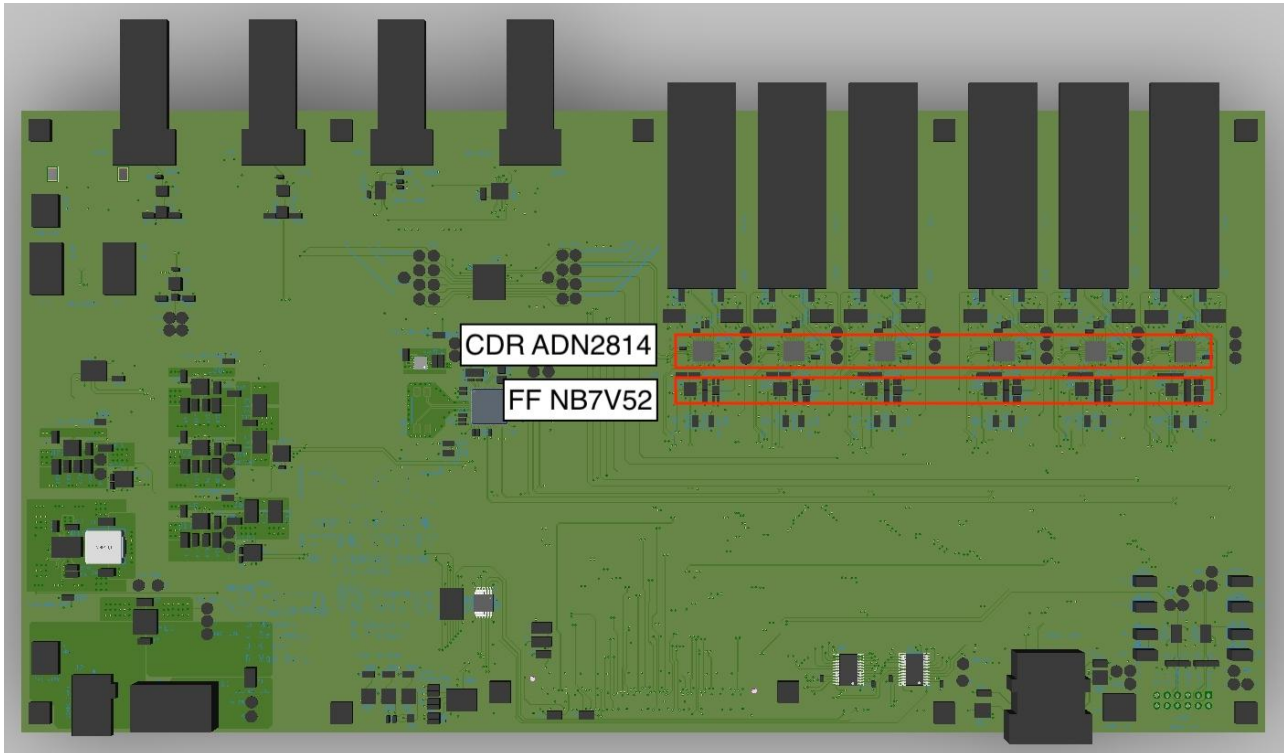
GIB: Clocks

- GPS reference clock 10MHz (sine wave)
- SI5395 low jitter clock generator: derives from reference clock, the 312.5MHz distributed clock



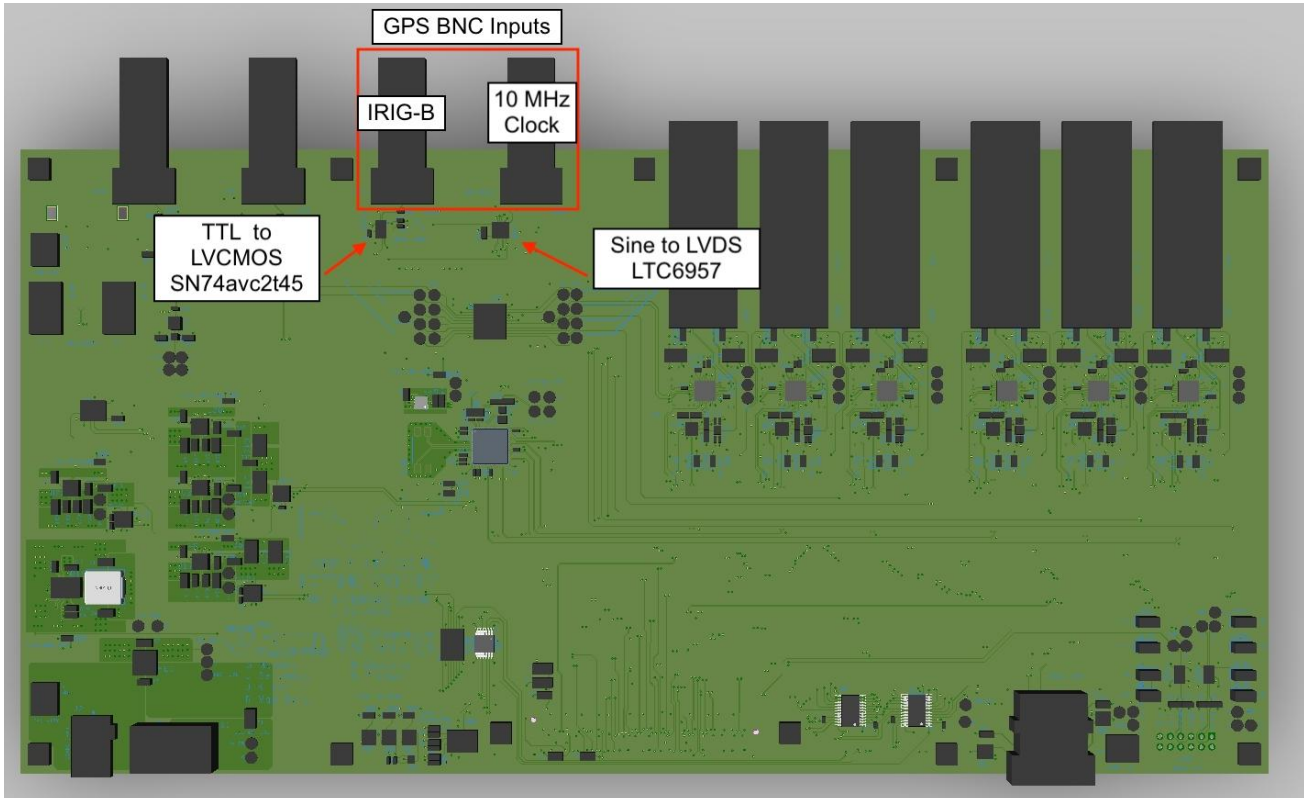
GIB: Data

- **Tx:** Data sent from FPGA, re-timed with D-type differential FF (NB7V52)
- **Rx:** Data received and clock recovered using CDR chip (ADN2814)



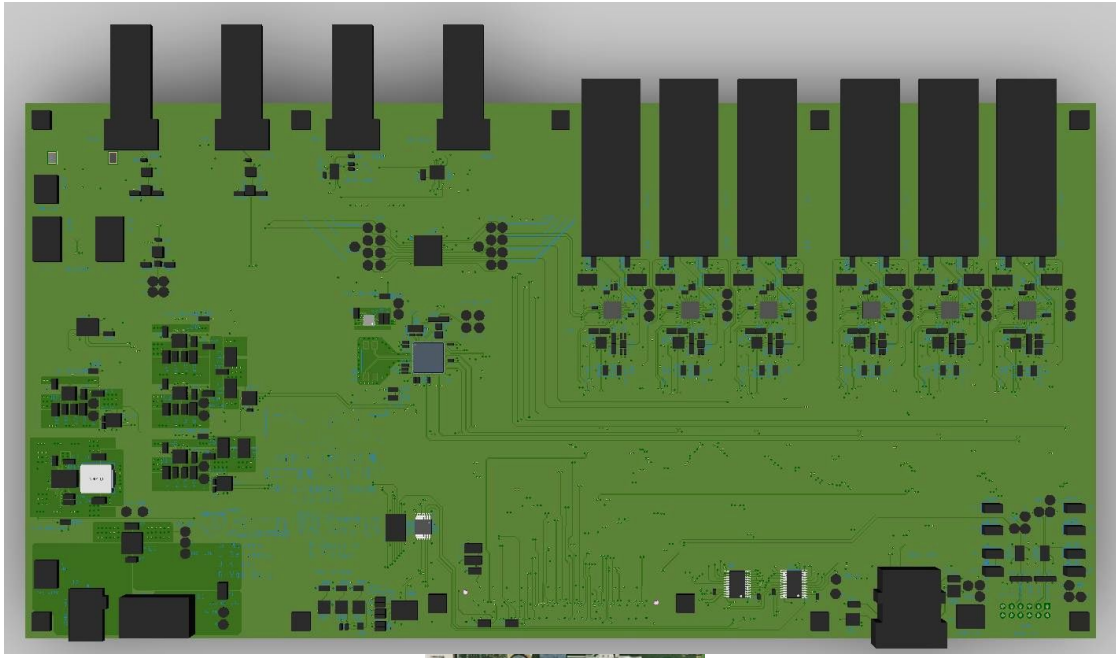
GIB: GPS Inputs

- **GPS Clock:** 10MHz Sine wave to LVDS
- **IRIG-B:** 5V TTL signal converted to 2.5V LVCMOS



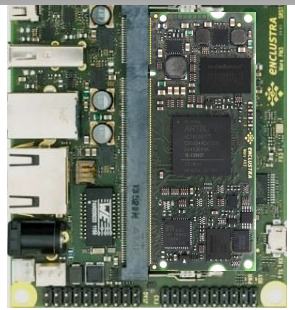
GIB: FPGA Board

- **Carrier & FPGA** are both COTS items
- **Carrier:** Enclustra PM3
- **FPGA:** Enclustra AX3 Artix-7 module
  - Flexible FPGA module choice
- Used in ProtoDUNE SP run 1 master timing unit (TLU)



PM3

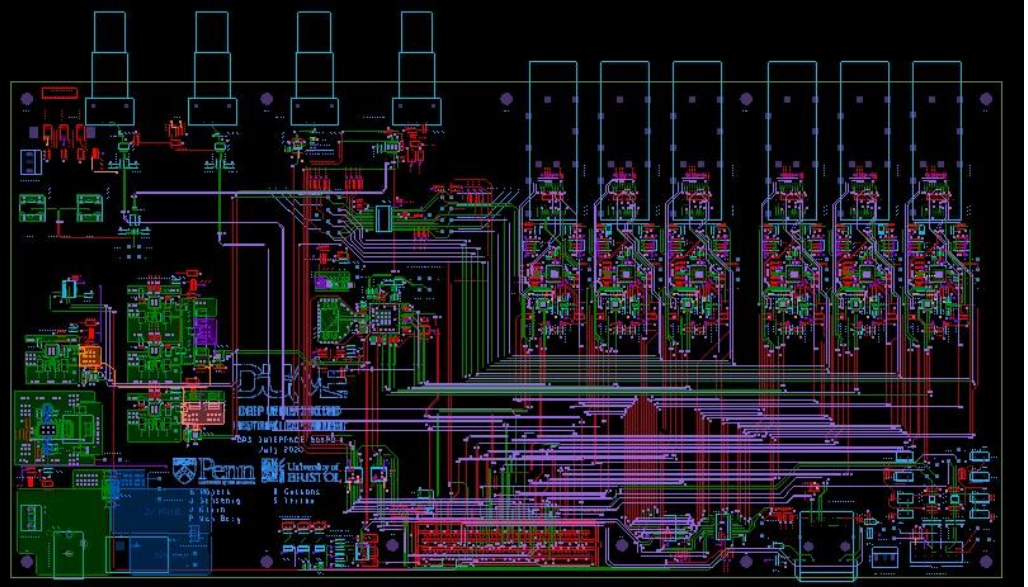
AX3

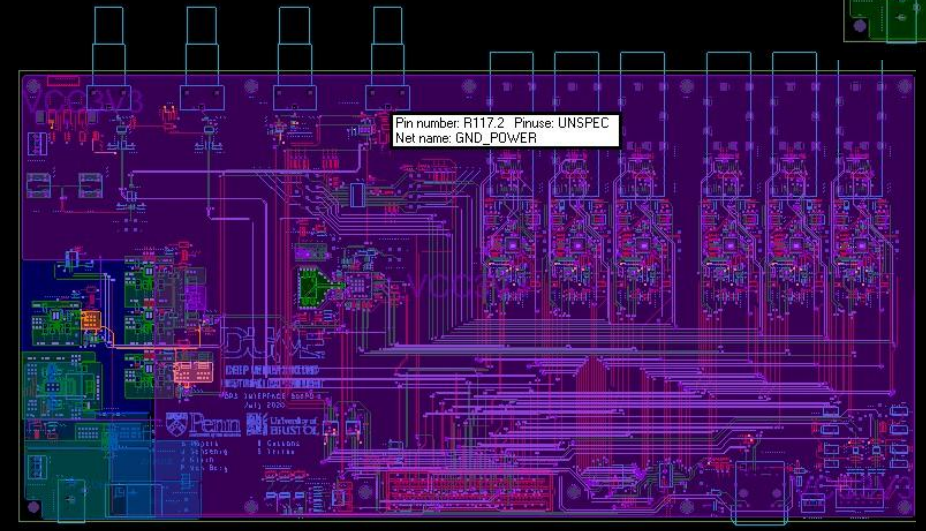


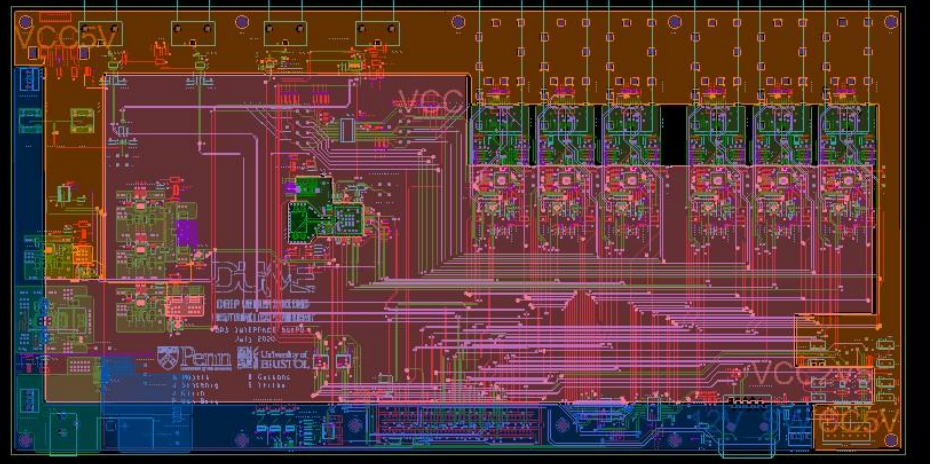
Example of how the GIB connects via FMC to Enclustra PM3 carrier board.

GIB: PCB

- 3 layer trace layout (right)
- 2 power planes layers (bottom)
- 8 layers: 3 signal, 2 Pwr, 3 GND
- 0.060in (1.524mm) thickness



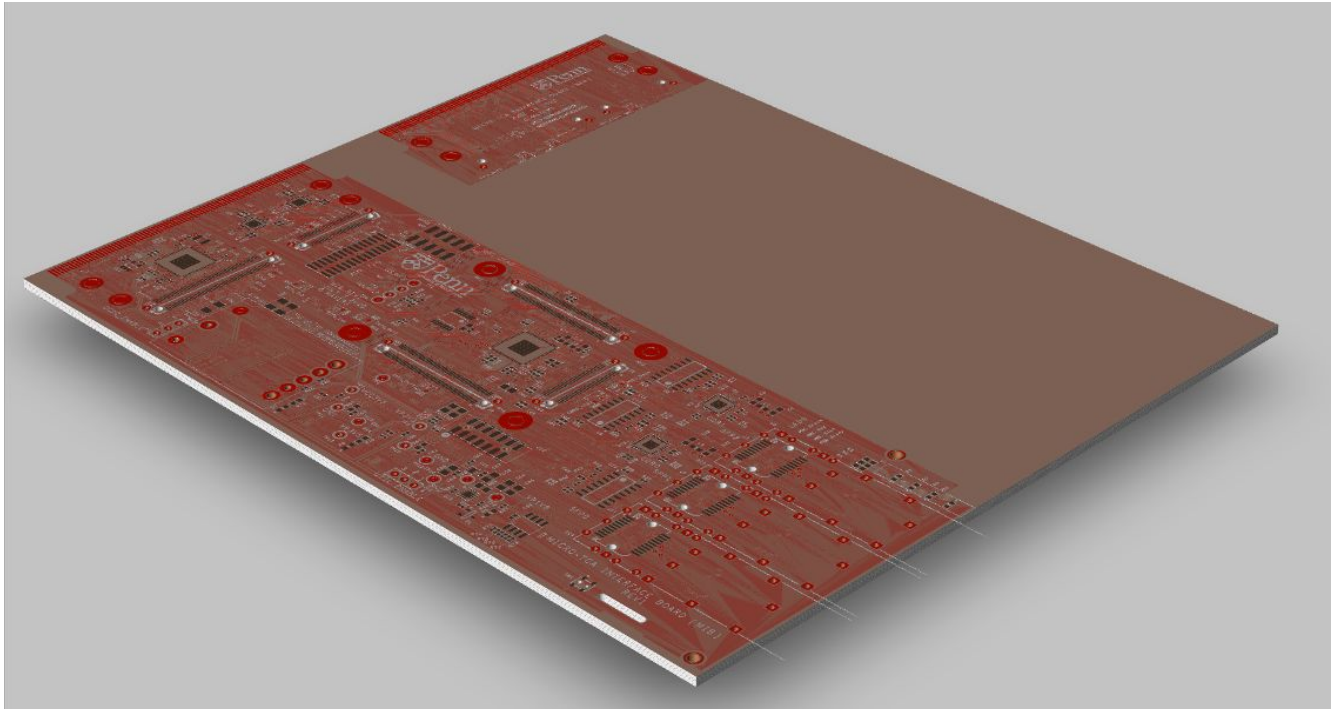




GIB: Status

- Submitted for fabrication (July 13) 10 day turn-around
- 10 boards being fabricated, planning to assemble 3.
- Boards will be assembled and tested at Penn

MicroTCA Interface Board

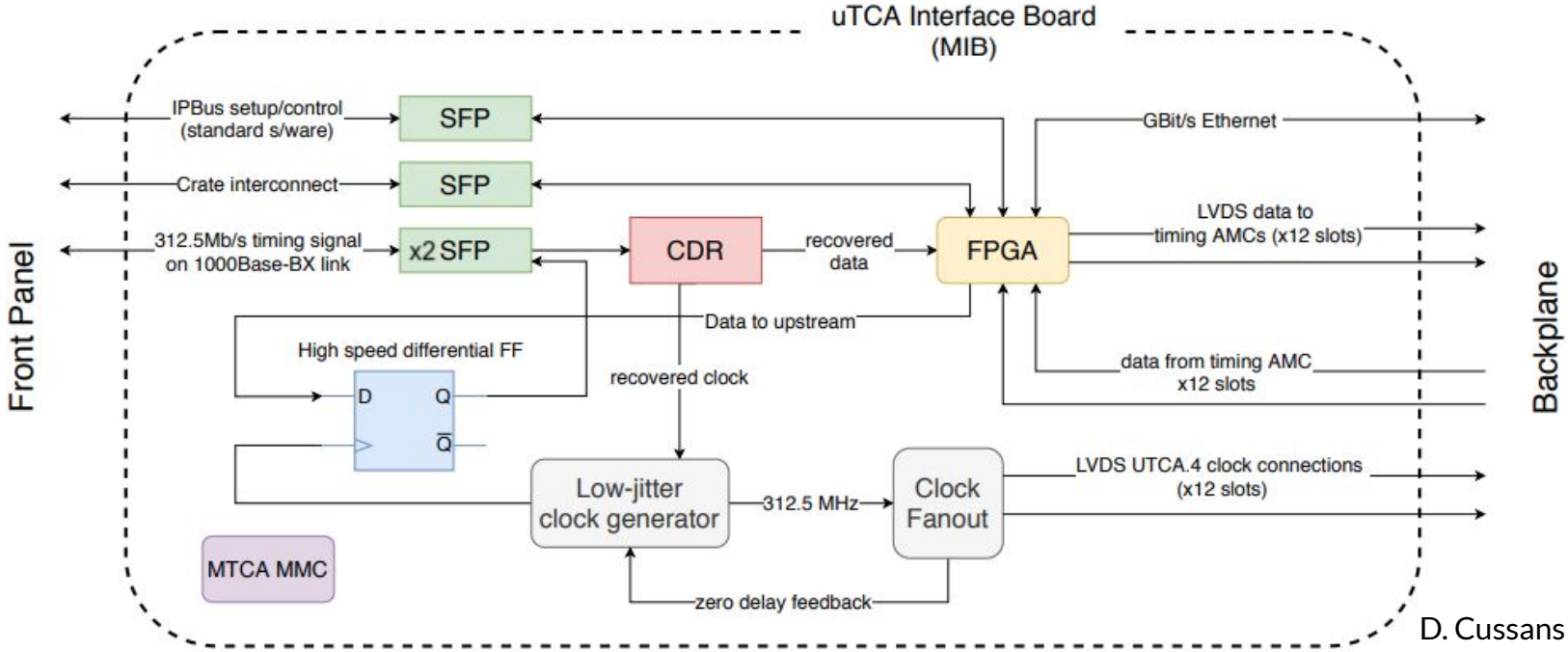


MIB: Functionality

- Receive timing data-stream from GIB
- Fan out clock and data to FIBs (COTS AMC carriers)
- Serialize timing commands and transmit to the timing network
- Phase measurement of incoming timing signals from slaves, i.e. FIBs and timing endpoints

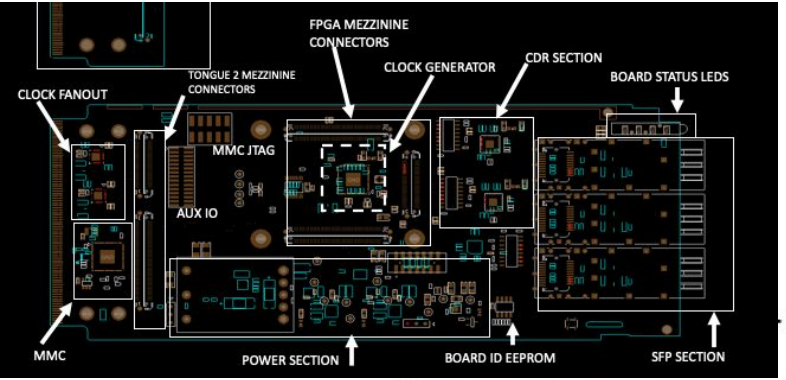
MIB: Block Diagram

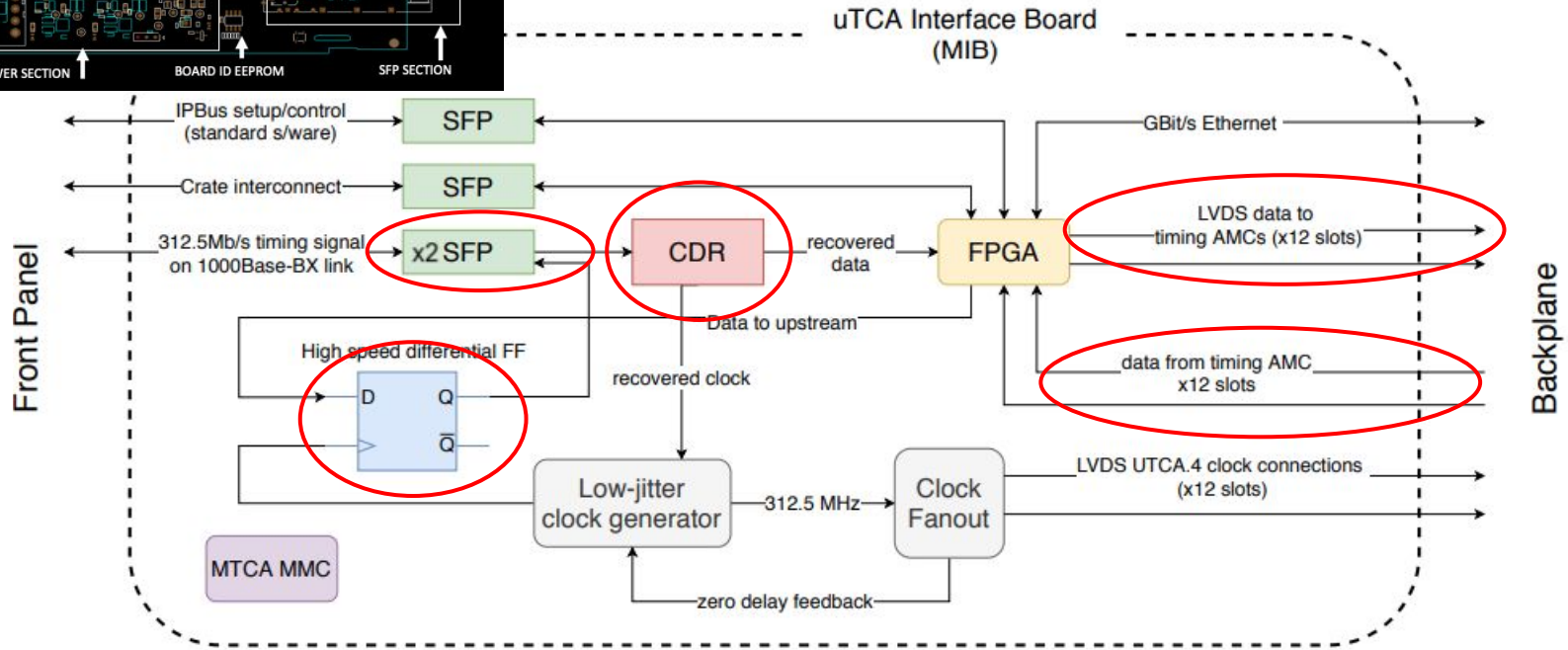
- Receive timing data from redundant GIBs
- Generate clock and data for all AMC/FIB slots
- IPBus setup/control via Gigabit link
- MMC controller



MIB: Data

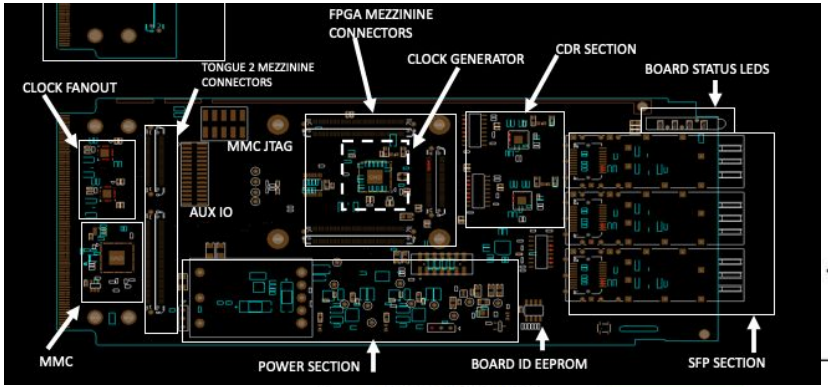
- **SFP Rx data from GIB's:** (SFP 1,2) recovered by CDR
- **SFP Tx data to GIB's:** from FPGA, either re-timed by FF or direct
  - LVDS data bus to/from all slots hosting AMC/FIB's

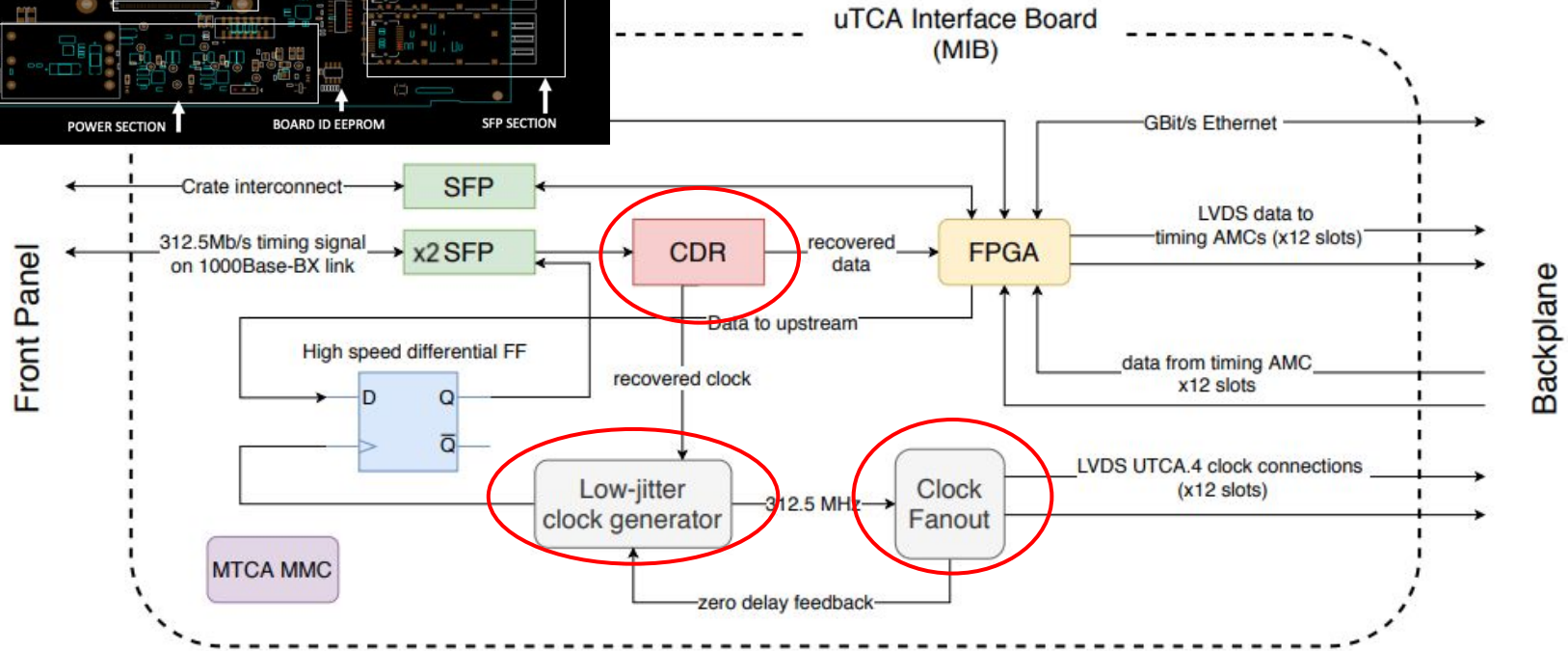




MIB: Clocks

- Recovered clock, select either SFP 1 or2 (redundant GIBs)
- Low jitter clock generator (SI5395)
- Clock fan-out (SI53342) to all AMC/FIB slots





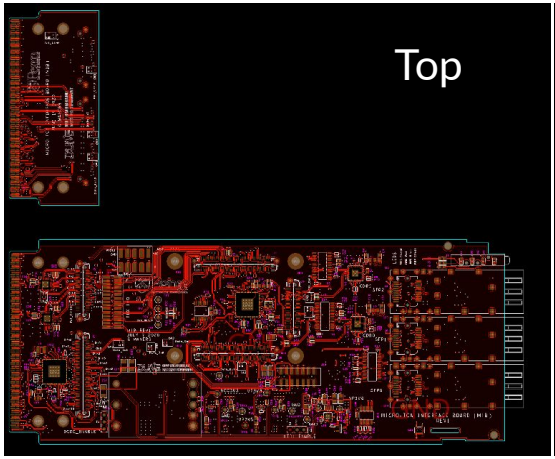
MIB: Power

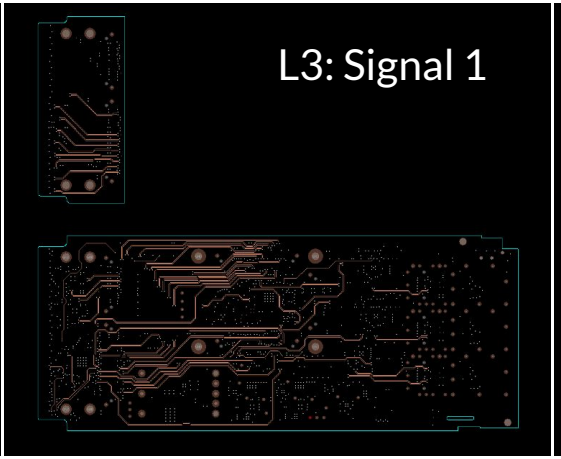
- Main power 12V @ 6.6A from MicroTCA crate
- DC-DC 12V → 3.5V
- LDO for VCC, VP 3.3V and 1.8V
- Estimated power usage 22W

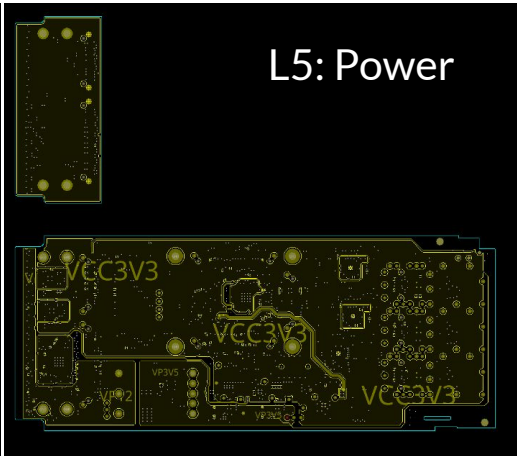
Power Requirements

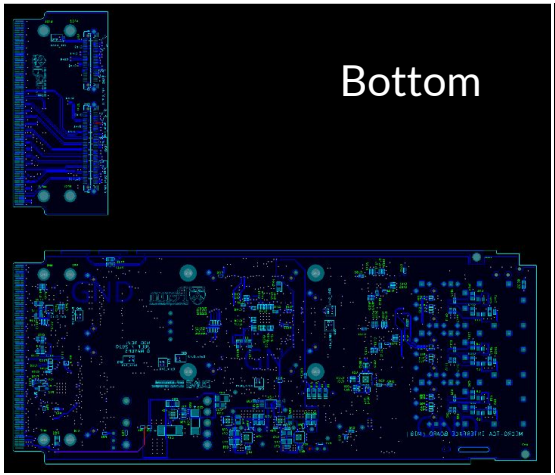
Part#	Disvription	IDD core (mA)	IDD_out/clk (mA)	No 0f Circuits	QTY	VCC3V3 IT(mA)	VP3V3 IT(mA)	VP1V8 IT(mA)
Si53344	10x clocks	280	21	10	5	2450		
Si53342	6x clocks	80	21	6	2	412		
SI5394P	4x clocks	250	30	2	1	60		250
NBSG53A	D-FF		50	1	1	50		
AND2814	CDR	145	-	-	1	145		
TE0712_MODULE	FPGA MODULE	3000	-	1	1	-	3000	
SPF_MODULES	SFP	220	-		2	440		
GREEN_LED	GREEN_LED	20	-	1	1	20		
RED_LED	RED_LED	20	-	1	1	20		
BLUE_LED	BLUE_LED	20	-	1	1	20		
					I (A)	3.617	3	0.25
					Power (W)	11.9361	9.9	0.45

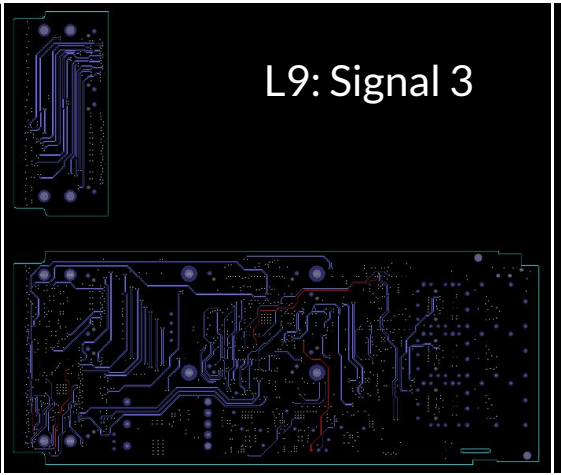
MIB PCB

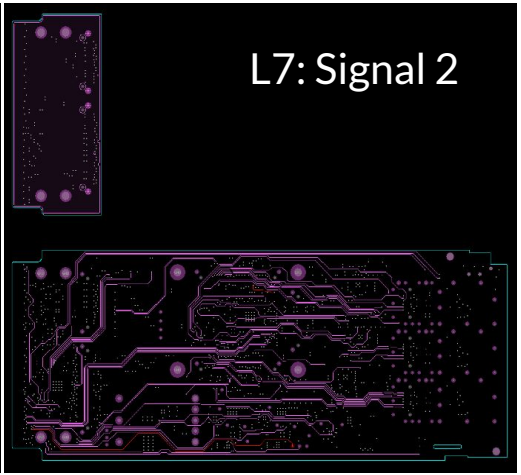










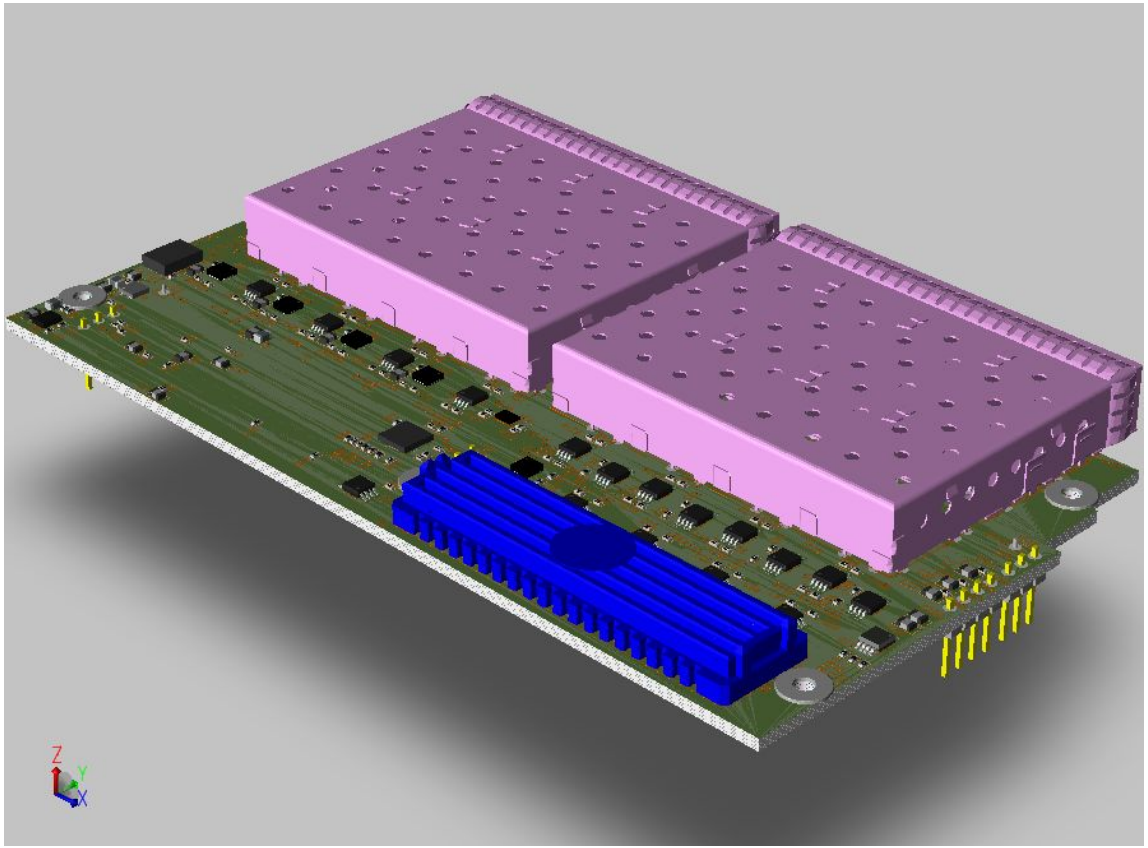


- 10 layer (5 signal, 1 pwr, 4 GND)

MIB: Status

- Schematic design and PCB layout finished, ready for fabrication.
- Bristol leading the fabrication and testing effort of MIB
- Quotes obtained, submitting PCB for fabrication soon

Fiber Interface Board

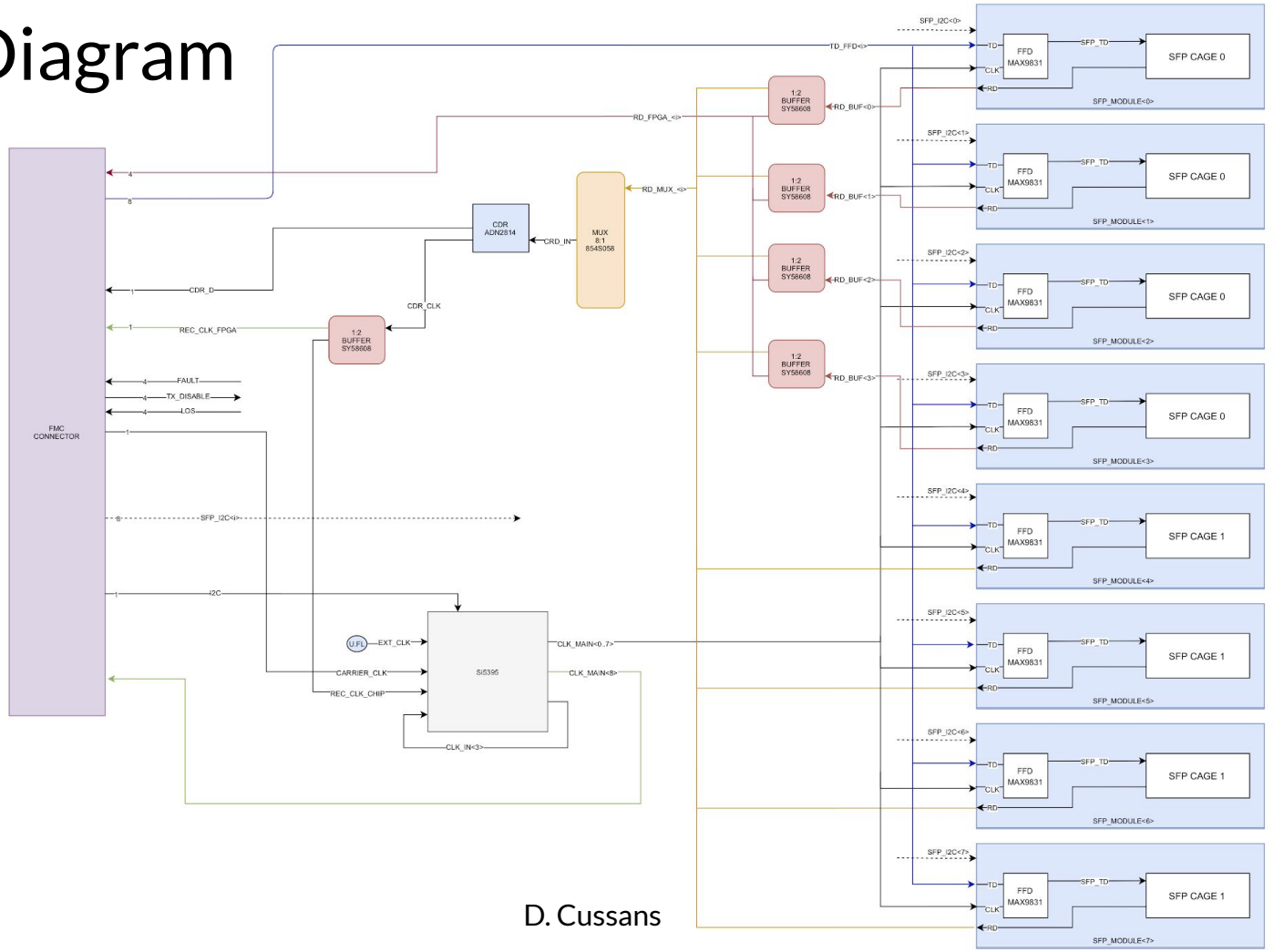


FIB: Functionality

- Receives clock and data from MIB
  - Low jitter clock generator (SI5395)
- Tx data to subsystem timing endpoints
  - Retimed onto low jitter clock with D-type FF
- All eight SFP multiplexed onto a single CDR chip
  - Used to recover clock

FIB: Block Diagram

- 8 SFP I/O
- Clock generator, reference clock received from MIB
- Tx data re-timed with D-type FF
- Rx data multiplexed to CDR (and FPGA)



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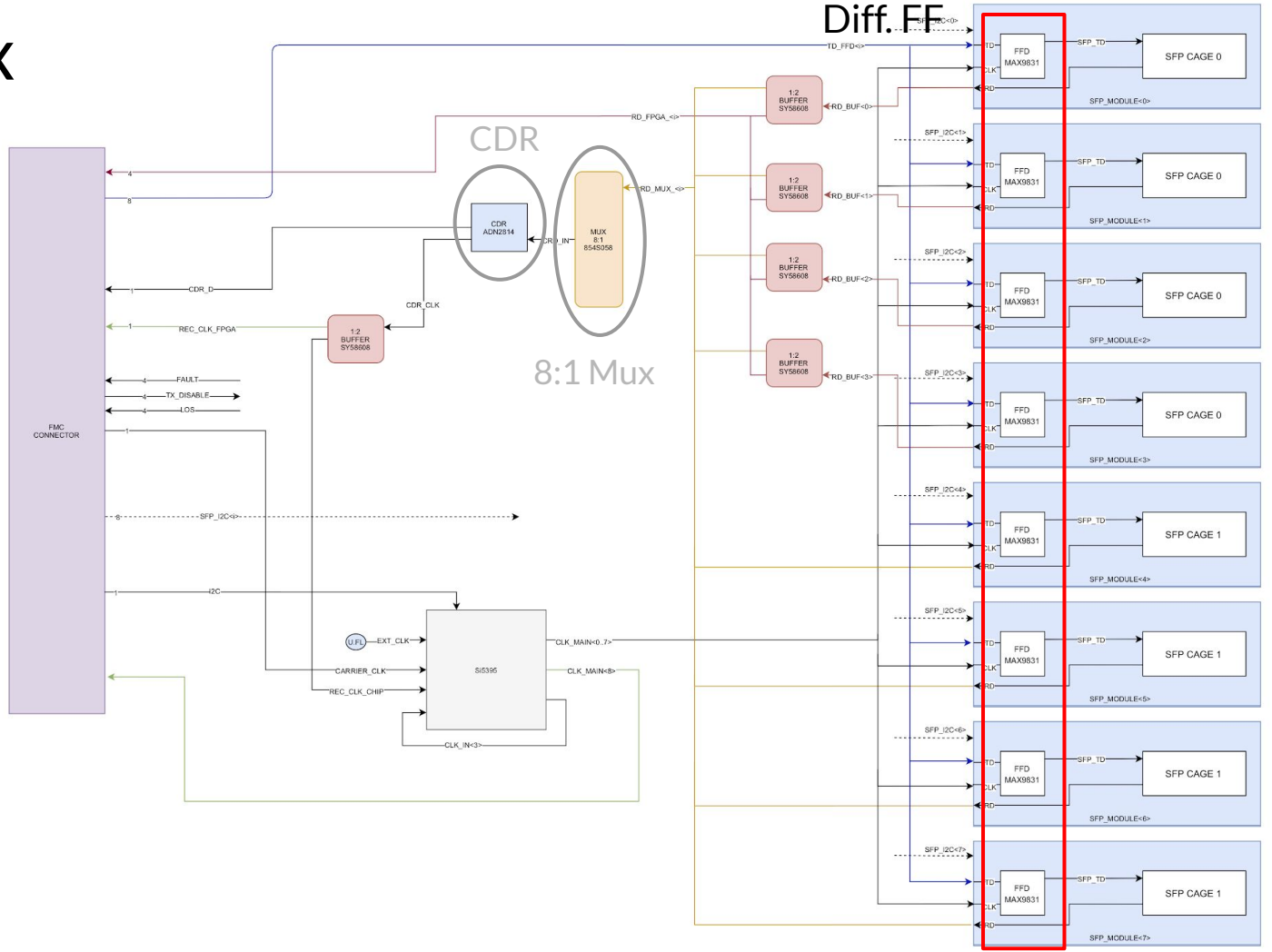
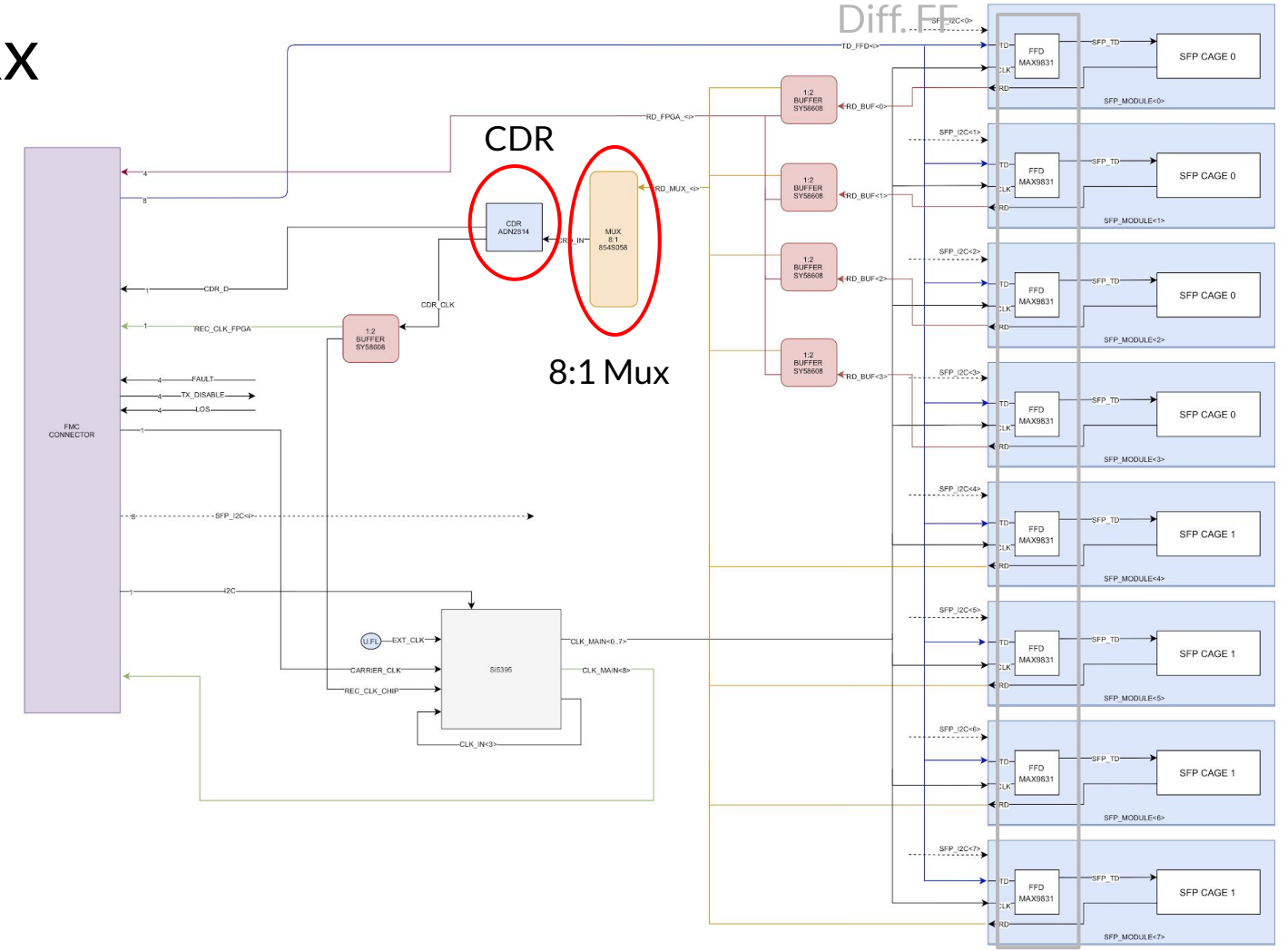
FIB: Data Tx

- 8 SFPs
- Tx data stream direct from FPGA
- Re-timed by high-speed differential D-type FF with 312.5MHz clock recovered from MIB



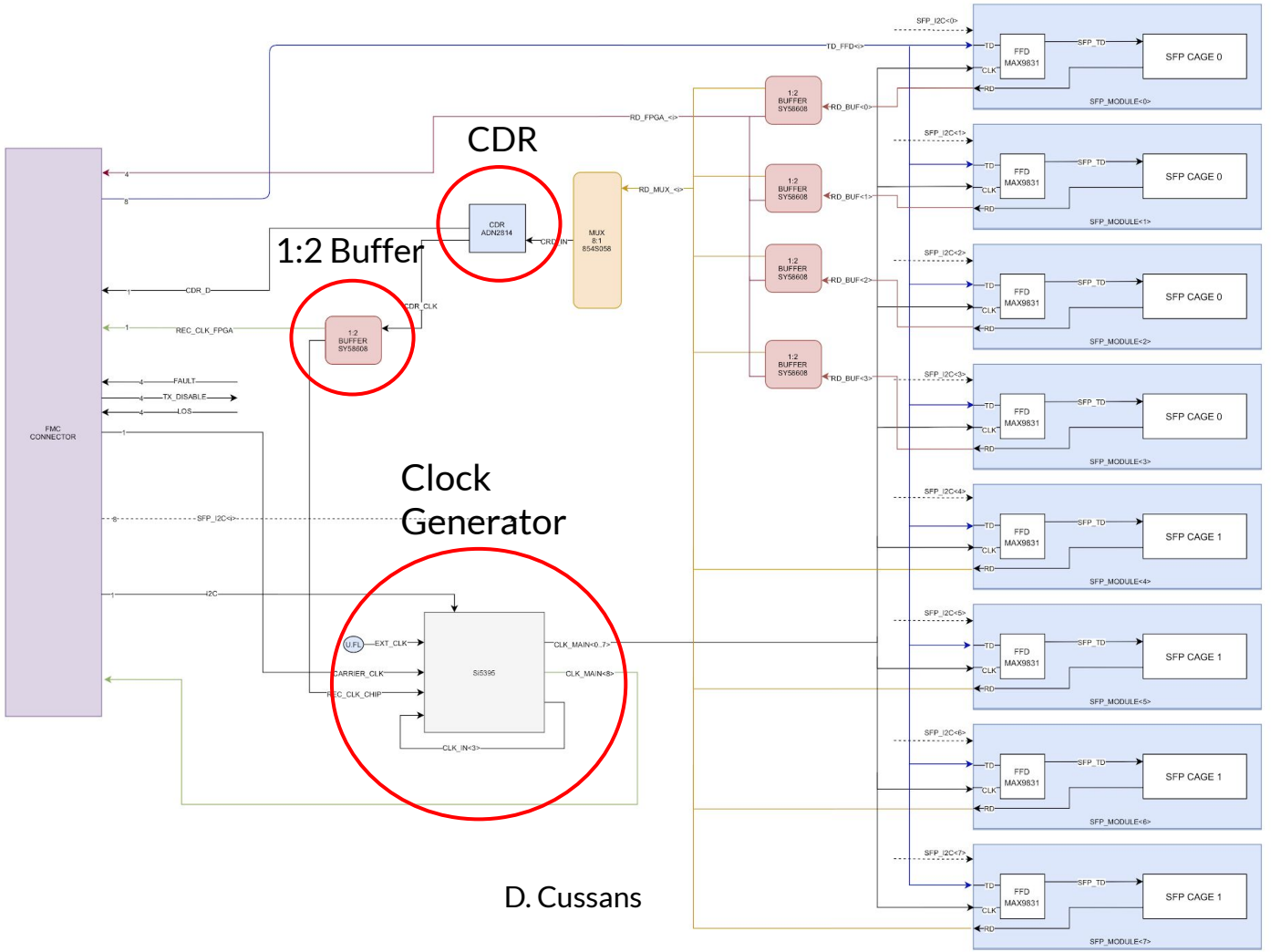
FIB: Data Rx

- (x8 ch) Rx data to 8:1 mux to CDR.
- Recovered clock: to clock generator and FPGA
- Recovered data: to FPGA



FIB: Clocks

- Clock recovered from MIB data using CDR (ADN2814)
- 1:2 buffer: clock for FPGA and clock generator
- Clock generator reference clock received from MIB (SI5395)



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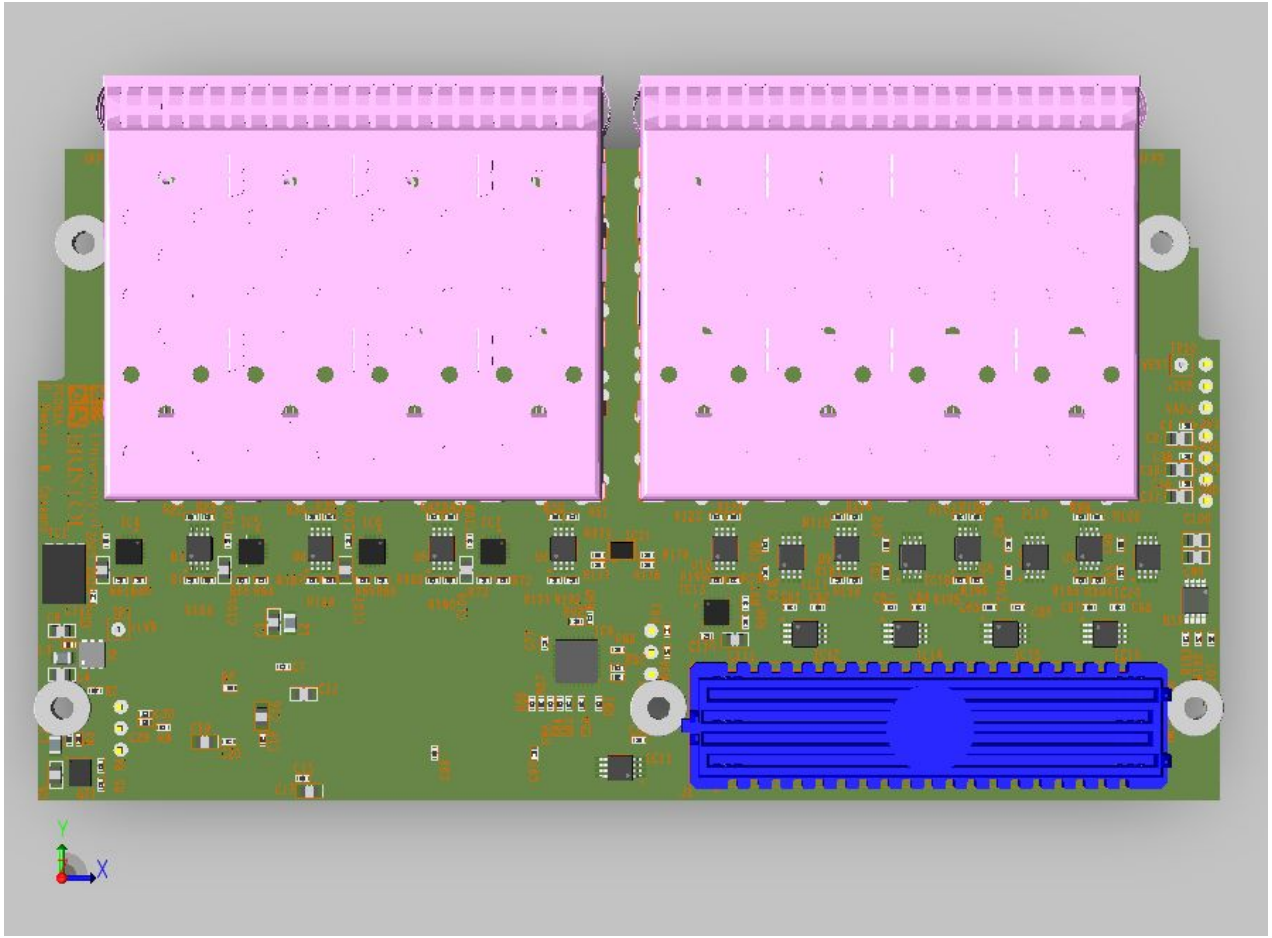
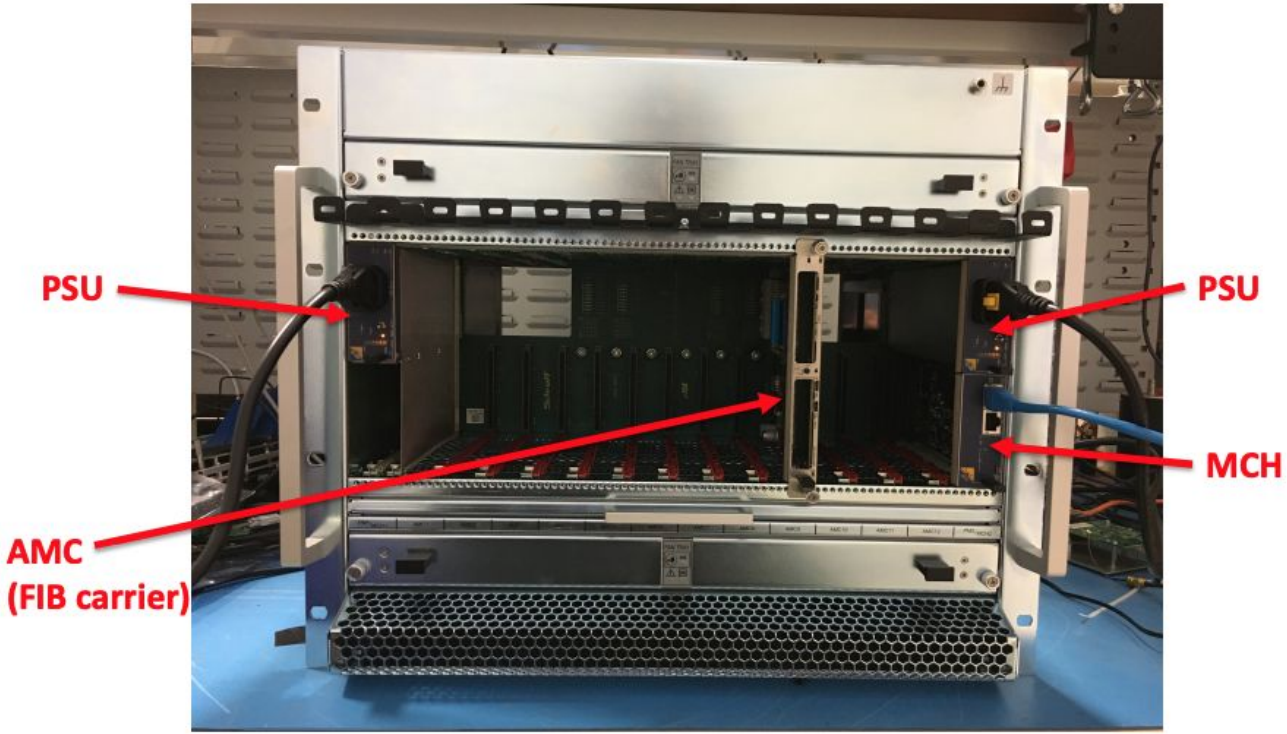
FIB: PCB

- FIB is a double width FPGA Mezzanine Card (VITA 57 FMC)
- Has 8 SFP cages
- Carrier board is AMC
- MicroTCA crate, up to 12 AMC/FIBs
    - 10 needed



FIB: Crate

- MicroTCA crate
- 12 slots for FIB/AMCs
- Contains one MIB per crate.



FIB: Status

- Four boards fabricated
- Assembled FIBs expected this week
- FIB tests will be done by Bristol
- Firmware for initial tests ready

Summary

- GIB submitted for fabrication.
  - Next steps are assembling and testing
- MIB will be submitted for fabrication and assembly soon.
  - Technical discussion underway with fabrication house
- Assembled FIBs expected this week.
  - Initial FIB testing firmware ready

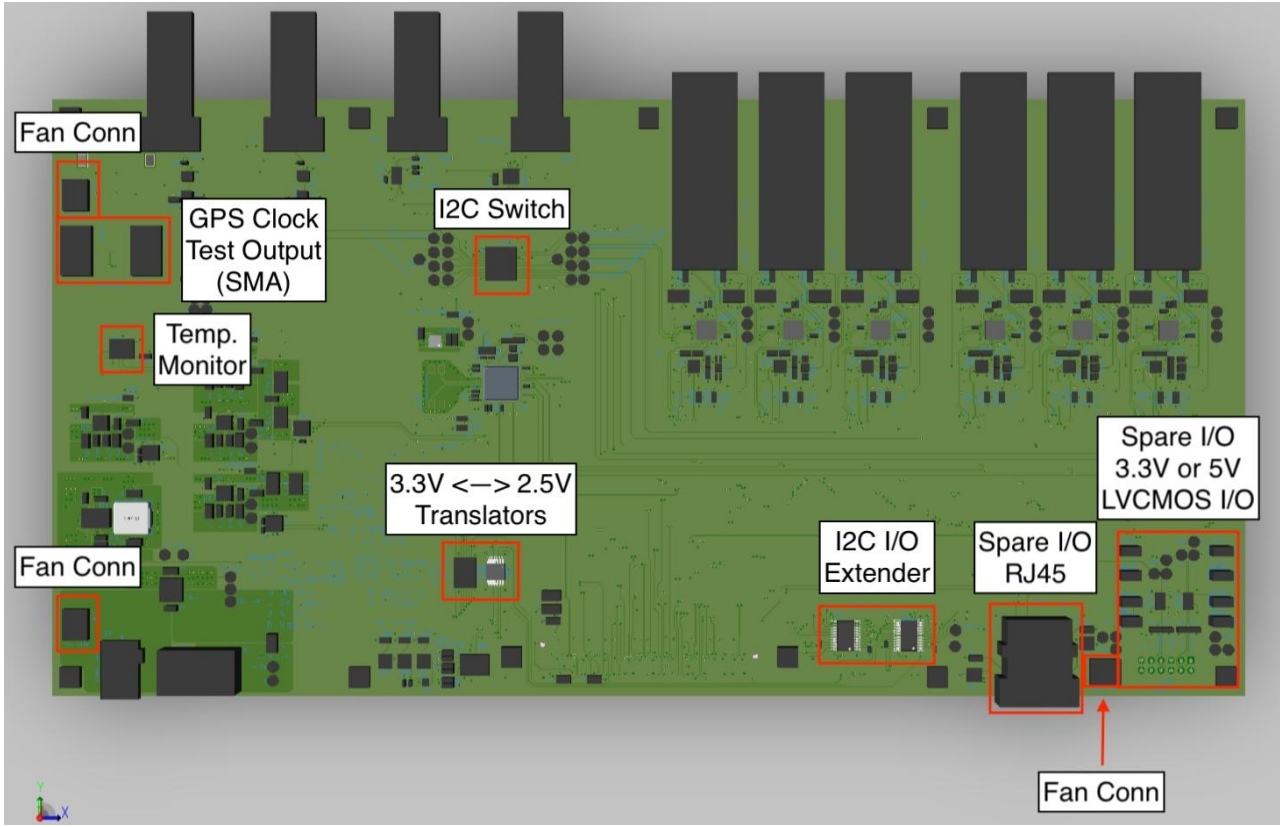
Thank You

Questions?

Backup Slides

GIB: Misc

- **I2C Switch:** Provide unique addr. for SFP, CDR
- **I2C I/O Ext.:** Handles the LOS, LOL, Fault, SFP Disable
- Spare I/O
  - (2) LVDS pairs
  - (4) 5V or 3.3V LVCMOS
- Fan connectors are 12V



MIB Dimensions