ECal with Integrated Electronics

Ray Frey, U of Oregon

Ongoing R&D Efforts:

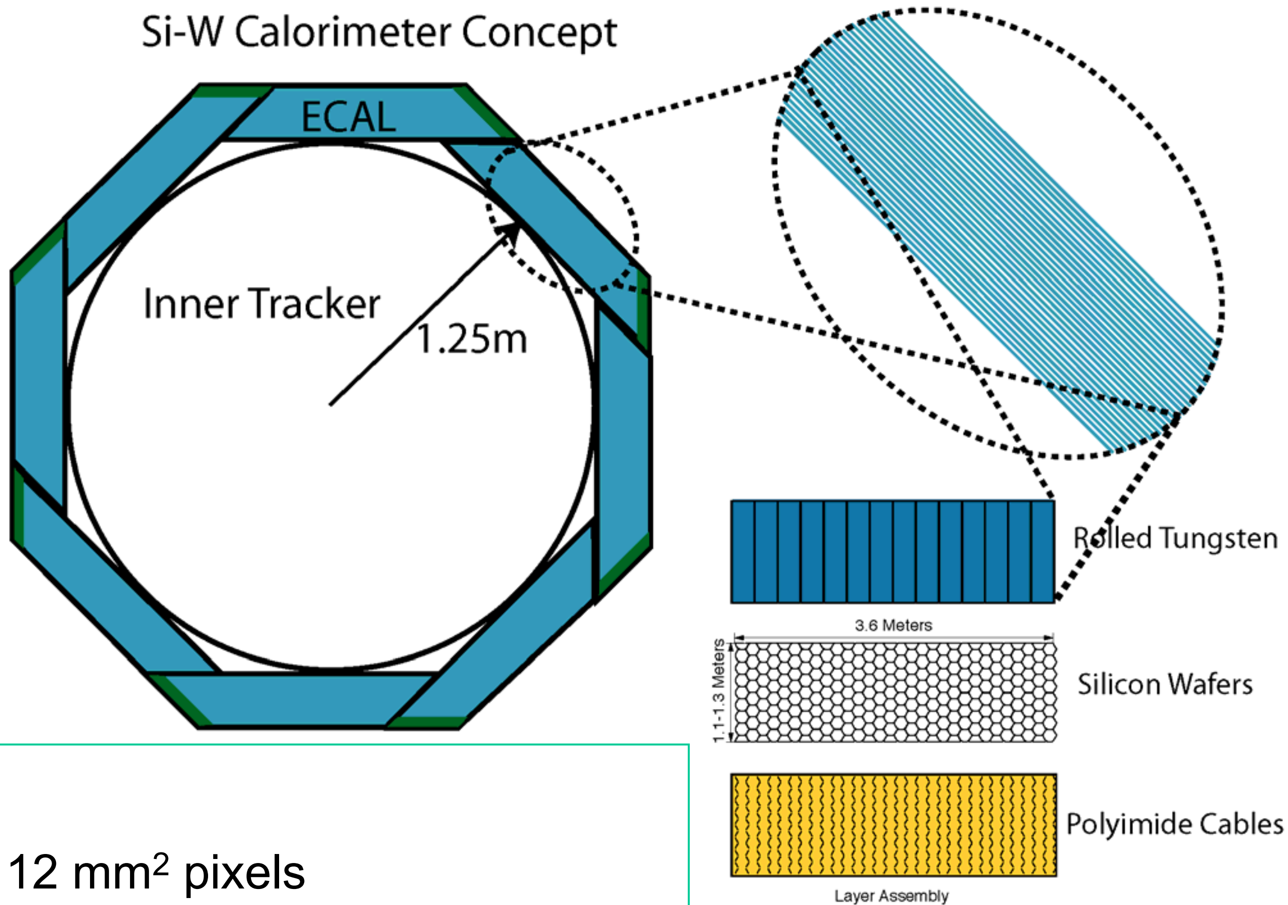
- CALICE silicon-tungsten ECal – 2 parallel efforts:
  - Technology Prototype → "Eudet Module" (integrated electronics)
  - Physics Prototype → currently in test beam (electronics external)
- MAPs ECal
  - Led by a sub-group of CALICE
  - More recent – needs some proof of principle work before test beams
- "U.S." silicon-tungsten ECal
  - Has developed only an integrated approach from the start

Goal of this R&D

Design a <u>practical</u> ECal which (1) meets (or exceeds) the physics requirements (2) with a technology that would actually work at the ILC.

- The physics case implies a highly segmented “imaging calorimeter” with modest EM energy resolution $\Rightarrow$ Si-W
- The key to making this practical is a highly <u>integrated electronic readout:</u>
  - readout channel count = pixel count / ~1000
  - requires low power budget (passive cooling)
  - must handle the large dynamic range of energy depositions (few thousand) with excellent S/N
- This takes some time to develop (getting close).
- Testing in beams will be crucial.

The "U.S." Silicon-Tungsten ECal R&D



Currently optimized for the SiD concept

Baseline configuration:

- transverse segmentation: 12 mm^2 pixels
- longitudinal: $(20 \times 5/7\ X_0) + (10 \times 10/7\ X_0) \Rightarrow$ 17%/sqrt(E)
- 1 mm readout gaps $\Rightarrow$ 13 mm effective Moliere radius

US Si-W ECal R&D Collaboration

M. Breidenbach, D. Freytag, N. Graf, R. Herbst, G. Haller, J. Jaros
Stanford Linear Accelerator Center

- KPiX readout chip
- downstream readout
- detector, cable development
- mechanical design and integration

J. Brau, R. Frey, D. Strom, M. Robinson, A.Tubman
U. Oregon

- detector development
- readout electronics

V. Radeka
Brookhaven National Lab

- readout electronics

B. Holbrook, R. Lander, M. Tripathi
UC Davis

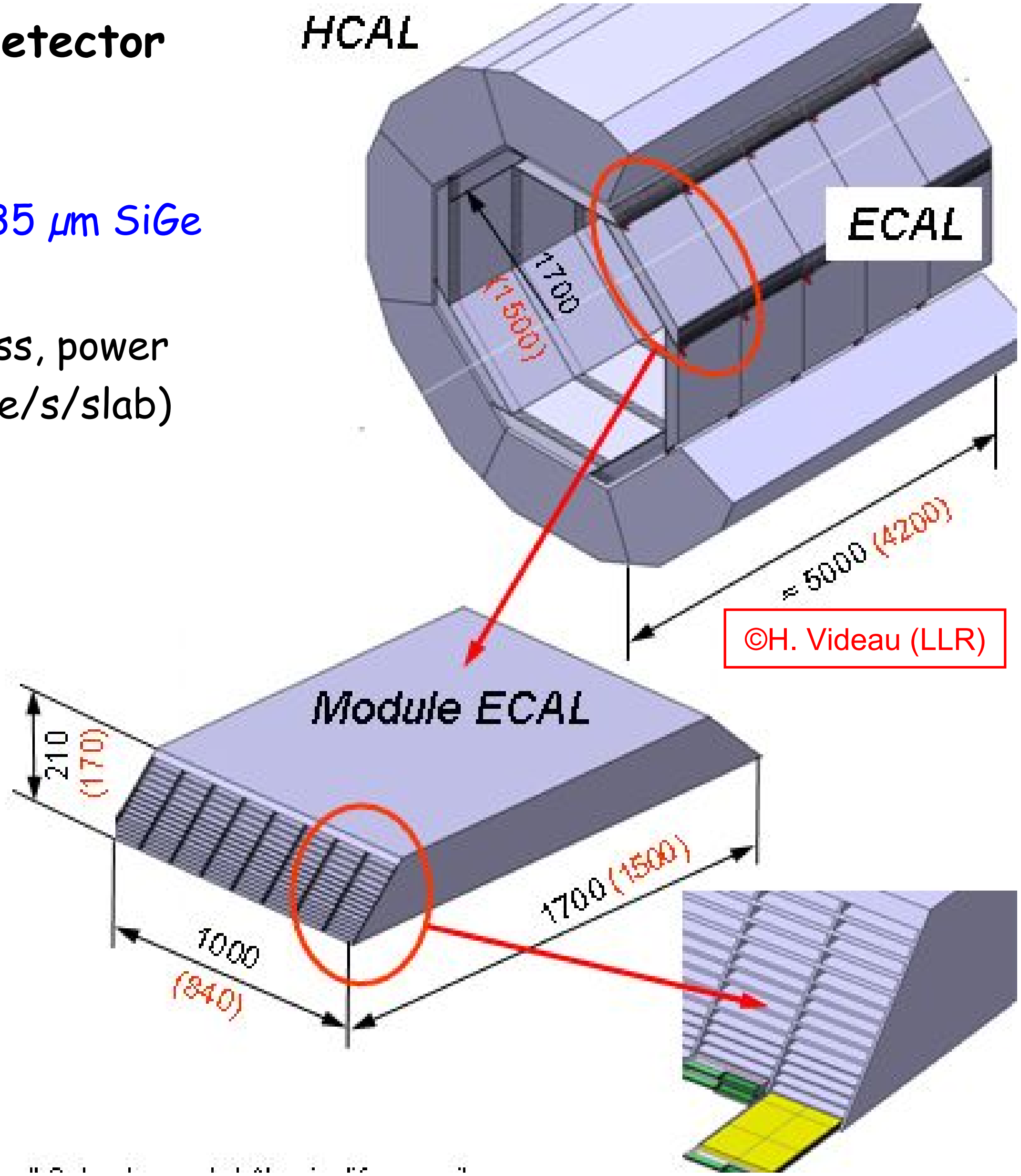
- cable development
- bump bonding

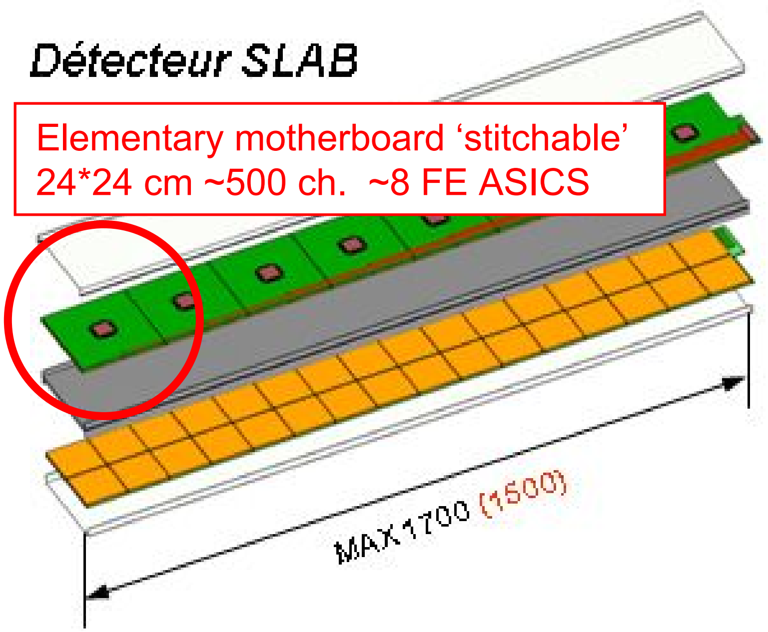
S. Adloff, F. Cadoux, J. Jacquemier, Y. Karyotakis
LAPP Annecy

- mechanical design and integration

Technological prototype : "EUDET module"

- **Front-end ASICs embedded in detector**
  - Very high level of integration
  - Ultra-low power with pulsed mode
  - FLC_TECH1 ASIC prototype in 0.35 μm SiGe
- **All communications via edge**
  - 4,000 ch/slab, minimal room, access, power
  - small data volume (~ few 100 kbyte/s/slab)
- **« Stitchable motherboards »**





Laboratoire d'Annecy de Physique des Particules – Annecy le vieux

Argonne National Laboratory

Department of Physics - University of Texas at Arlington

Northern Illinois Center for Accelerator and Detector Development – North Illinois University - Batavia

School of Physics and Astronomy, University of Birmingham

Cavendish Laboratory, Cambridge University

Laboratoire de Physique Corpusculaire - Clermont

Joint Institute for Nuclear Research - Dubna

DESY - Hamburg

Laboratoire de Physique Subatomique et Corpusculaire – Grenoble

Hamburg University

University of Iowa – Iowa

Kangnung National University - Kangnung

Kobe university – Kobe

Department of Physics,Imperial College London

Department of Physics and Astronomy, University College London

Physics Department, Royal Holloway University of London

Institut de Physique Nucléaire – Lyon

Department of Physics and Astronomy, University of Manchester
Shinshu University - Matsumoto

University of Minsk

Department of Physics, McGill University, Montréal

Institute of Theoretical and Experimental Physics - Moscow

Lebedev Physics Institute - Moscow

Moscow Engineering and Physics Institute- Moscow

Institute of Nuclear Physics - Moscow State University Moscow

Bhabha Atomic Research Center - Mumbai

Laboratoire de l'Accélérateur Linéaire - Orsay

Laboratoire Leprince-Ringuet - Ecole Polytechnique - Palaiseau

Physique des Interfaces et Couches Minces - Ecole Polytechnique - Palaiseau

Charles University - Prague

Institute of Physics, Academy of Sciences of the Czech Republic - Prague

Institute of High Energy Physics - Protvino

Department of Physics, University of Regina, Regina

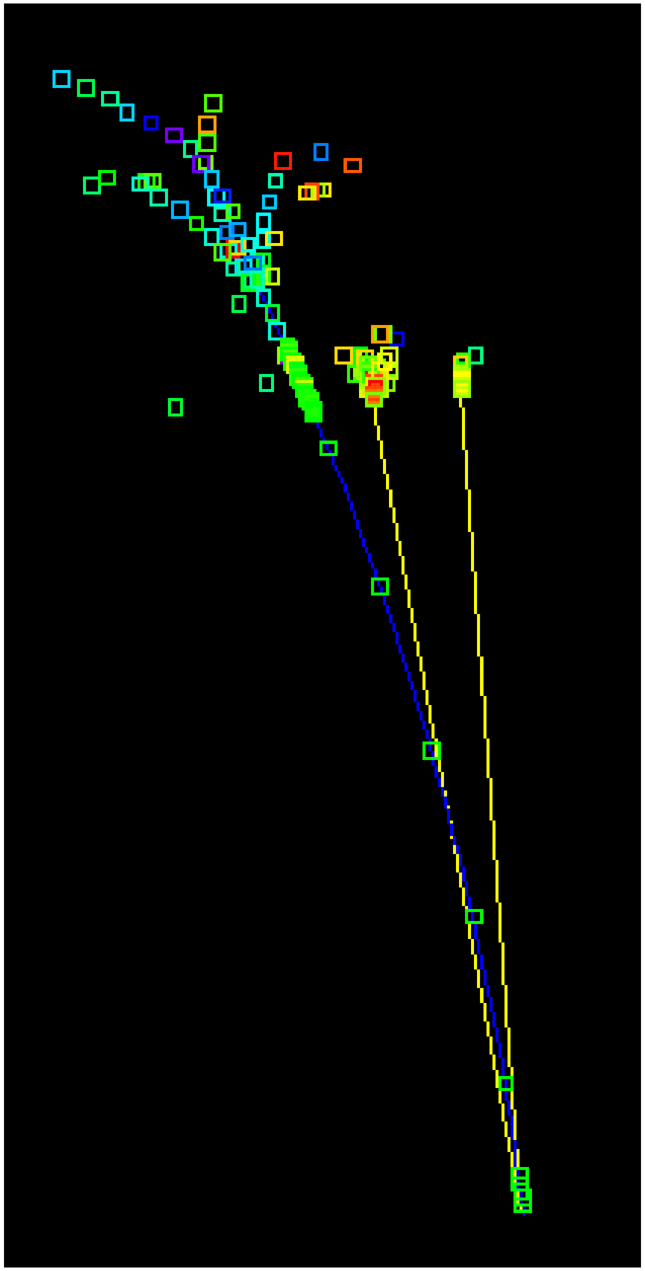
EWHA Womans University - Seoul

Yonsei University - Seoul

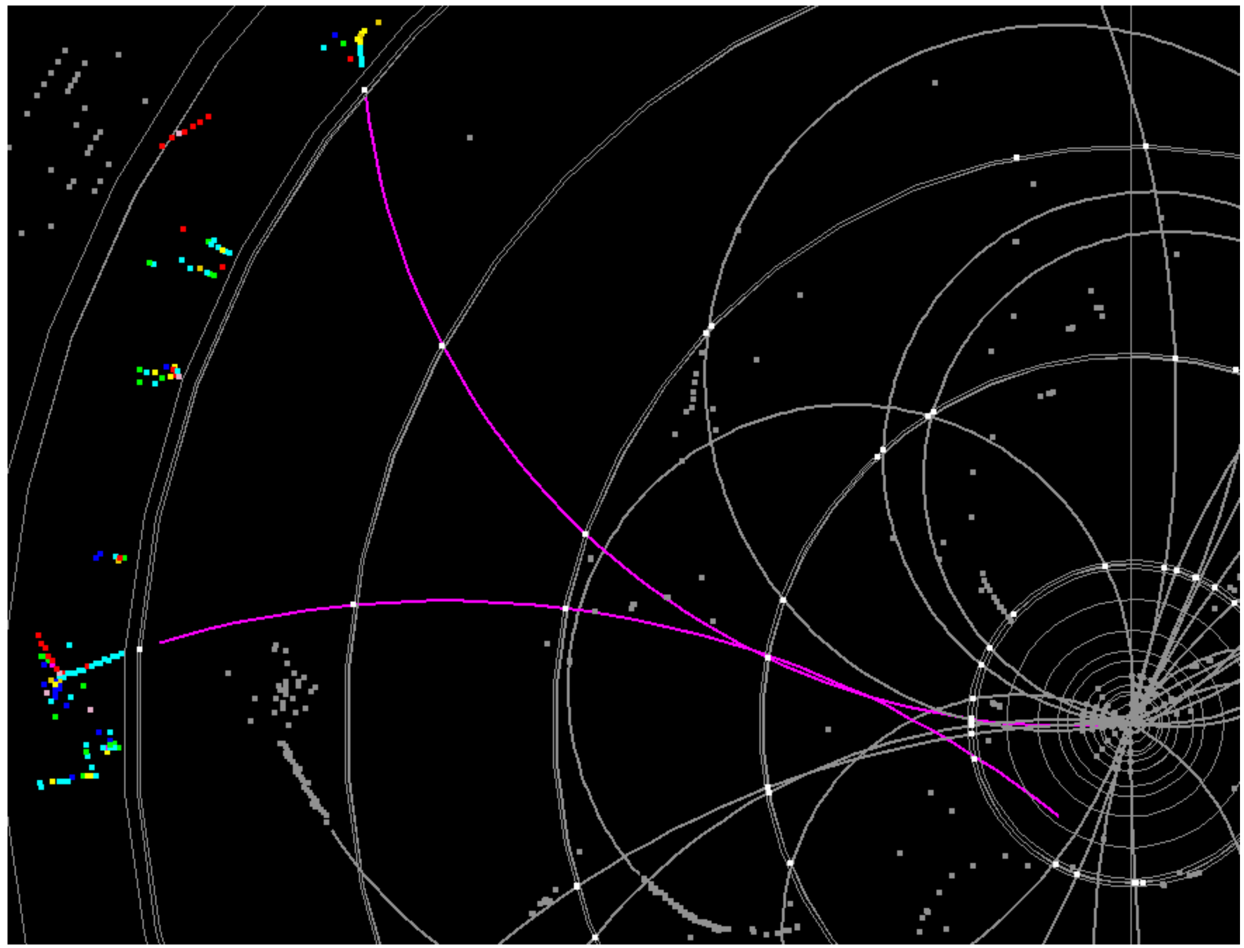
School of Electric Engineering and Computing Science, Seoul National University

Sungkyunkwan University - Suwon

"Imaging Calorimeters"



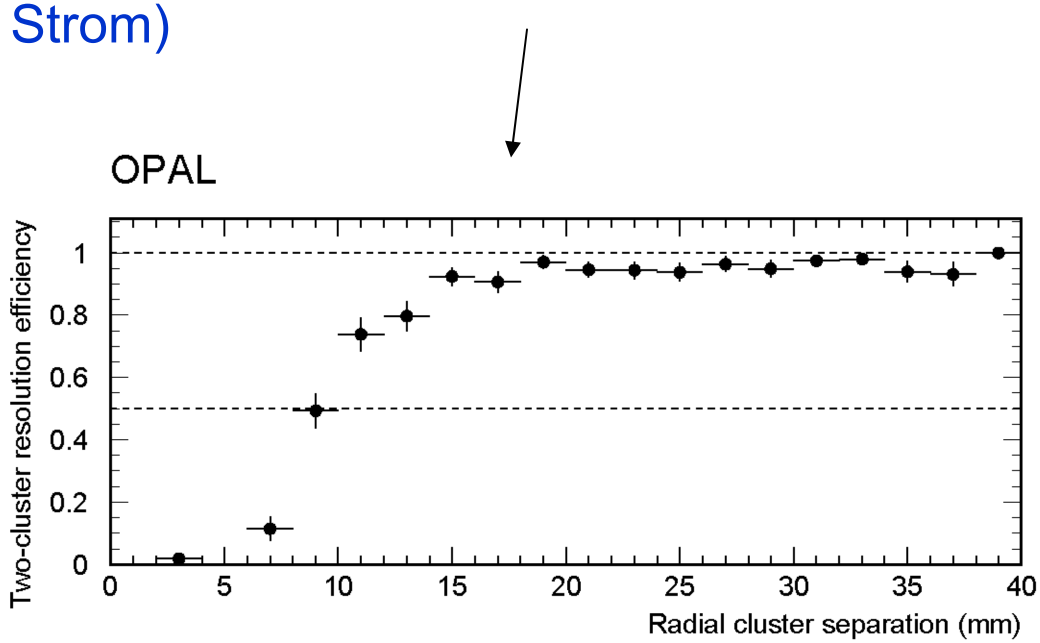
A highly segmented ECal is part of the overall detector tracking (charged and neutrals)



Segmentation requirement

- In general, we wish to resolve individual photons in jets, tau decays, etc.
- The resolving power depends on Moliere radius and segmentation.
- We want segmentation significantly smaller than R_m

Two EM-shower separability in LEP data with the OPAL Si-W LumCal (David Strom)

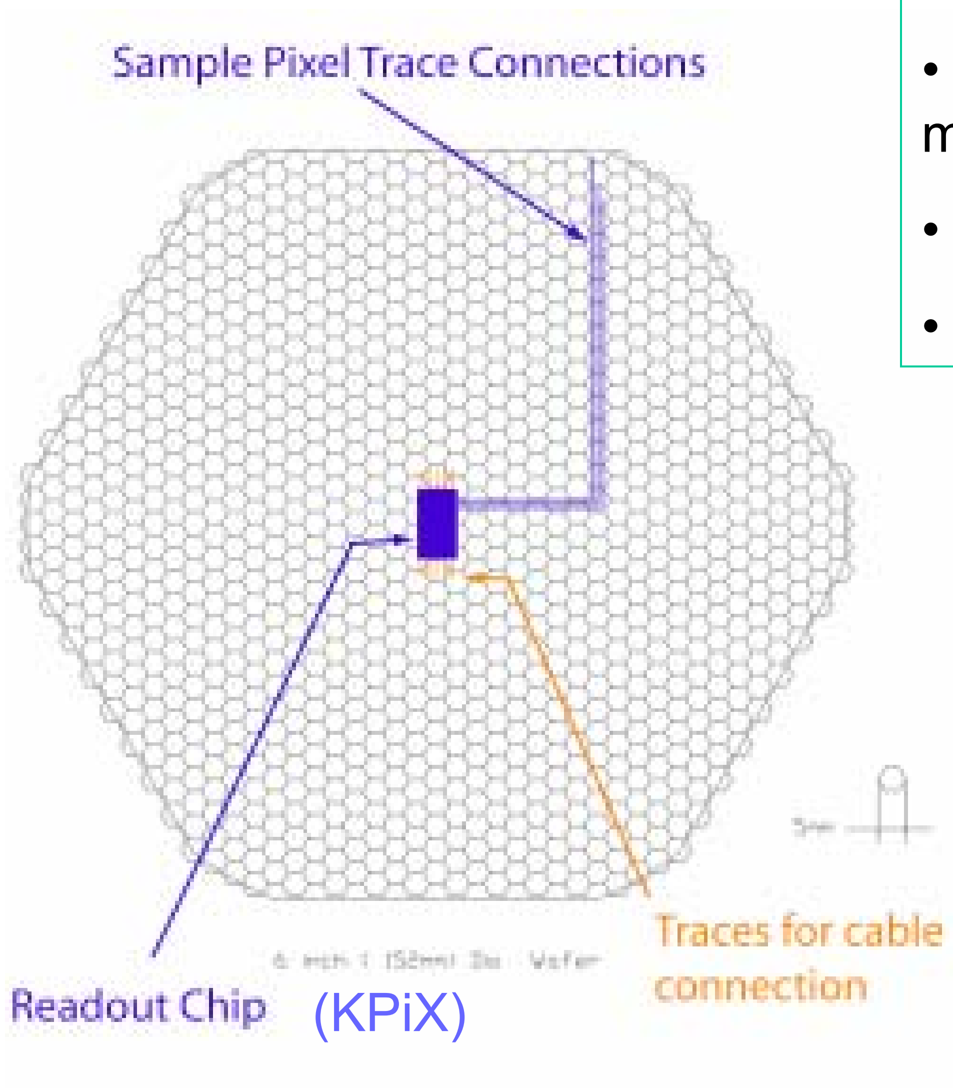


$$f_E \simeq \frac{R_{cal}}{\sqrt{R_M^2 + (4d_{pad})^2}}$$

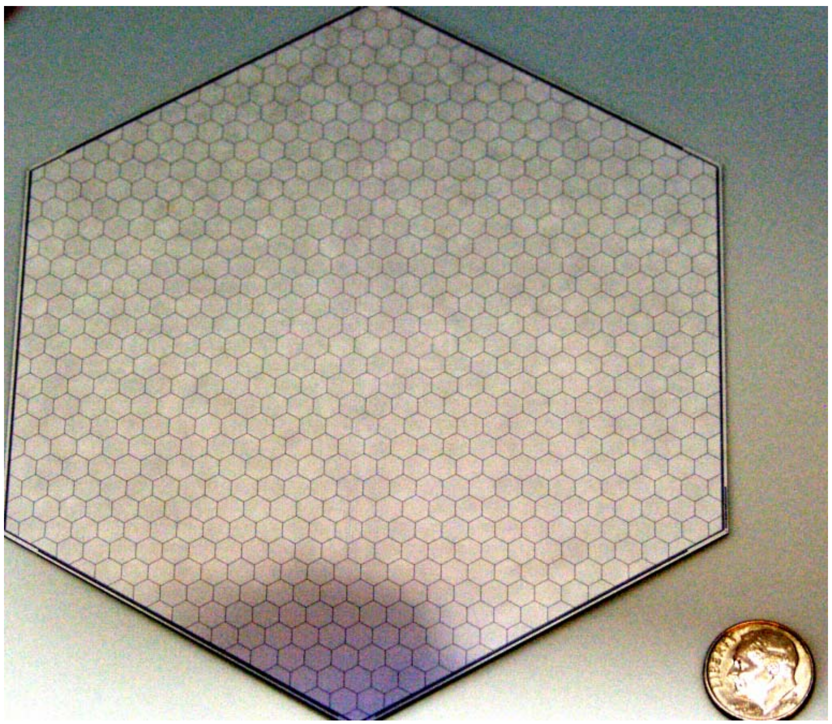
$$d = 2.5\text{mm} \ , \ R_M \sim 17\text{mm}$$

Silicon detector layout and segmentation – U.S.

- Silicon is easily segmented
- KPiX readout chip is designed for 12 mm^2 pixels (1024 pixels for 6 inch wafer)
- Cost nearly independent of seg.
- Limit on seg. from chip power (≈2 mm^2)



Fully functional prototype (Hamamatsu)



MAPS-based ECAL Design

Valencia

Features of the Monolithic Active Pixel Sensor (MAPS) -based calorimeter:

- **Binary readout**: hit or no hit per pixel (1-bit ADC)
- Pixels are small enough to ensure low probability of more than one particle passing through a pixel
- With ~100 particles/mm^2 in the shower core and 1% probability of double hit the pixel size should be ~40 μm×40 μm
  - **Current design with 50 μm×50 μm pixels** – see Yoshi Mikami's talk
- Timestamps and hit pixel numbers stored in memory on sensor
- Information read out in between trains
- Total number of ECAL pixels around 8×10^{11}: Terapixel system
- Only monolithic designs can cope with that number of pixels – hence MAPS

Konstantin Stefanov

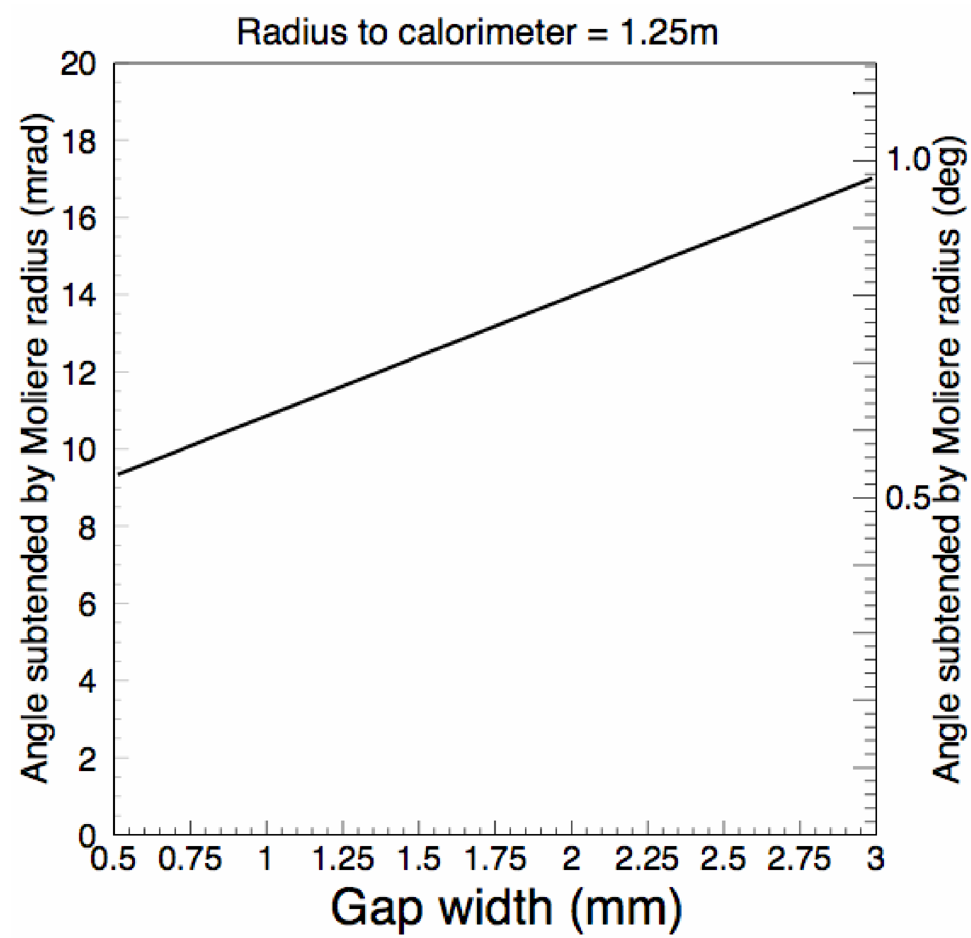
On behalf of

J. Crooks, P. Dauncey, A.-M. Magnan, Y. Mikami, R. Turchetta, M. Tyndel, G. Villani, N. Watson, J. Wilson

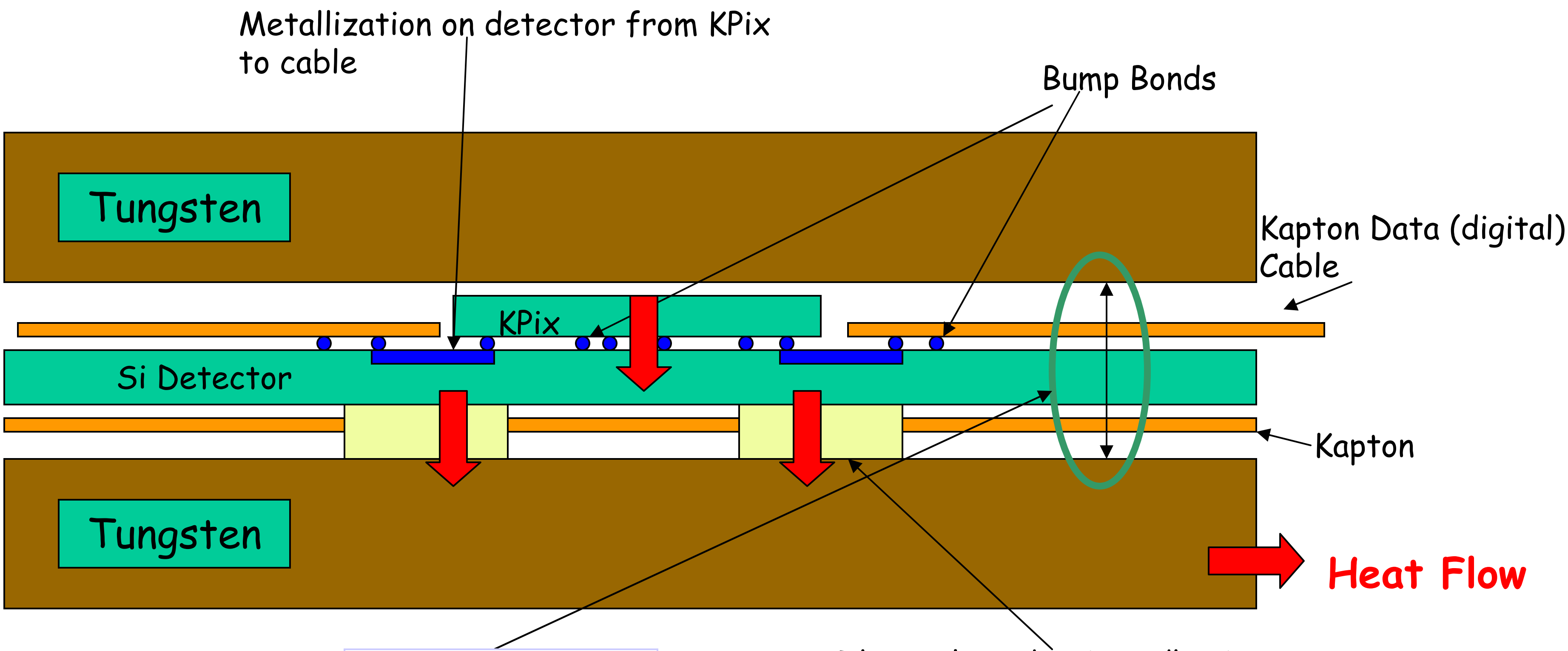
Critical parameter for R_M is the gap between layers

Config.	Radiation length	Molière Radius
100% W	3.5mm	9mm
92.5% W	3.9mm	10mm
+1mm gap	5.5mm	14mm
~~+1mmCu~~	~~6.4mm~~	~~17mm~~

Assumes 2.5mm thick tungsten absorber plates

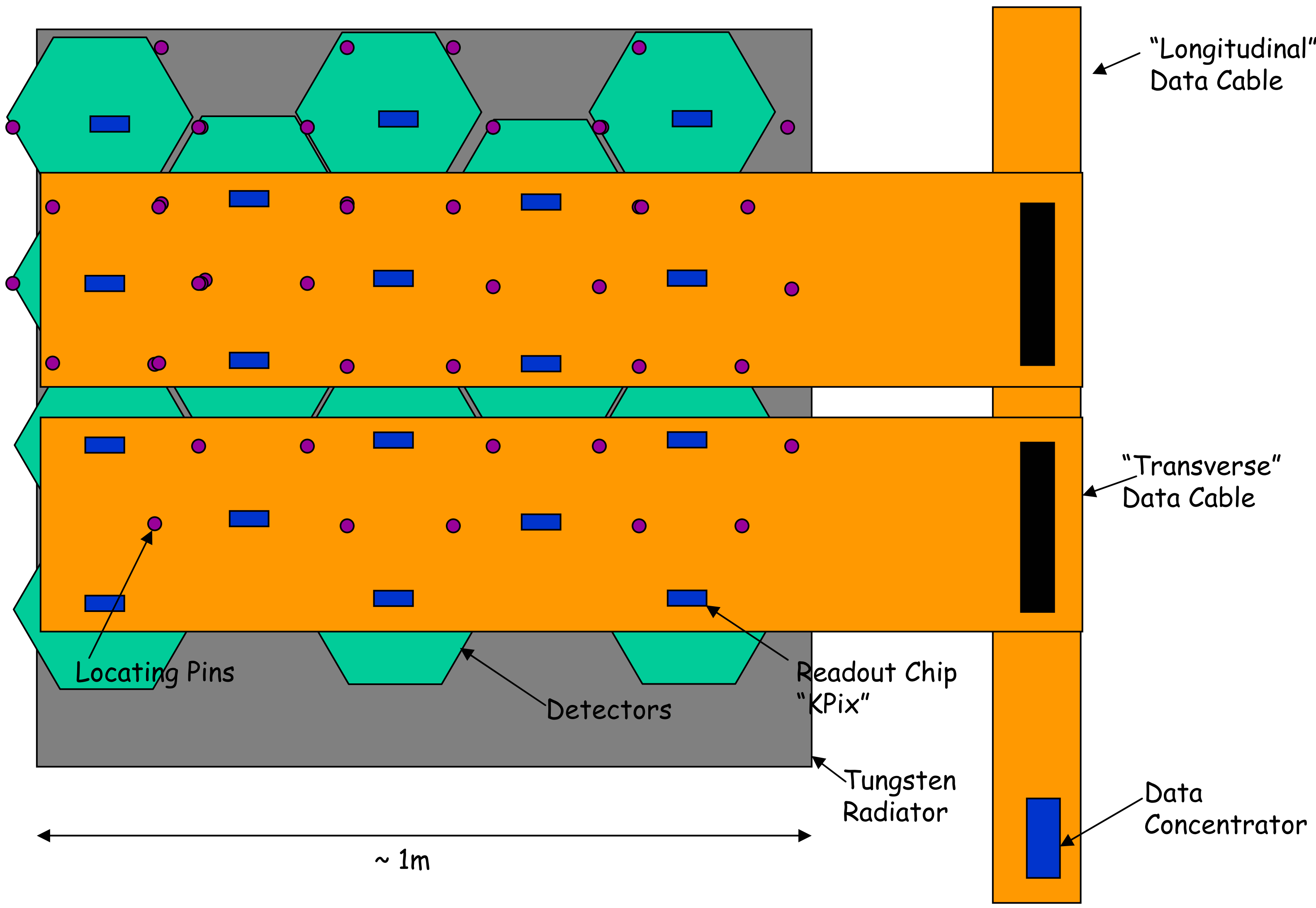


US Si-W readout gap schematic cross section



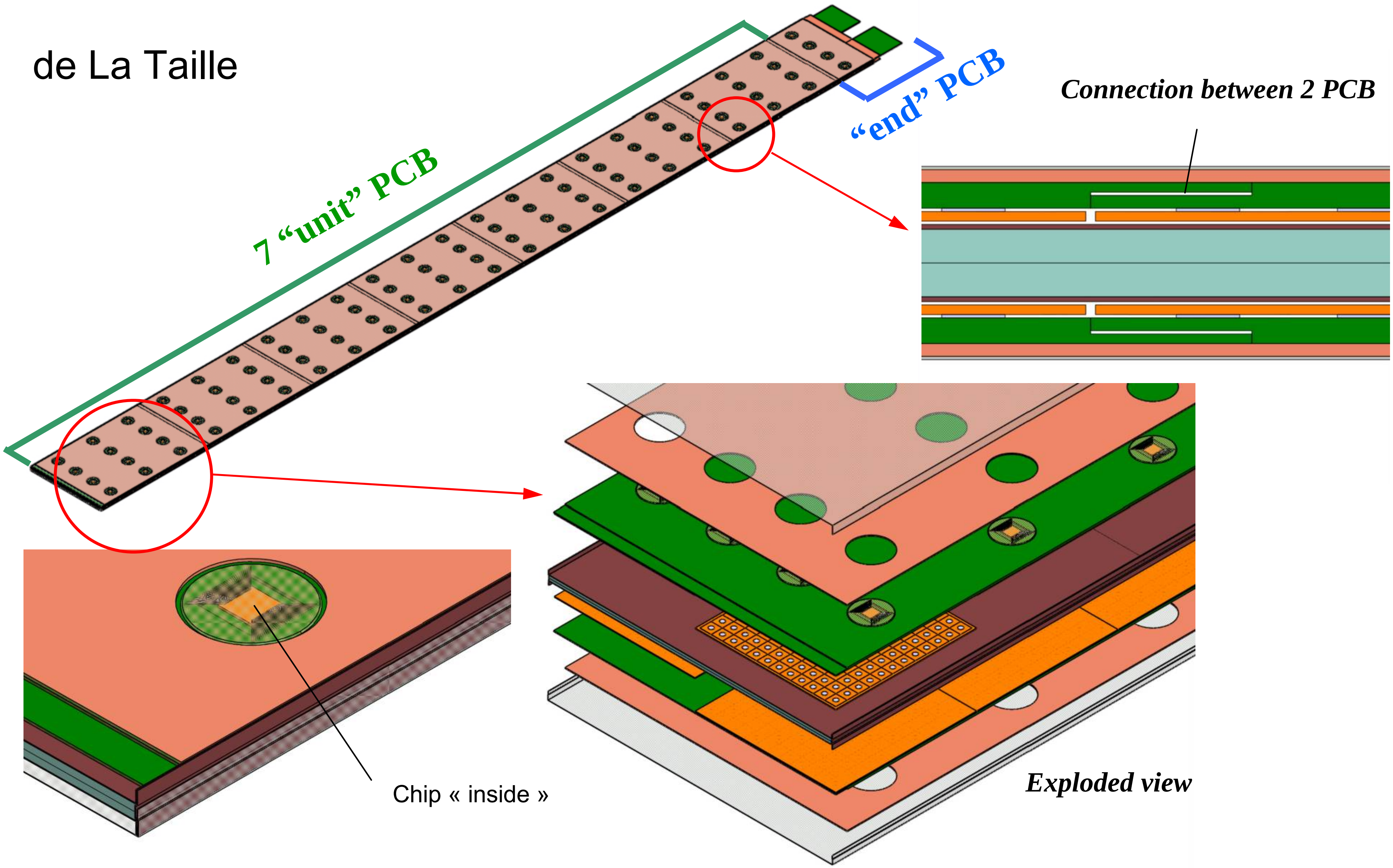
Gap ≤ 1 mm

Conceptual Schematic – Not to any scale!!!

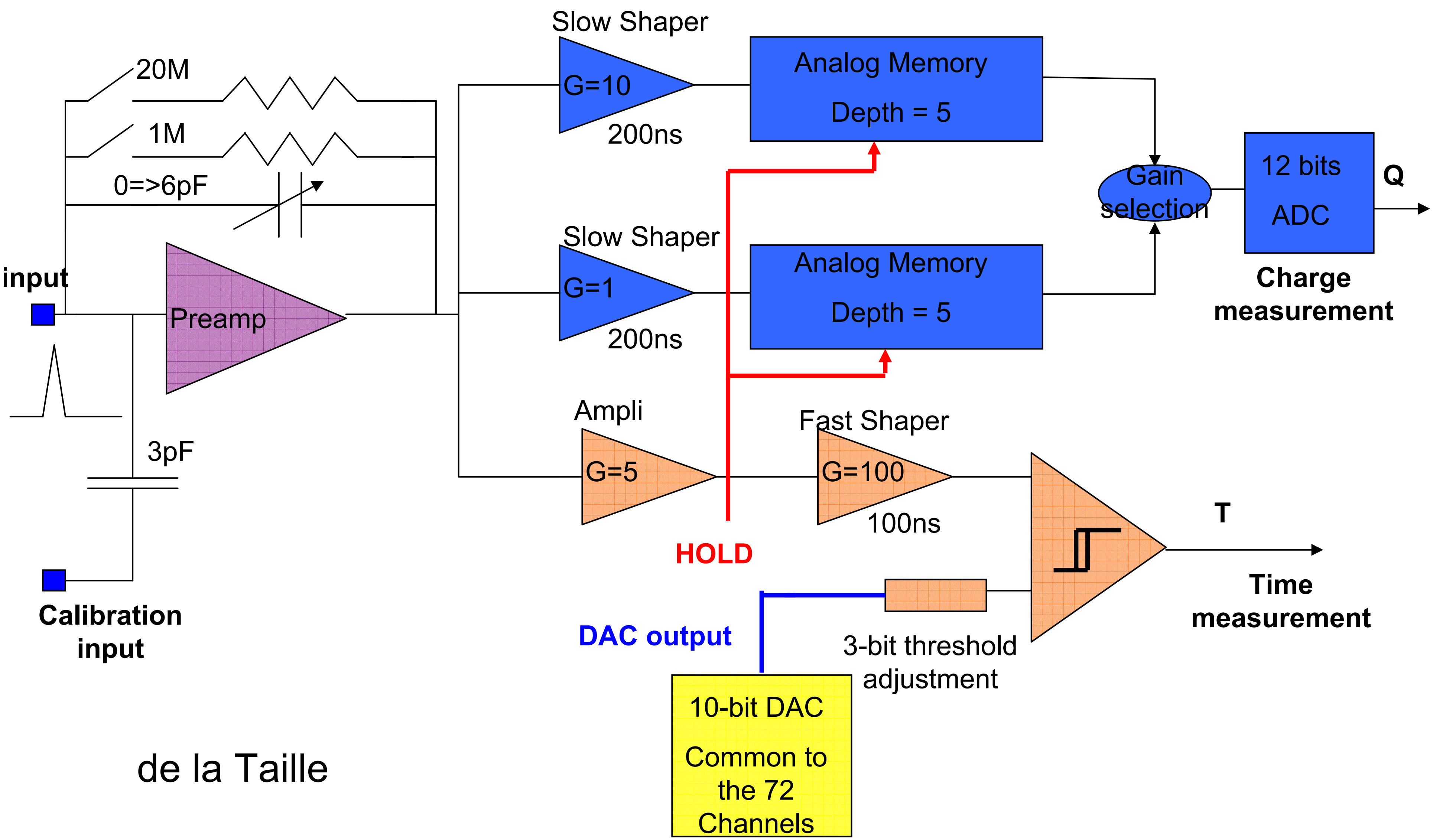


EUDET - Detector slab (2)

de La Taille



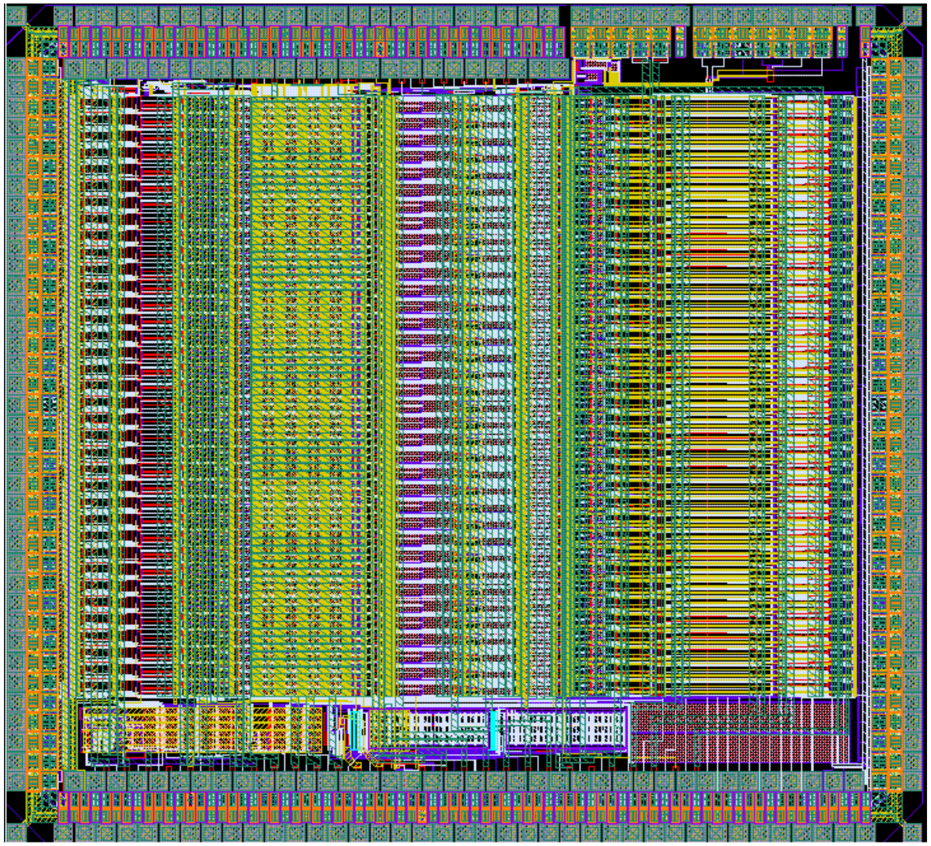
One channel

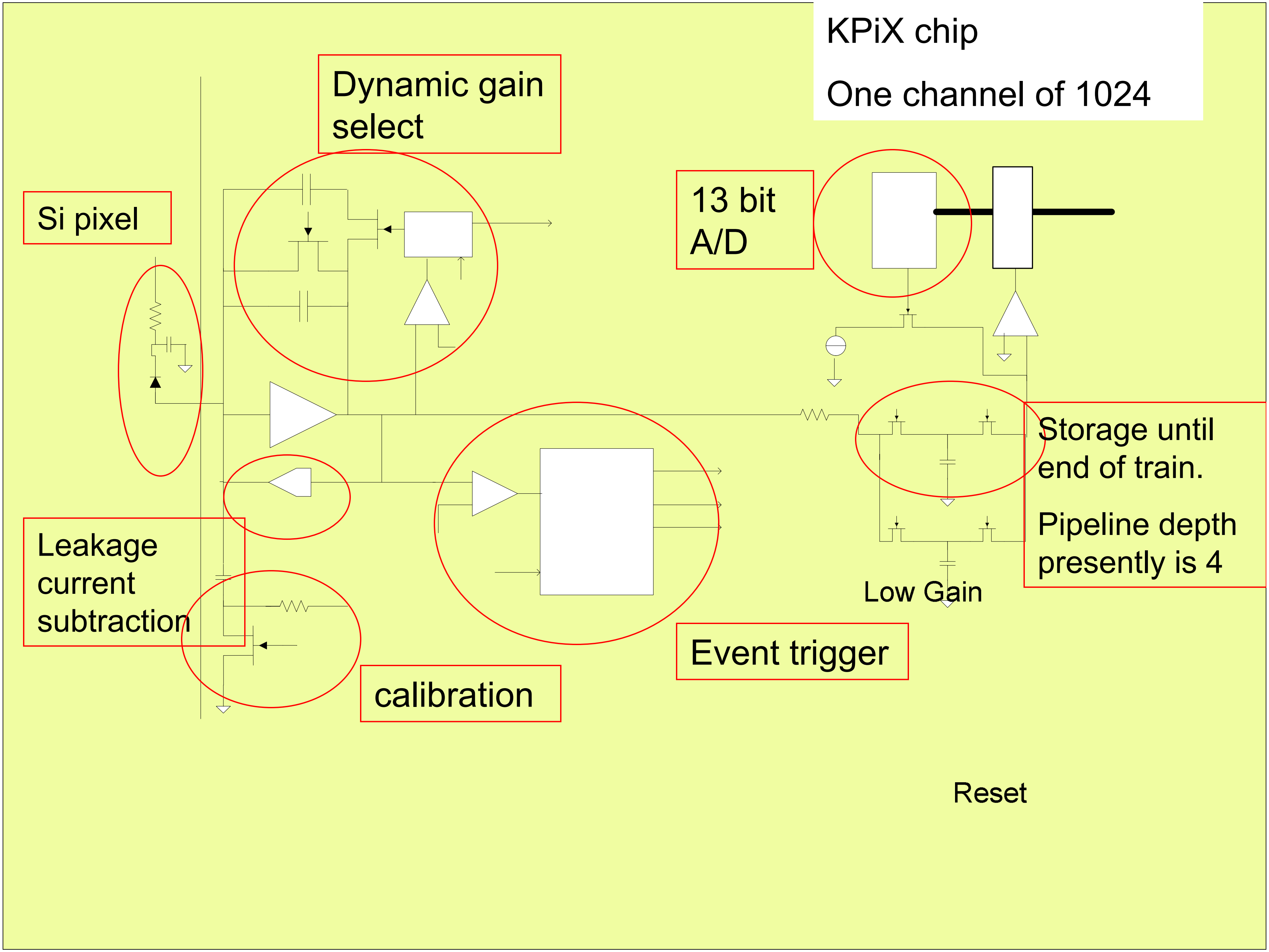


de la Taille

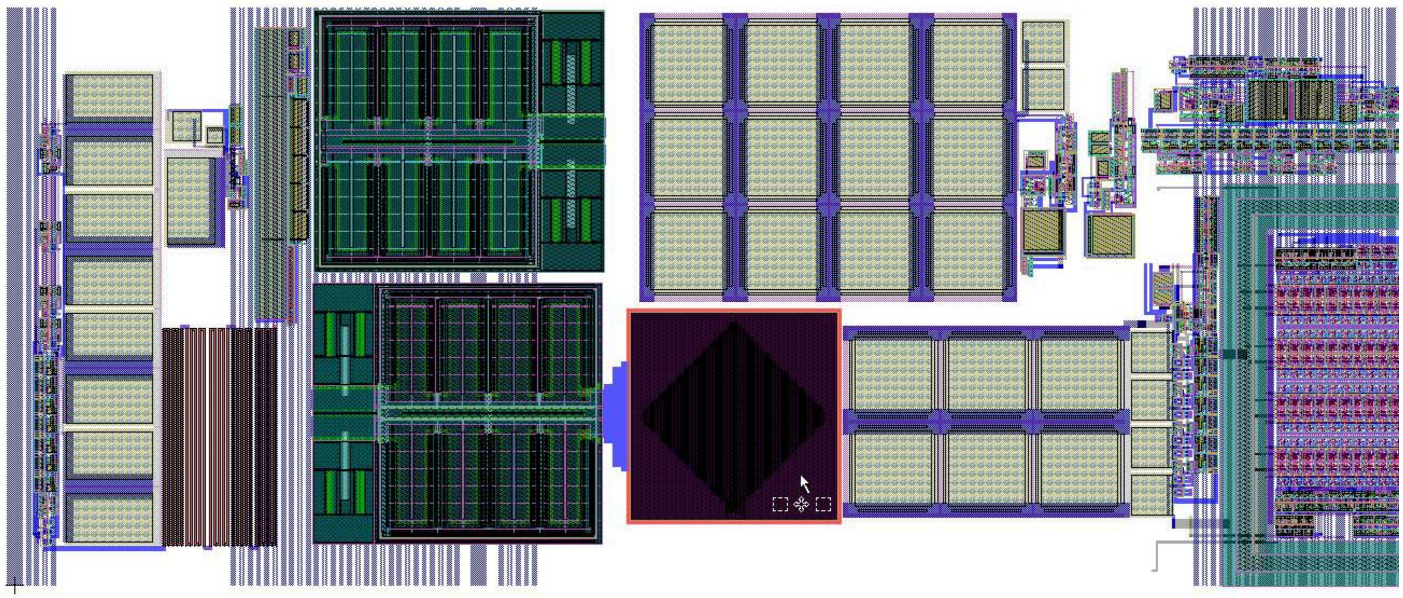
SKIROC for W-Si ECAL

- Silicon Kalorimeter Integrated Read Out Chip (Nov 06)
- 36 channels with 16 bits Preamp + bi-gain shaper + autotrigger + analog memory + Wilkinson ADC
- Digital part outside in a FPGA for lack of time and increased flexibility




KPiX chip
One channel of 1024
Dynamic gain select
Si pixel
13 bit A/D
Storage until end of train.
Pipeline depth presently is 4
Low Gain
Leakage current subtraction
Event trigger
calibration
Reset

KPiX Cell 1 of 1024



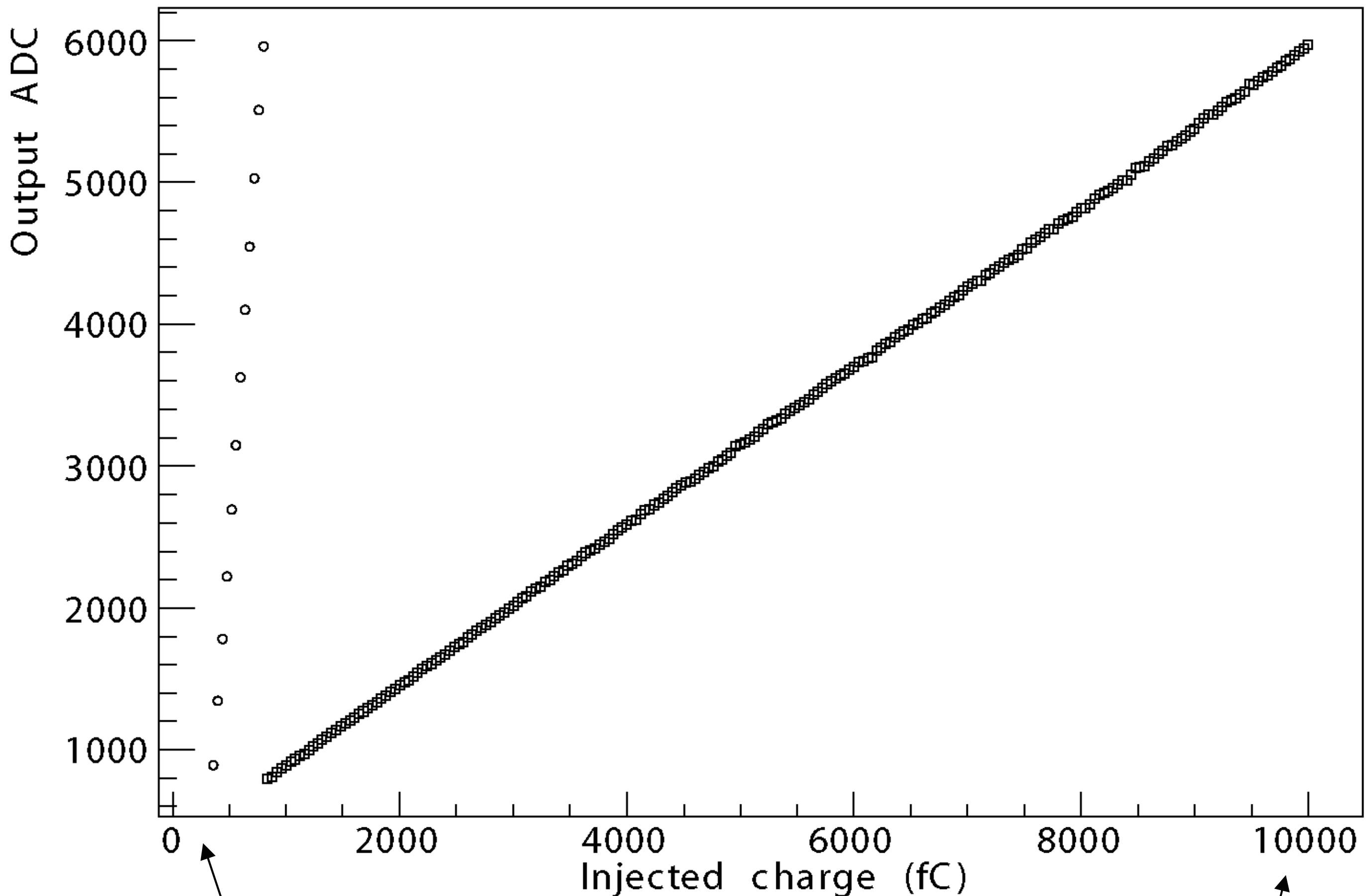
64-channel prototypes:

- v1 delivered March 2006
- v4 delivered Jan 16, 2007

It’s a complicated beast – may need a v5 before going to the full 1024-channel chip ?

Dynamic Range

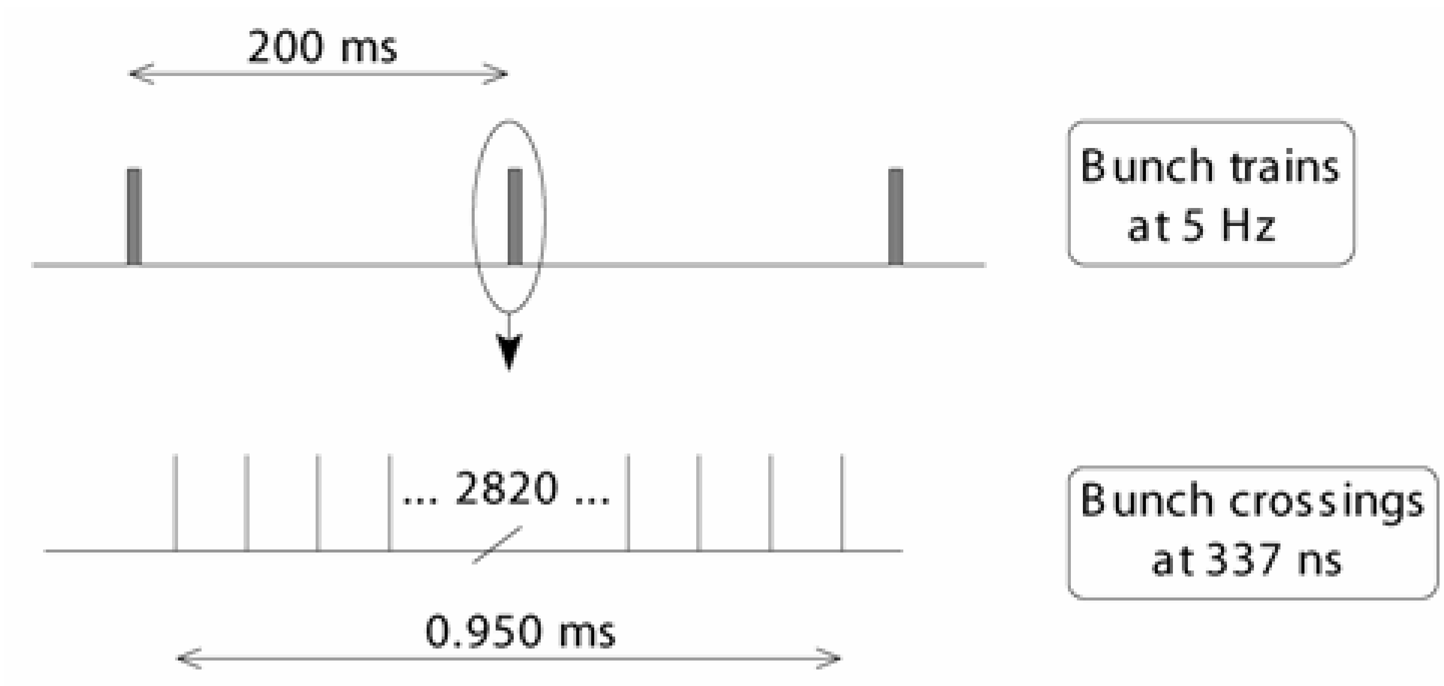
KPiX-2 prototype on the bench



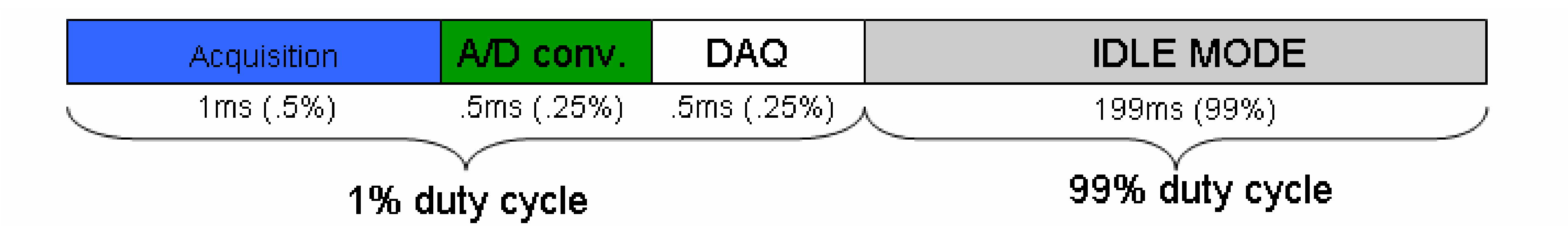
1 MIP (4 fC)

Max signal: 500 GeV electron

Power Pulsing



de La Taille



KPiX Power

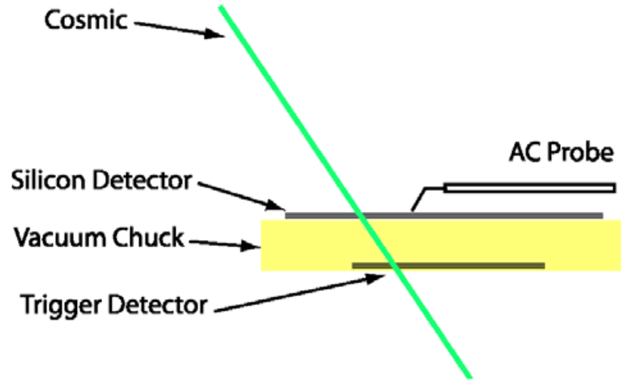
			Cold Train/Bunch Structure				
Phase	**Current (ma)**	**Instantaneous Power (mw)**	**Time begin (us)**	**Time End (us)**	**Duty Factor**	**Average Power (mw)**	**Comments**
All Analog "on"	370.00	930.00	0.00	1,020.00	5.10E-03	4.7	Power ok with current through FET's
Hold "on", charge amp off	85.00	210.00	1,021.00	1,220.00	9.95E-04	0.2	
Analog power down	4.00	10.00	1,020.00	200,000.00	9.95E-01	9.9	
LVDS Receiver, etc		3.00	0.00	200,000.00	1.00E+00	3.0	Receiver always on.
Decode/Program		10.00	1.00	100.00	4.95E-04	0.0	Sequencing is vague!
ADC		100.00	1,021.00	1,220.00	9.95E-04	0.1	
Readout		50.00	1,220.00	3,220.00	1.00E-02	0.5	
Total						18.5	Total power OK

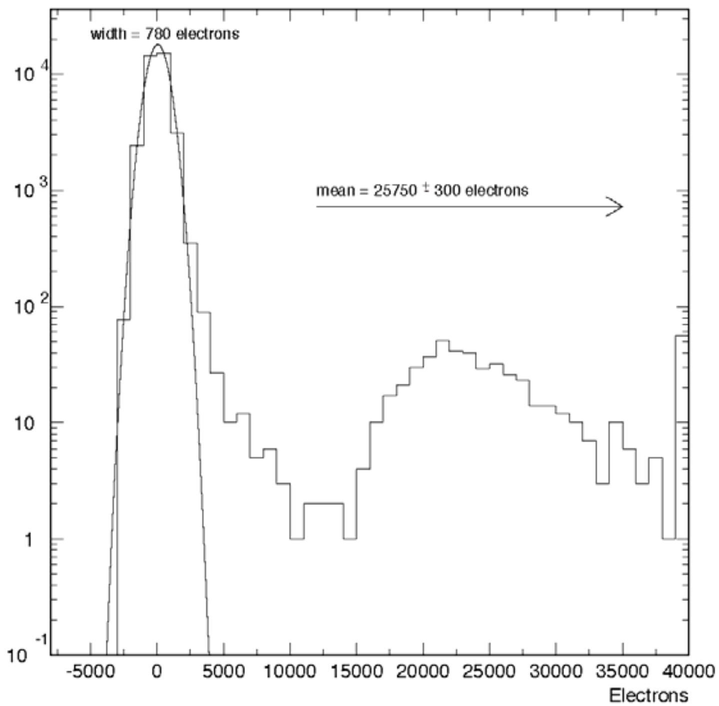
18 mW average power per 1024-channel chip

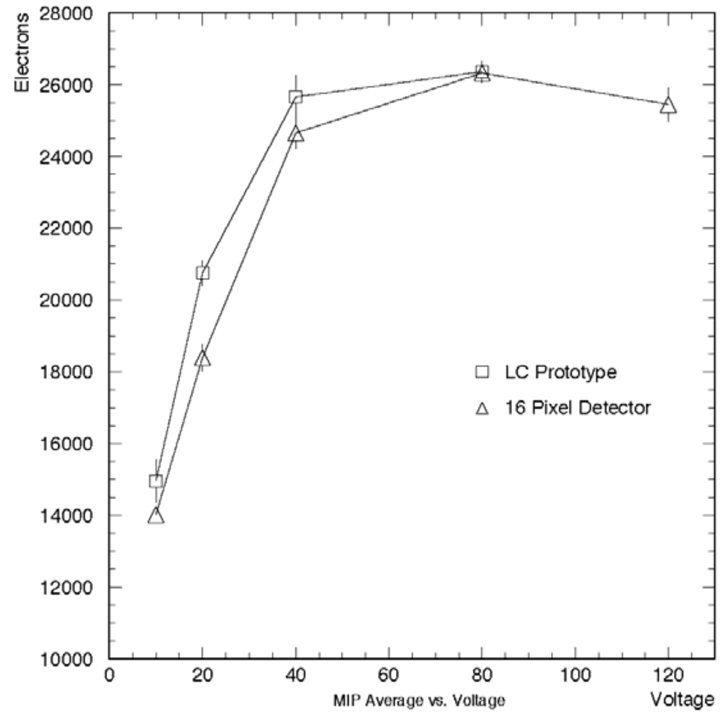
Passive-only cooling within the calorimeter seems to be OK.

prototype Si detector studies

Response of detectors to Cosmics
(Single 5mm pixel)
Simulate LC electronics
(noise somewhat better)

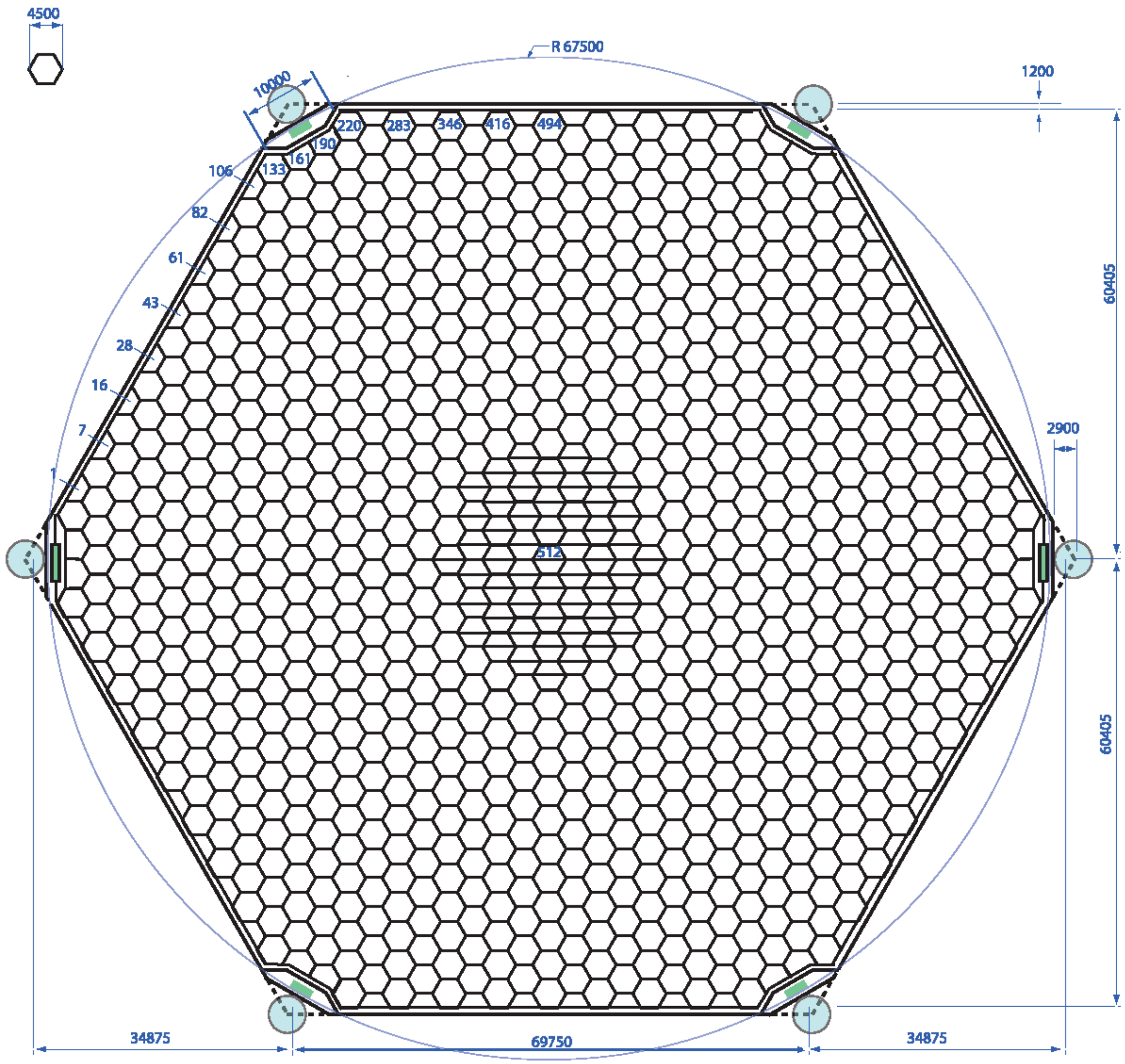






Errors do not include ~ 10% calibration uncertainty (no source calibration)

v2 US Si detector – for full-depth test module



- 6 inch wafer
- 1024 12 mm^2 pixels

ready to go except for funding

R&D Milestones – US Si-W

I. Connect (bump bond) prototype KPiX to prototype detector with associated readout cables, etc
  - Would benefit from test beam (SLAC?) - 2007
  - A "technical" test

II. Fabricate a full-depth ECal module with detectors and KPiX-1024 readout * – functionally ≈equivalent to the real detector
  - Determine EM response in test beam – 2008
  - Ideally a clean 1-30 GeV electron beam (SLAC?)

III. Test with an HCal module in hadron test beam (FNAL?) – 2008-?
  - Test/calibrate the hadron shower simulations; measure response

IV. Pre-assembly tests of actual ECal modules in beam – >2010

* *pending funding*

Test beam requirements (wishes)

For the initial testing (milestone I):

- nearly anything will do

For the EM response test (milestone II)

- Dedicated electron or positron beam
  - 1 – 30 GeV
  - Rate down to one (or zero) particles per bucket
  - Well-localized (~1 cm) beam
- Timing:
  - KPiX can run in an externally triggered mode
    - Buffer depth of 4
    - Requires about 3-6 ms to complete a DAQ cycle → expect dead time

For the test in the hadron beam line (milestone III):

- Sufficient quantity of electrons (low to high energy) to verify carry-over of response from the EM test, otherwise program mostly defined by HCal
- Will need a veto of transverse shower leakage out of the ECal (scintillators)

Summary

- The R&D leading to an "ILC-ready" Si-W ECal technology is progressing well.
  - The MAPs concept provides an interesting alternative
- The Si-W R&D should result in full-depth modules which will require test beam evaluation
  - The CALICE Eudet module (30 layers x 12cm x 150cm) - 2009
  - The US Si-W module (30 layers x 16cm x 16cm) - 2008*
- These highly segmented, analog devices should provide an interesting test for simulation modeling of (early developing) hadron showers.
  - May be crucial for understanding the HCal
- As we transition from R&D to "D" (>2010), there will certainly be a need for pre-assembly tests of the real ECal modules.