DHCAL Progress and Test Beam Preparation

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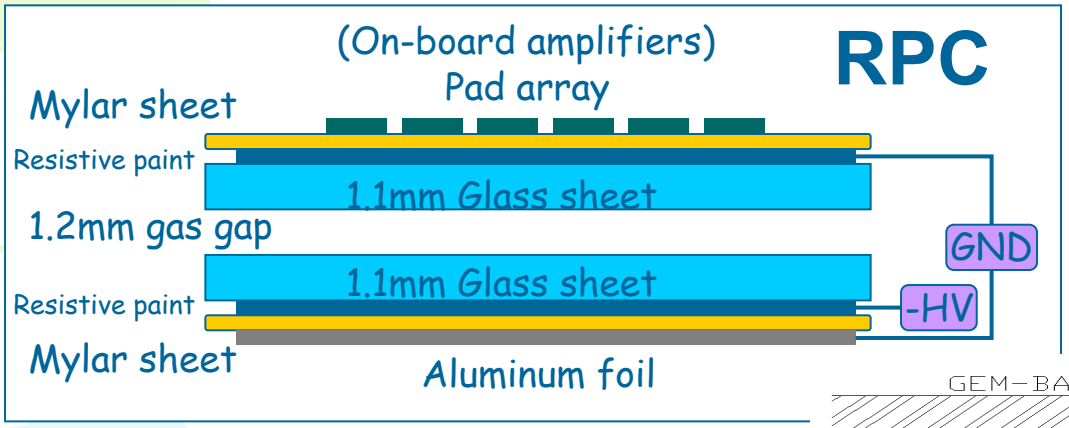
ANL-HEP

CALICE
Calorimeter for ILC

Introduction

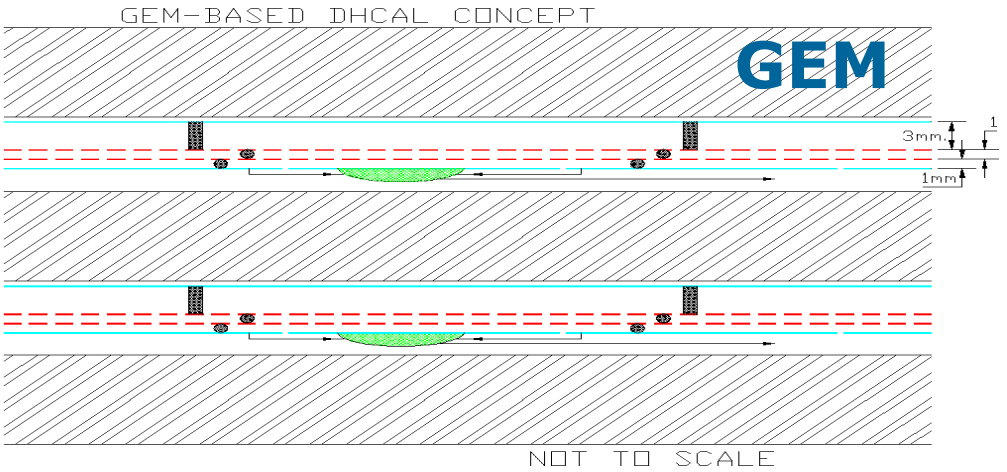
- Particle Flow Algorithm (PFA)
  - Is widely believed to be THE way to achieve precise jet measurement at the ILC
  - Demonstrated ~3GeV jet energy resolution at Z-pole
    - Two-jet events with light quarks (Geant4 simulation)
    - Higher CM energy study is in progress
  - Key issue is particle separation in the calorimetry
  - HCal single particle energy resolution is less important
- Digital Hadron Calorimeter (DHCal)
  - Provide fine segmentation (~1cm^2) which makes pattern recognition easier
  - Simplifies readout system
  - Simplifies detector calibration
  - Single particle energy resolution is pretty good (Geant4 simulation)

Active Medium Candidates

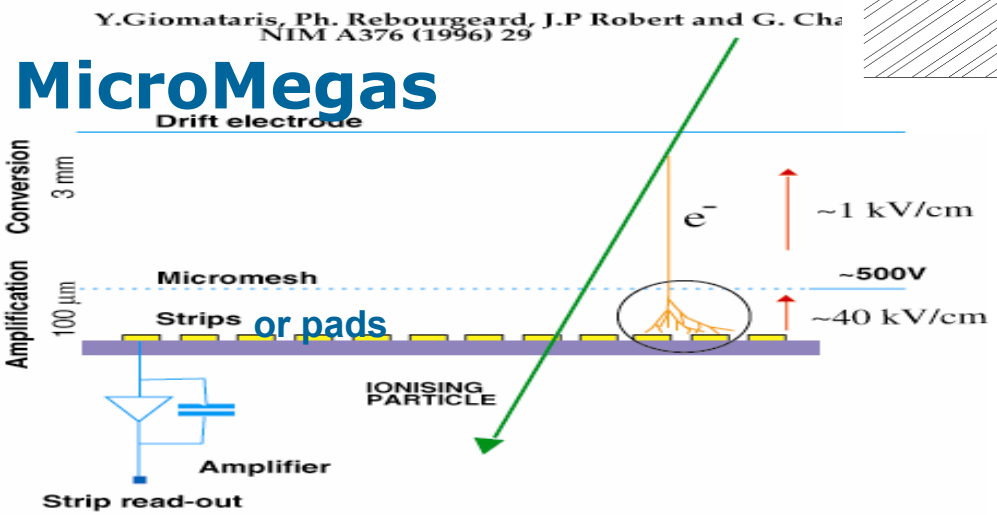


European Group:
IHEP (Protvino) + collaborators

US Group:
Argonne + collaborators



UTA + collaborators



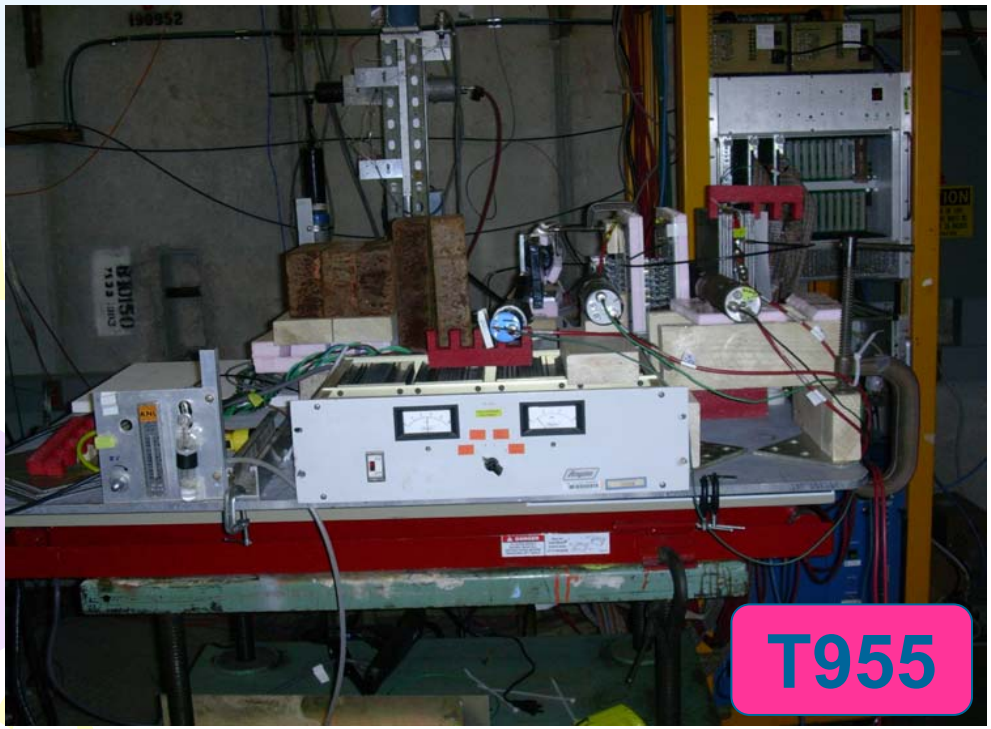
LAPP (Annecy) + collaborators

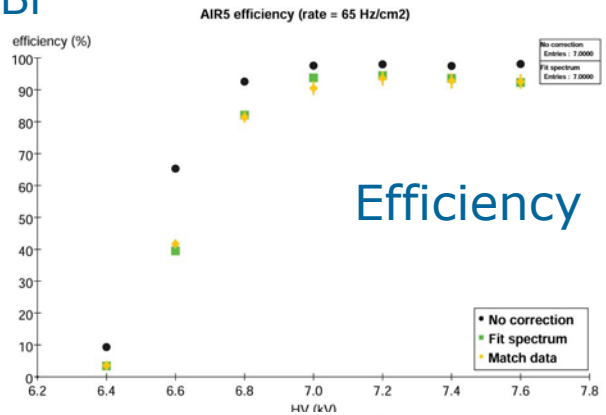
Active medium R&D status

Measurement	European RPC	US RPC	GEM	mMegas
Signal characterization	yes	yes	yes	yes
HV dependence	yes	yes	yes	yes
Single pad efficiencies	yes	yes	yes	
Geometrical efficiency	yes	yes		
Tests with different gases	yes	yes	yes	
Mechanical properties	?	yes		
Multipad efficiencies	yes	yes	ongoing	
Hit multiplicities	yes	yes	ongoing	
Noise rates	yes	yes	ongoing	
Rate capability	yes	yes		
Tests in 5 T field	yes	no	no	
Tests in particle beams	yes	yes	ongoing	planned
Long term tests	ongoing	ongoing	ongoing	
Design of larger chamber	yes	yes	ongoing	ongoing
Overall R&D	**Done**	**Done**	**Ongoing**	**Started**

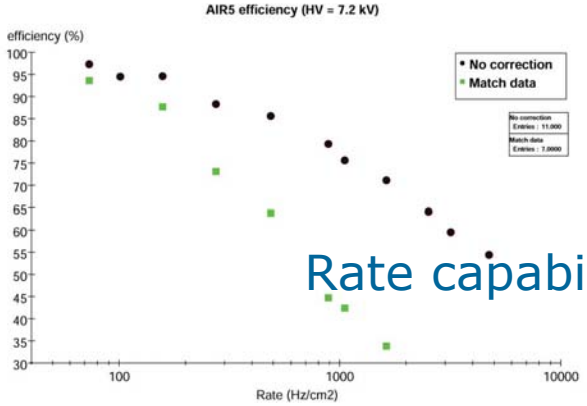
RPC chamber beam test

- European RPC effort
  - Chamber in beam test 2002 (IHEP, Protvino)
  - RPC characteristics study: efficiency, hit multiplicity, rate capability, etc
- US RPC effort
  - 3 RPC's (2 RPC designs, 2 readout) tested at Fermilab MTBF (Feb, 2006)
  - Tested with Muon, Pion and Proton beams
  - RPC characteristics study: efficiency, hit multiplicity, rate capability, etc
  - All test results consistent with cosmic ray tests at ANL
  - Very positive experience with Fermilab MTBF





Efficiency

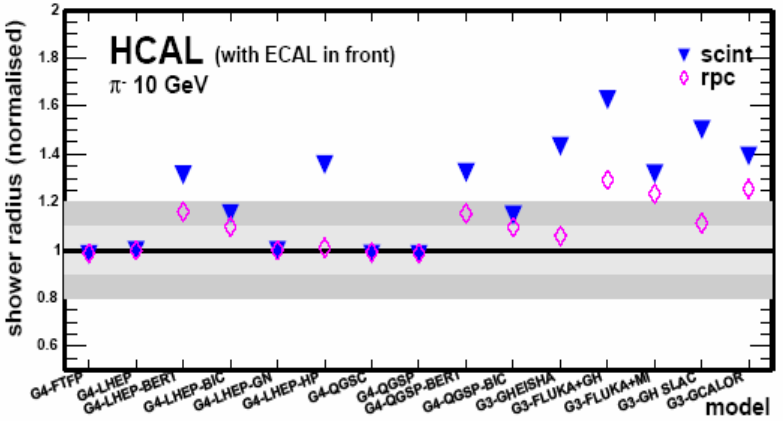


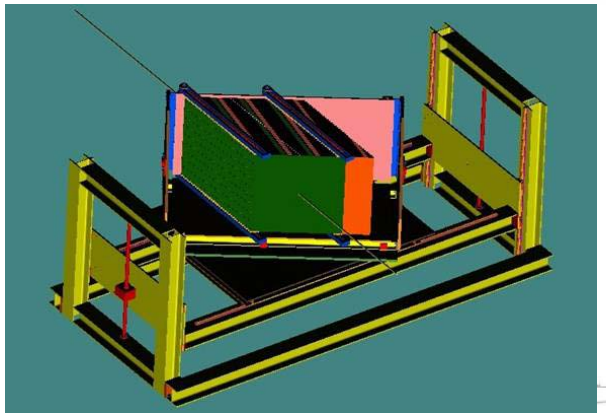
Rate capability

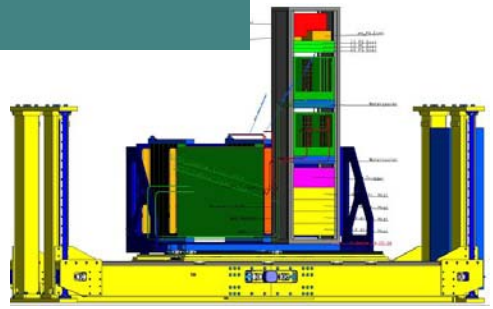
Big goal: 1m³ prototype section

- Motivation for Prototype Section(PS) and beam tests
  - validate RPC and GEM approach (technique and physics)
  - Validate concept of the electronic readout
  - Measure hadronic showers with unprecedented resolution
  - Validate MC simulation of hadronic showers
  - Compare with results from Scintillator HCAL
- Details of the PS:
  - 1 m³ (to contain most of hadronic showers)
  - 40 layers with 20 mm steel plates as absorber
  - Lateral readout segmentation: 1x1 cm²
  - Longitudinal readout segmentation: layer-by-layer
  - Instrumented with Resistive Plate Chambers (RPCs) and Gas Electron Multipliers (GEMs)
- Biggest challenge:
  - Readout ~400,000 channels

Comparison of hadron shower simulation codes by G Mavromanolakis







DHCal test beam plan

- US RPC + GEM: staged approach
  - Feb.- Mar. 2007: GEM chamber characteristics run at Fermilab MTBF
    - This will be done using 100 channel ADLink PCI based DAQ card
  - April 2007: “slice test” at Fermilab MTBF
    - Slice test: mini-calorimeter stack (~10 layers)
      - Active medium: 8 RPCs + 2 GEMs, 16x16cm^2 active area in each chamber
      - Absorber: 4mm copper + 16mm steel
    - Validate DCAL chip + readout system for prototype section
      - Readout system as close as possible to the 1m^3 prototype section
    - Limited data/simulation comparison
    - 2 additional GEMs will be tested with KPix chip, 8x8cm^2 active area
  - Later 2007:
    - RPC: finish slice test, analyze data, prepare for prototype section
  - 2008: construction and test of prototype section (if funding permits)
    - Construct 1st prototype section: RPC + DCAL readout
      - European RPC effort: join the effort and supply part of the RPC’s
    - Detailed test program in Fermilab test beam
    - Construct 2nd prototype section: GEM + ? Readout
- MicroMegas
  - 2007: construct 1 50x50cm^2 chamber for beam test
  - 2008: construct 1 layer of 100x100cm^2 prototype

Readout system for PS: conceptual design

Conceptual Design of the Readout System
for the
Linear Collider Digital HCAL Prototype Detector

John Dawson, Gary Drake, Bill Haberichter,
Jose Repond, Dave Underwood, Lei Xia
Argonne National Laboratory

John Butler, Menakshi Narain
Boston University

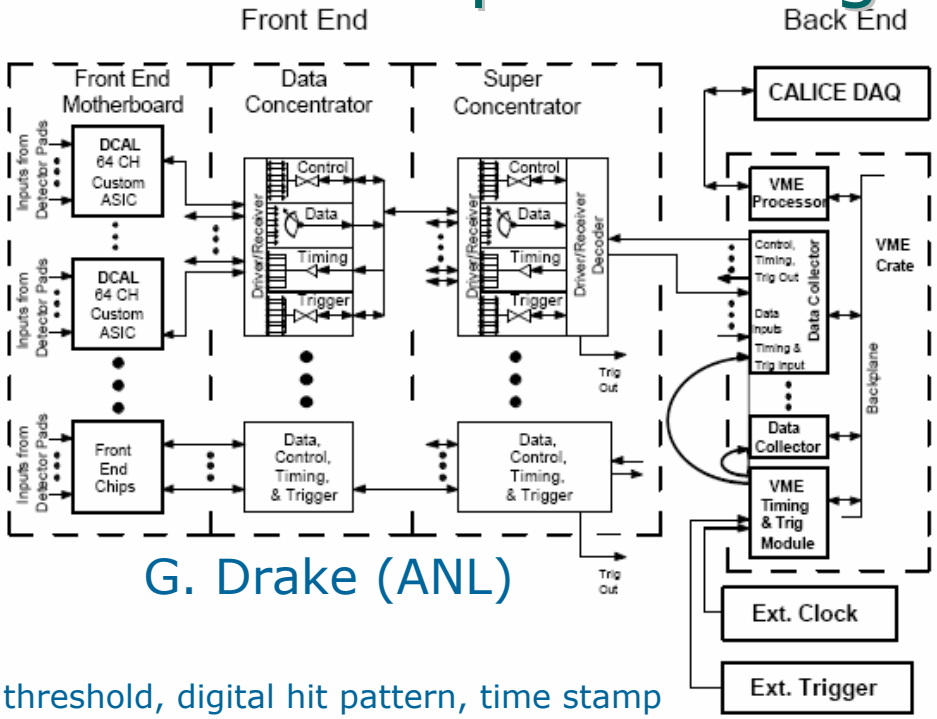
Mark Oreglia
University of Chicago

Jim Hoff, Abder Mekonani, Raymond Yarema
Fermi National Accelerator Laboratory

Edwin Nobeck, Yasar Onel
University of Iowa

Andy White, Jaehoon Yu
University of Texas - Arlington

Version 1.13
Sept. 12, 2005

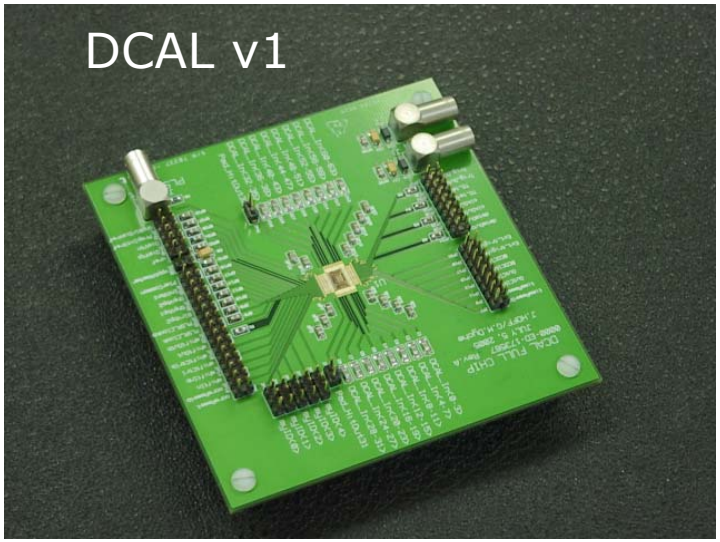


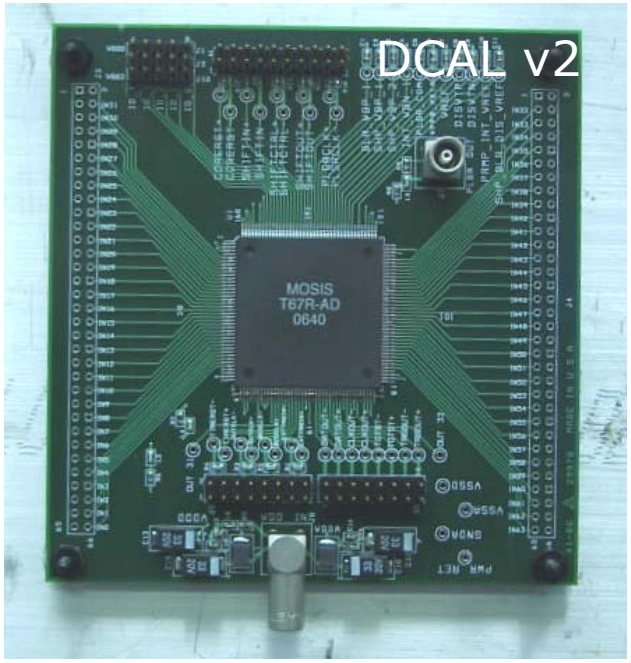
G. Drake (ANL)

- Front-end ASIC: DCAL chip
  - 64 channels, programmable threshold, digital hit pattern, time stamp
- Pad board
  - Slice test: 16x16 1cm^2 pads, 20x20cm^2(RPC)/30x30cm^2(GEM) in size with empty edges
  - PS: 32x48 1cm^2 pads, 32x48 cm^2 in size
- Front-end board
  - Same design for slice test and PS: hosts 4 DCAL chip, 16x16 pads, 16x16cm^2
  - Glued to pad board with conductive epoxy
- Data concentrator board
  - Slice test: 1/front-end board, take data from 4 DCAL chips
  - PS: take data from 3 FE boards, 12 DCAL chips
- Super concentrator:
  - Slice test: not used
  - PS: read 6 data concentrators, design similar to data concentrator
- Data collector: same design for slice test (1) and PS (7)
- Trigger and timing module: same design from slice test (1) and PS (1)

DCAL chip

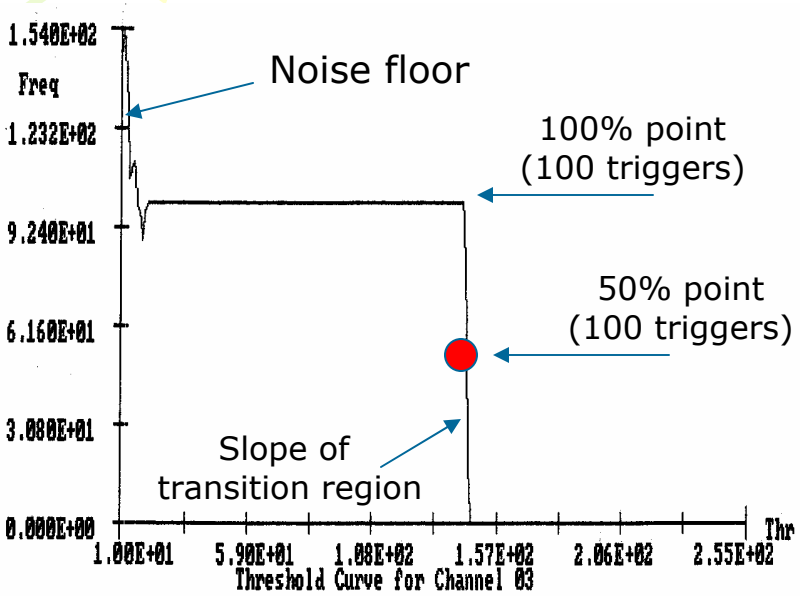
- DCAL specs
  - Developed to read out digital (hadron) calorimeter
  - 64 input channels
  - Two gains: low (RPC) high (GEM)
  - Triggerless or triggered operation
  - Output: hit pattern + timestamp (100ns resolution)
- History of development
  - Conceptual design: early 2004 by ANL
  - Design started at FNAL: June 2004
    - A Mekkaoui, J Hoff, R Yarema
  - 1st submission: March 2005
    - Extensively tested, all functions performed as expected
  - Redesign:
    - Decrease gain by factor of 20(GEM) and 100(RPC)
    - Decoupling of clocks (readout and front-end)
  - 2nd submission: July 2006
    - 40 (packaged) chips in hand, being tested
- Tests done by the end of 2006
  - Read/write registers
  - Test of pipeline with ext. triggers
  - Threshold tests using on-board Q-inj: H-Gain
  - Threshold tests using on-board Q-inj: L-Gain
  - Tests of noise floor



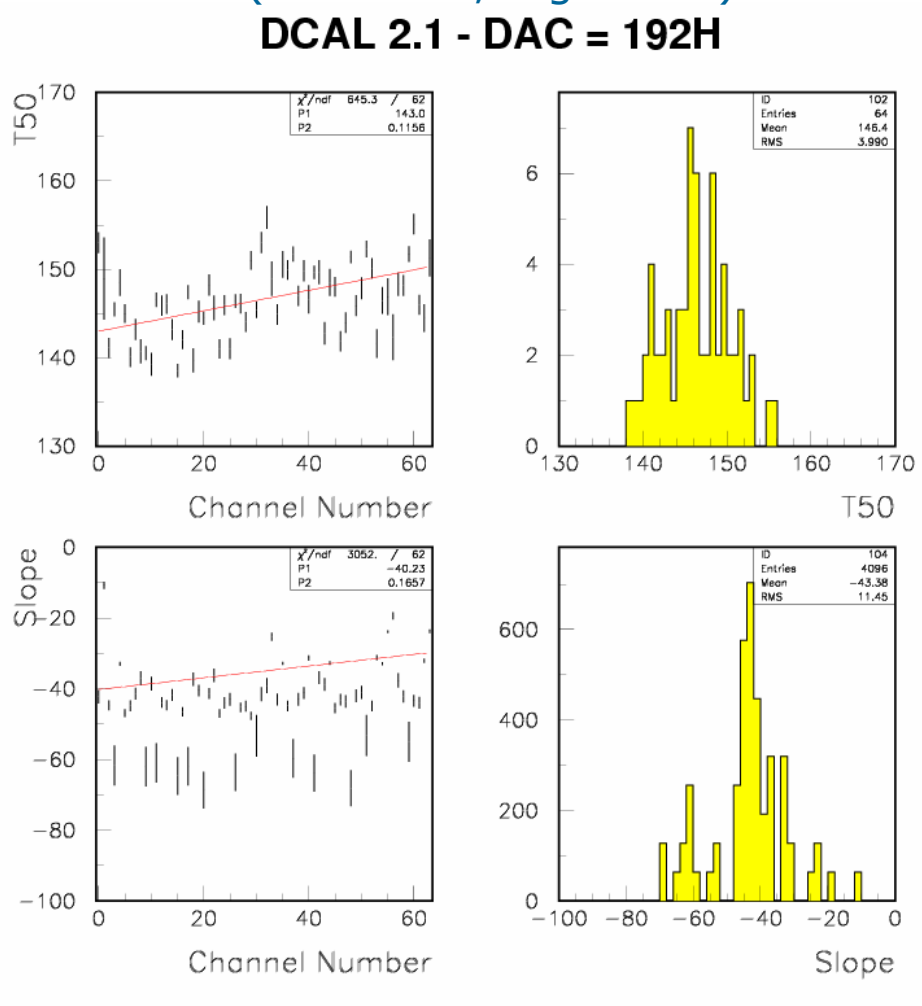


DCAL test (1)

Threshold Response Tests
Typical Channel
(DAC=192, High-Gain)
On-board Q-inj, ext. trig., pipeline enabled

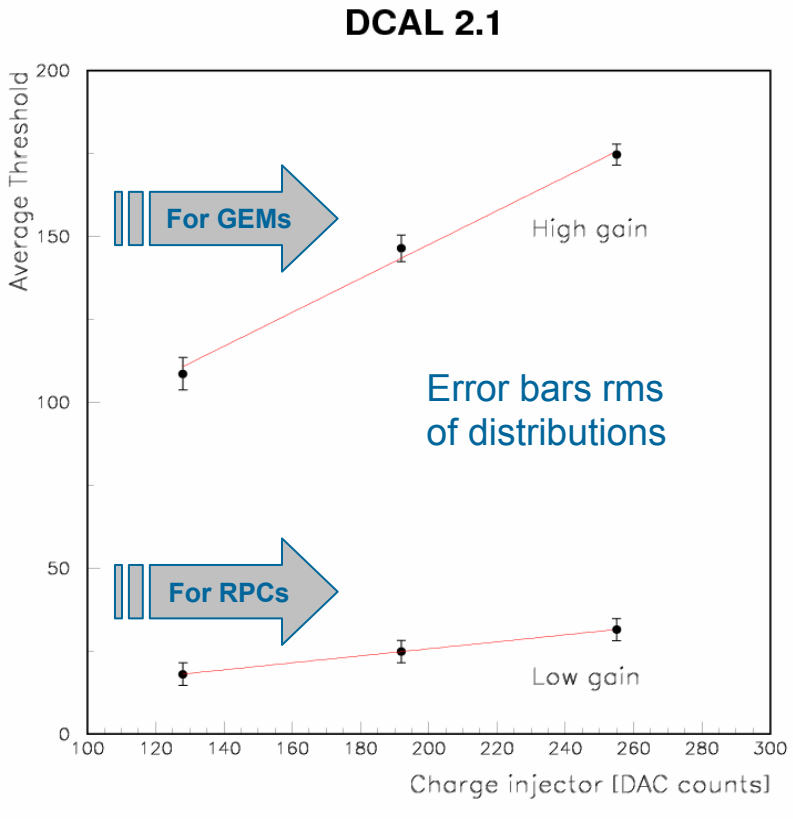


Summary for All Channels
(DAC=192, High-Gain)



All channels OK, except
Channel #31, 32 are noisier (understood)

DCAL test (2)

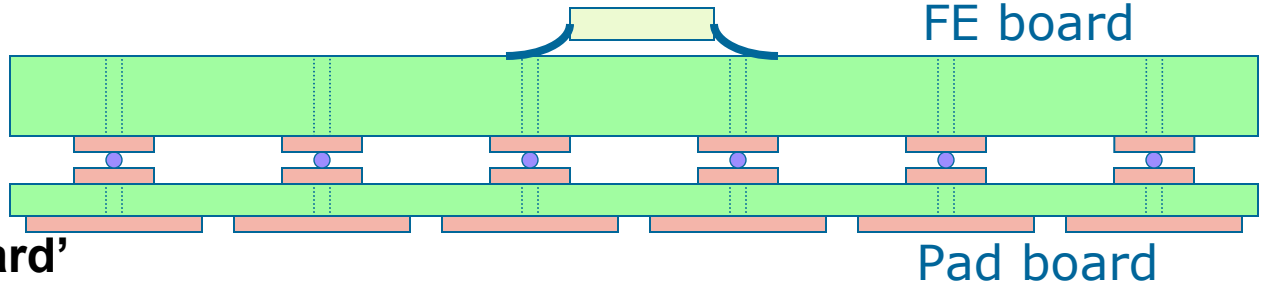


Ratio of slopes ~5.
Expected ~8.4pF/1.5pF = 5.6

- Found 2 minor issues
  - Chip addressing only works at 0 address
    - Slice test: solved by adjusting the design of the FE board
    - PS: correct problem for production run
  - Noise pickup on ch31, ch32
    - Due to a close-by test line
    - RPC: not a problem
    - GEM: leave the test line un-connected when packaging
- A few more tests yet to do
  - Low-gain noise floor
  - External charge injection
  - Self-trigger
  - Digital noise pickup

Pad board and FE board (1)

G Drake (ANL)



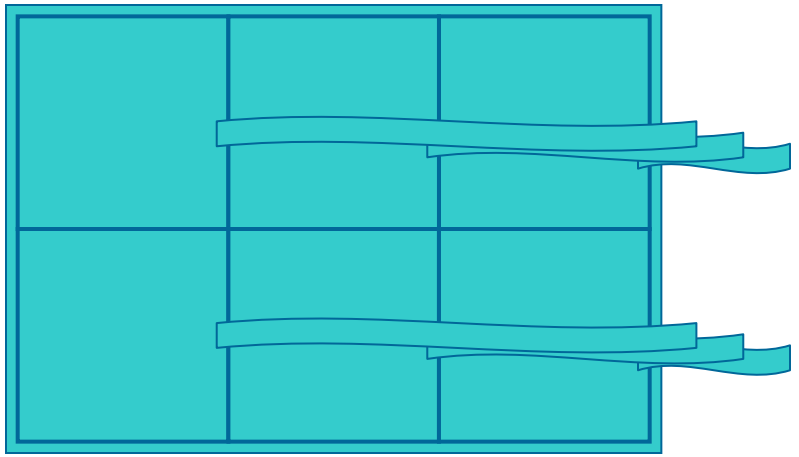
New Concept

Split old 'Front-end board'

'front-end board' highly complex and difficult
blind and buried vias + large board => (almost) impossible to manufacture
split into two boards to eliminate buried vias

Pad boards

four-layer board containing pads and transfer lines
can be sized as big as necessary
relatively cheap and simple
vias will be filled



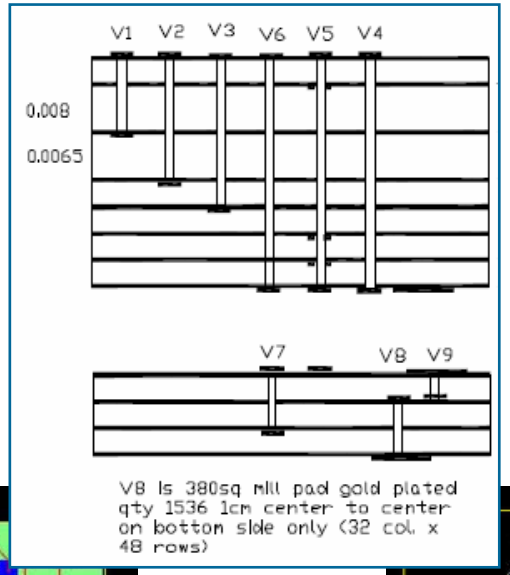
Front-end boards

eight-layer board
16 x 16 cm^2
contain transfer lines, houses DCAL chip
expensive and tough to design

Connections

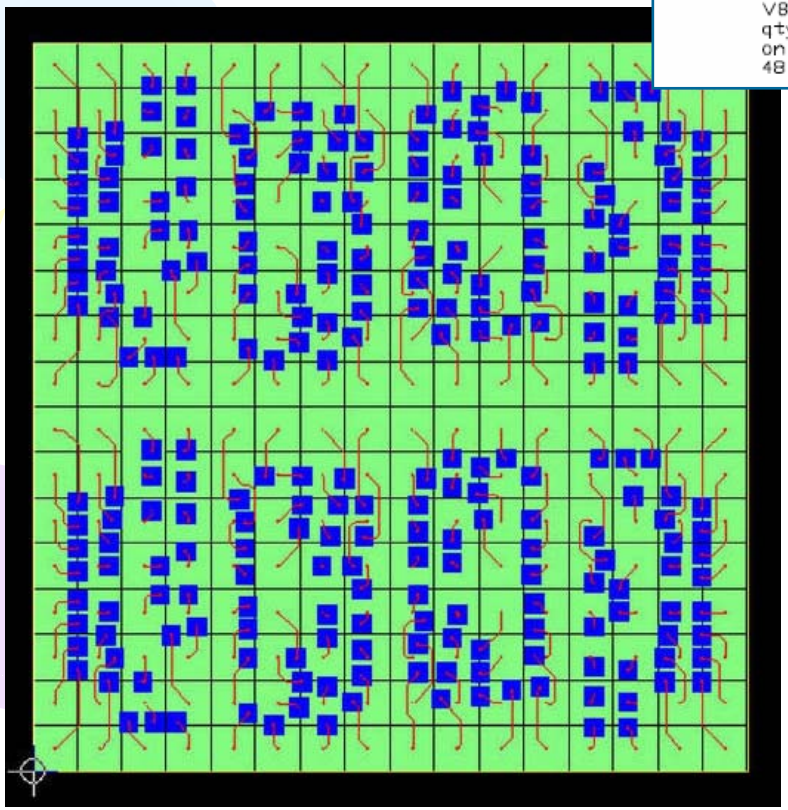
board to board with conductive glue on each pad (being tested)
cables for connection to data concentrators

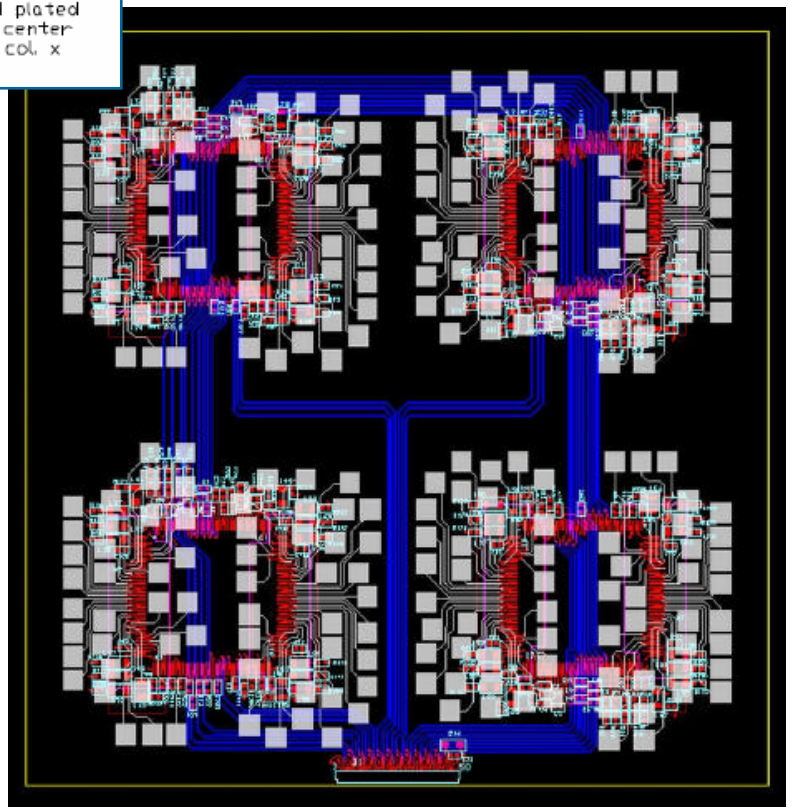
Pad board and FE board (2)



8 layer FE board
All (almost) layers

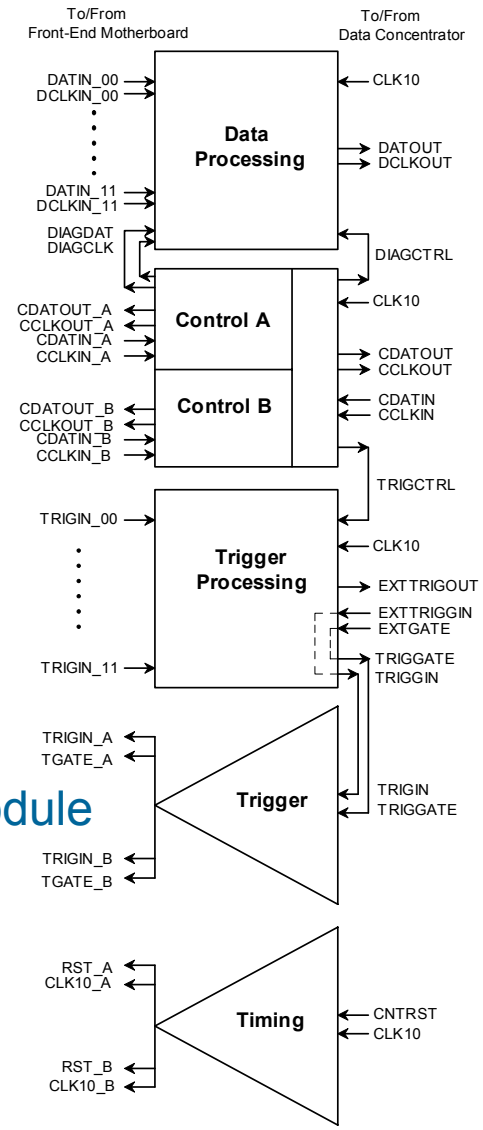
4 layer pad board





Data concentrator boards

Functionality defined
Protocol to data collector defined
Being designed at ANL



Timing and trigger module

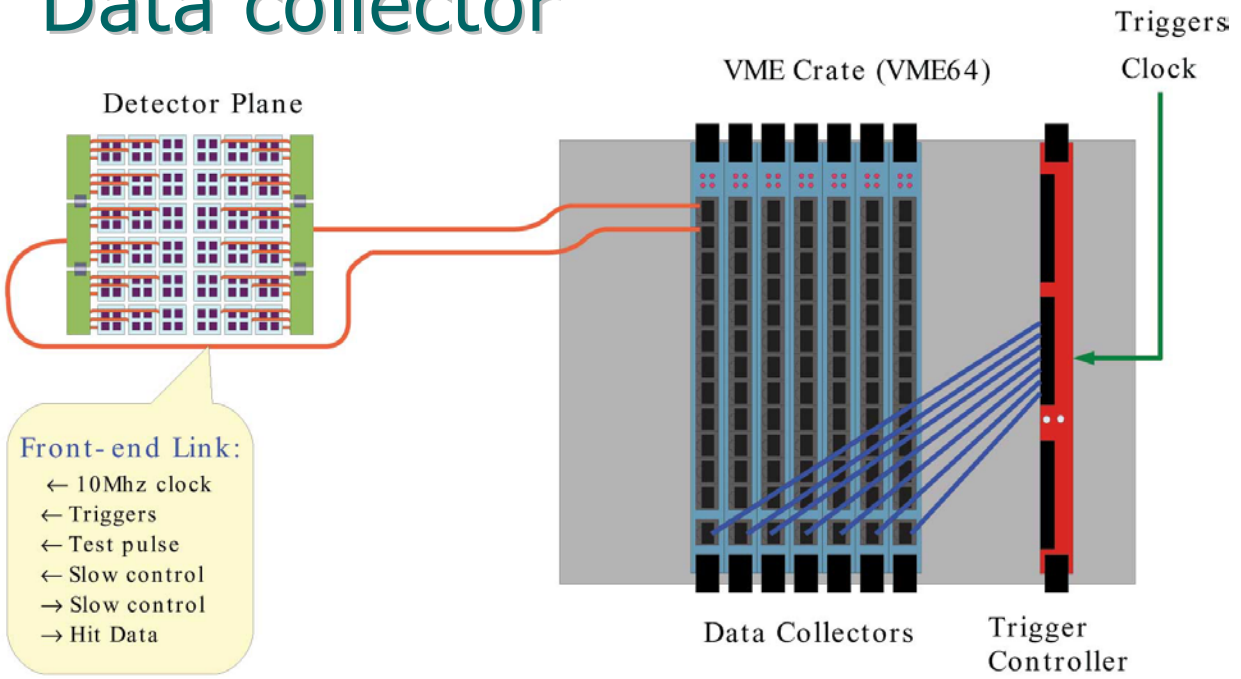
Functionality defined
Possibility of programming a commercially available module
To be designed by FNAL

Data collector

E Hazen (Boston)

New Design Effort

Actual design started
Goal: first prototype
by February 2007



Functionality

All data received as packets

Timestamp (24 bits) + Address (16 bits) + Hit pattern (64 bits)

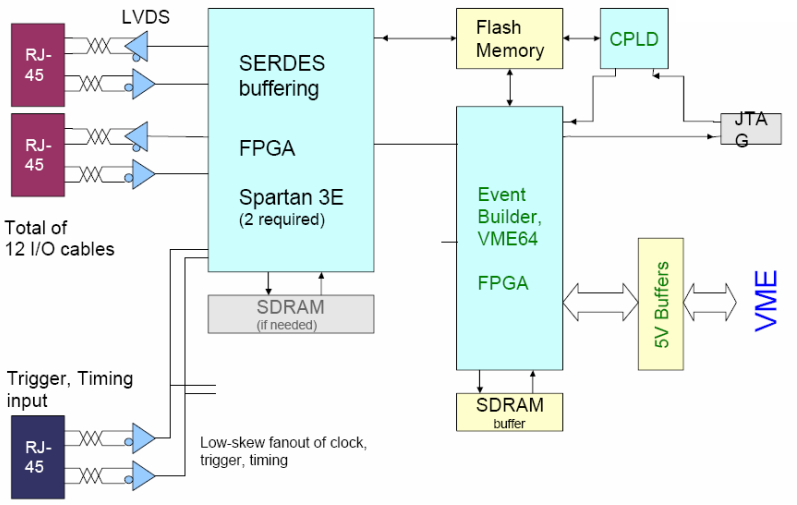
Packets grouped in buffers by matching timestamps

Makes buffers available for VME transfer

Monitors registers (scalars)

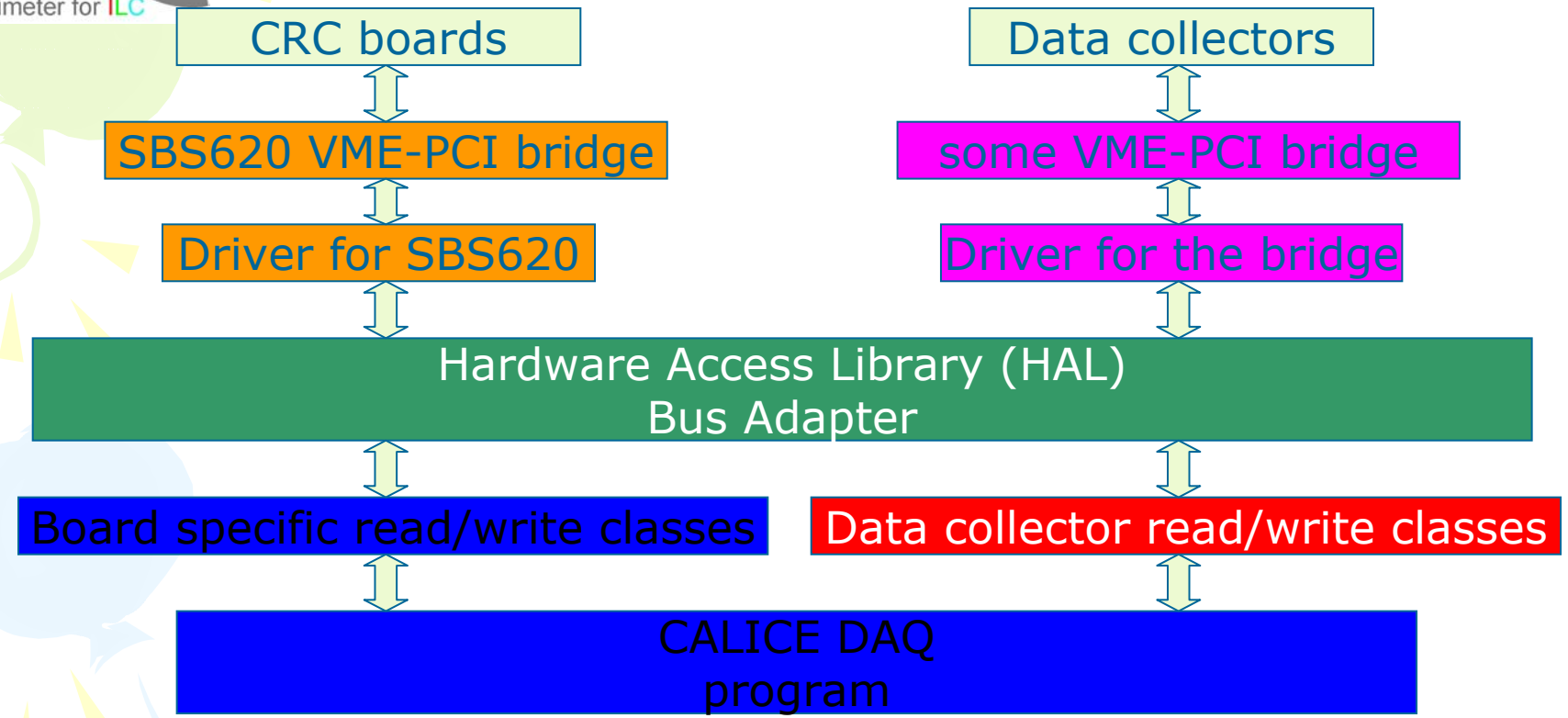
Slow control of front-end

Allows read/write to DCAL chips or
data concentrator boards



DAQ software

E May, A Kreps (ANL)



- Will be compatible with current CALICE test beam DAQ
- Use CALICE DAQ as much as possible to minimize the effort
  - Basically just need to supply some hardware specific I/O classes
- Currently focus on slice test, but will be used for 1m^3 PS as well

- Data format will follow existing CALICE convention

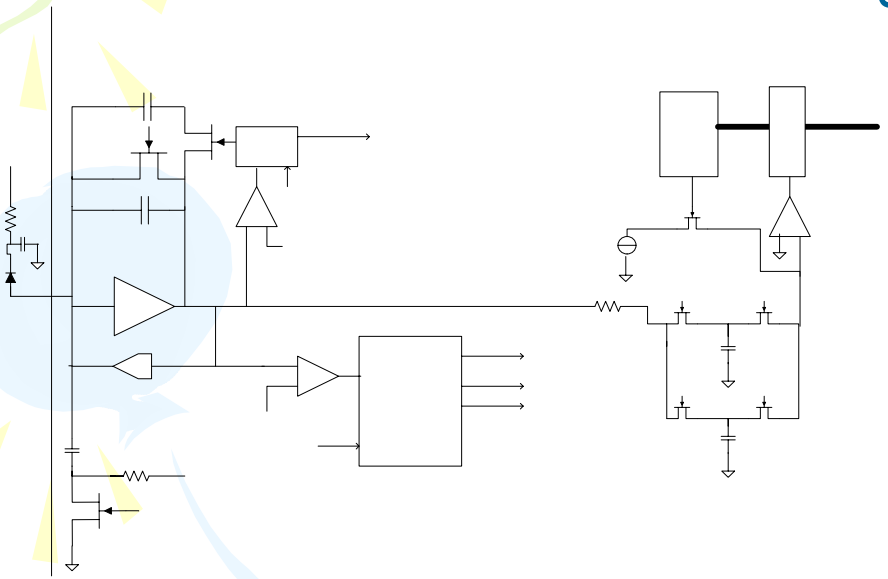
-- see Roman's talk on Friday for CALICE test beam software

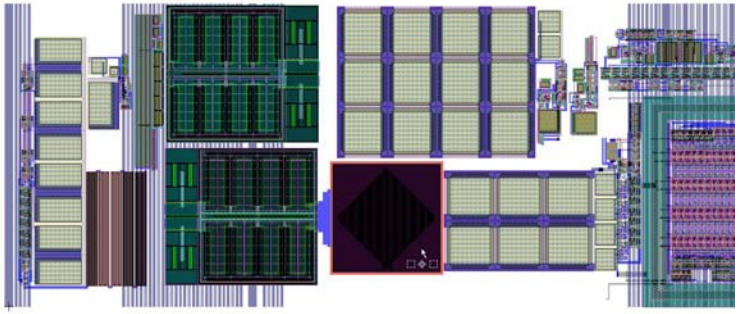
Other possibilities: KPix (SLAC/UTA) effort

Analog output. Two gain ranges

High: 0 – 500fC, Low: 0 – 10pC

Goal: 1024ch/chip + power pulsing





Current version

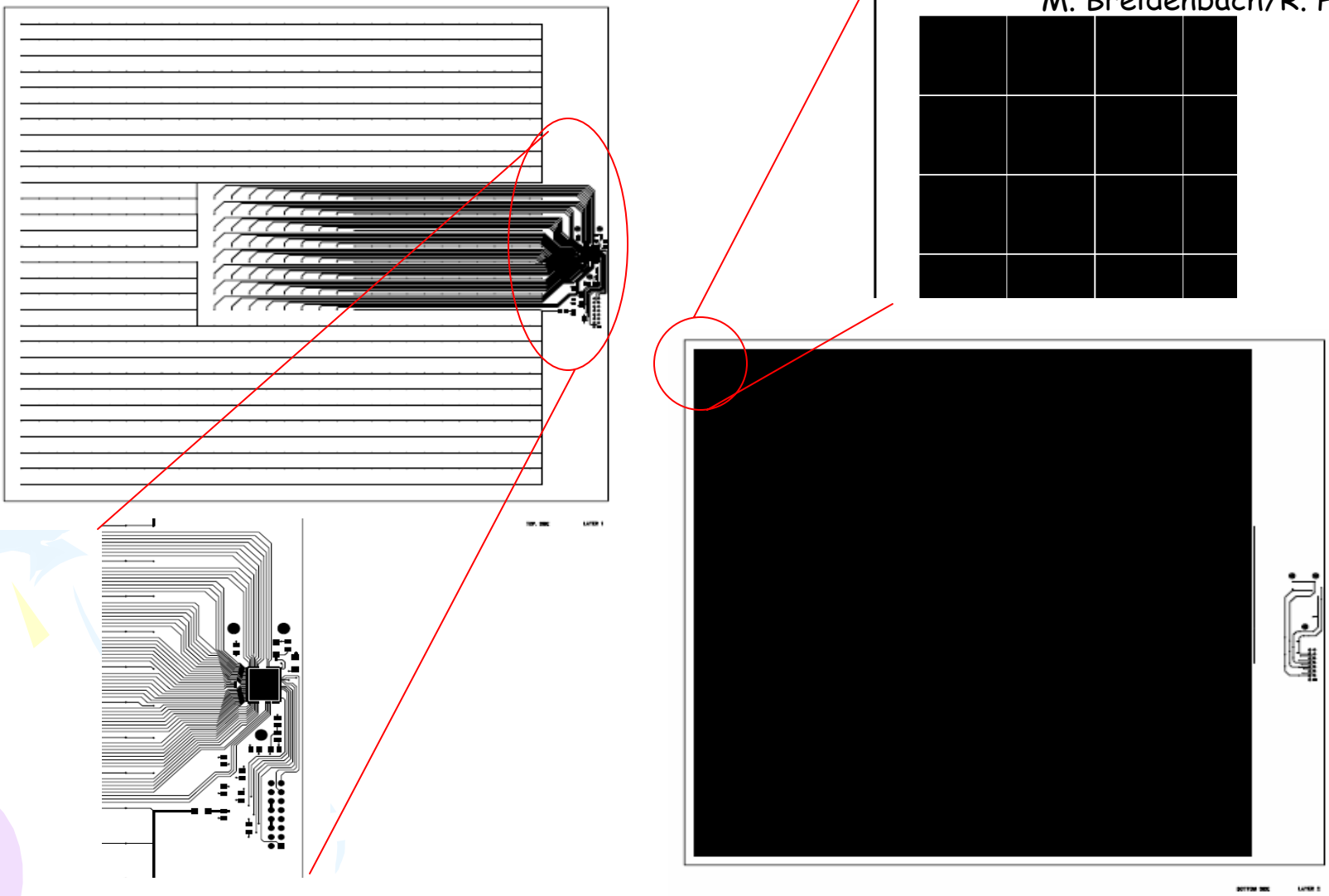
v3 – 64 channels – September 2006 (with GEM changes)

v4 – 64 channels, early 2007

Si-W Pixel Analog Section

KPix-GEM: pad + FE board details

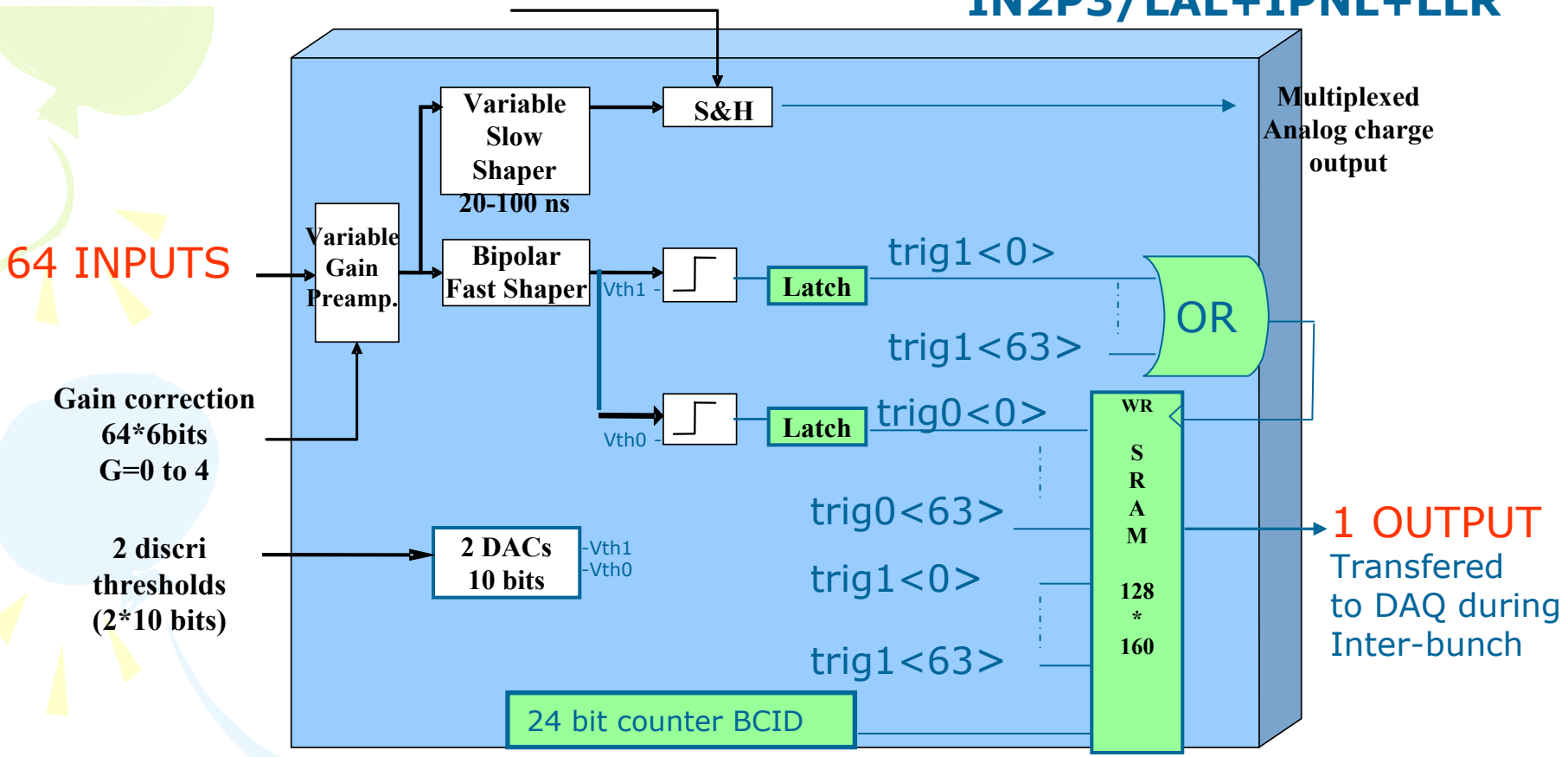
M. Breidenbach/R. Herbst



- KPix is a potential alternative for DHCAL readout
- Significant R&D is still needed to work out the system design
- FE board is going to be extremely challenging with 1024ch/chip

Other possibilities: MAROC/HaRDROC

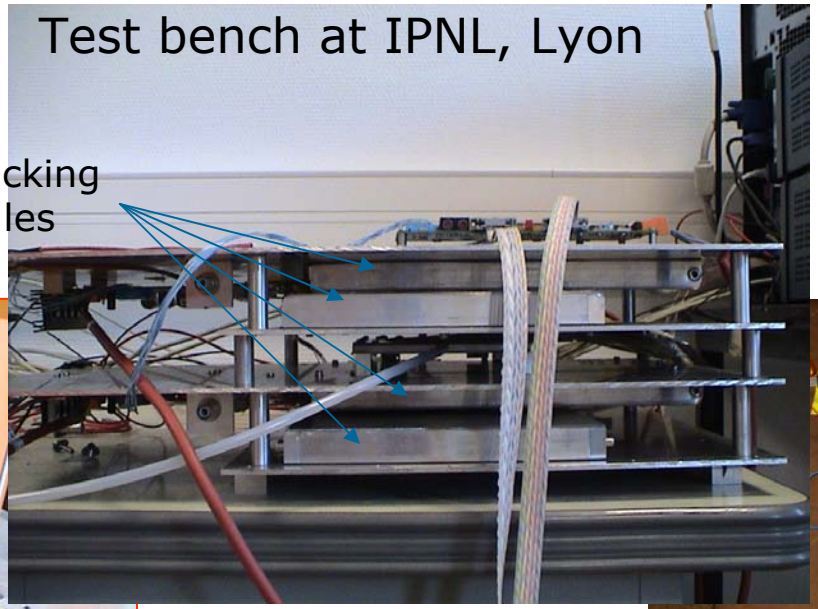
IN2P3/LAL+IPNL+LLR

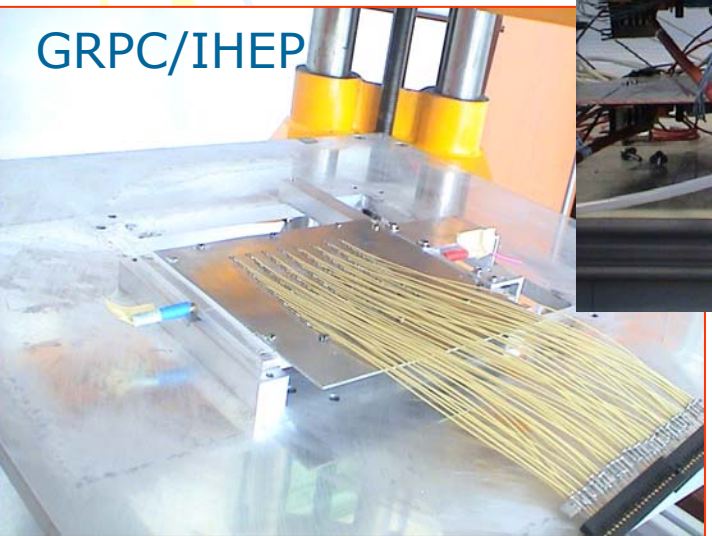


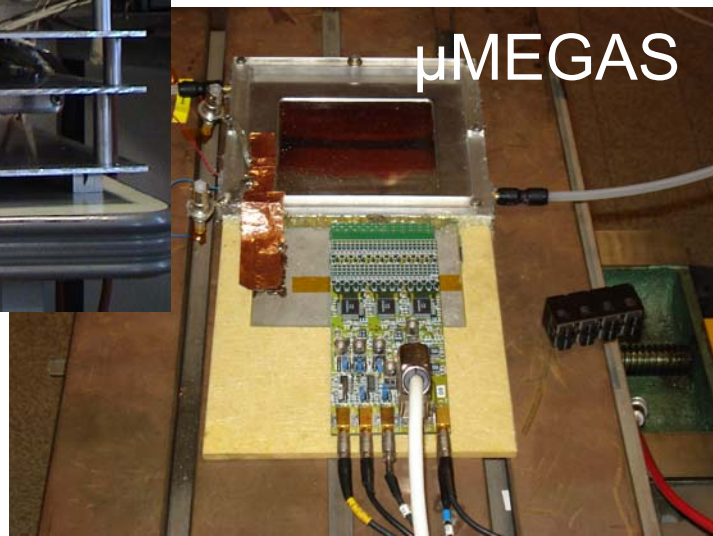
- Based on MAROC2 architecture (proven)
  - MAROC2: 64ch MAPMT chip for ATLAS lumi
    - MAPMT signal dynamic range ~ RPC, GEM signal
- HaRDROC ~ MAROC + power pulsing + digital memory
  - Submitted September 2006
  - Expected delivery Dec, 2006

HarDROC development

- PCB hosting 4 HarDROC chips will be developed and tested (IPNL + LAL + LLR + LAPP)
  - PCB expected in March 2007
  - To be tested on 10x40 cm^2 GRPC (collab. with IHEP)
  - To be tested on 10x40 cm^2 mMEGAS (collab. with Saclay)
  - Test with cosmic ray bench and then with beam
- Future: extend to 1x1m2 for GRPC and mMEGAS
  - In collaboration with ceimat (Madrid)





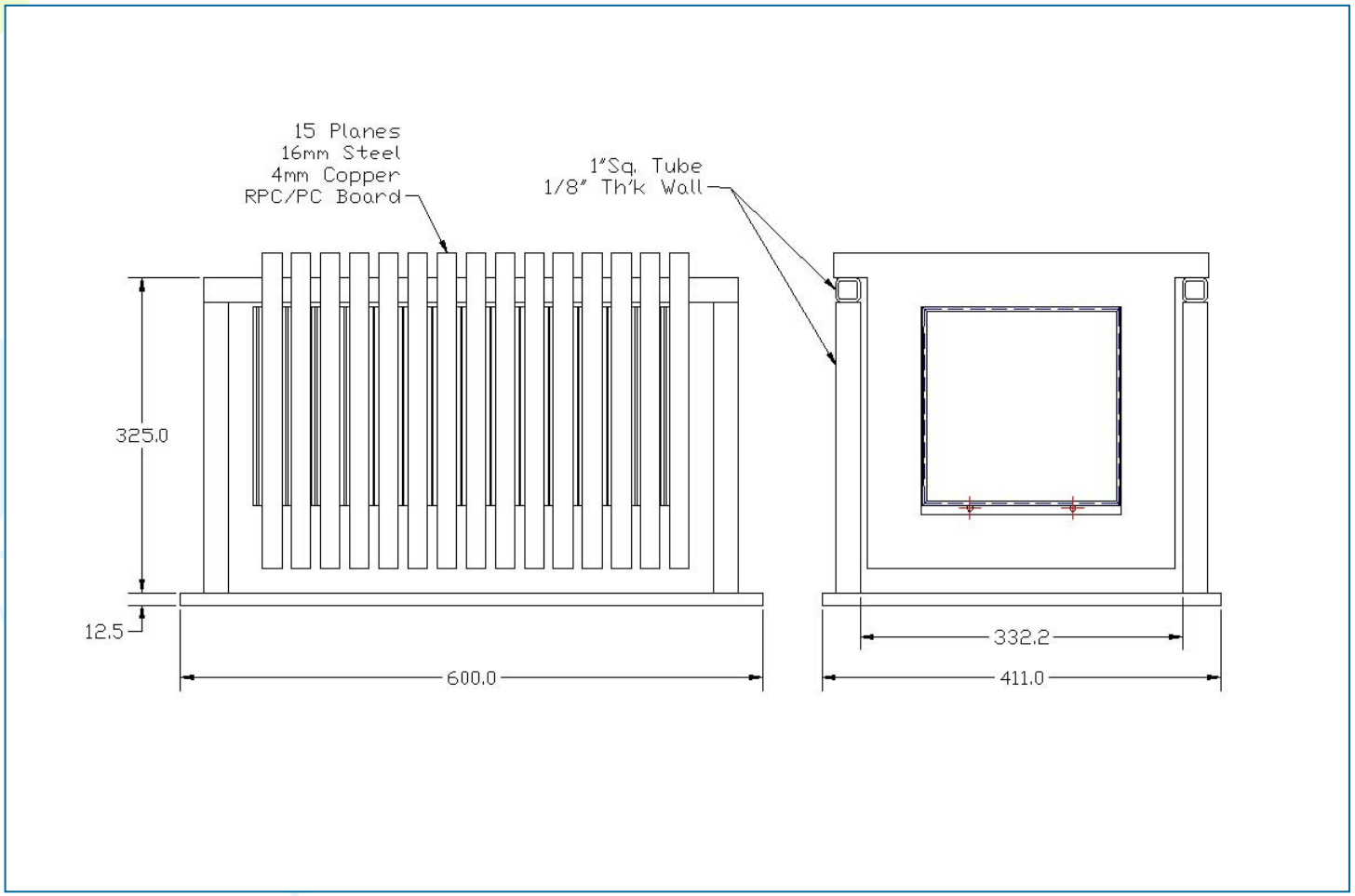


Readout summary

	Item	DCAL	KPix	HaRDROC
FE ASIC	**Current version**	v2	v3	v1
	Current ch# /final ch#	64/64	64/1024	64/64
	Test	Almost done	Ongoing	Started?
	Additional submission	No	Yes	?
	Overall status	Almost done	Ongoing	Ongoing
Readout system for PS	**Conceptual design**	Done	Yes	?
	FE board	Design finished	No	Started?
	Concentrator	Design started	Design started	No
	Data Collector	Design ongoing	No	No
	Trigger Timing module	Specified	No	No
	DAQ software	Started	Started	No
	Overall system	Well advanced	Started	No

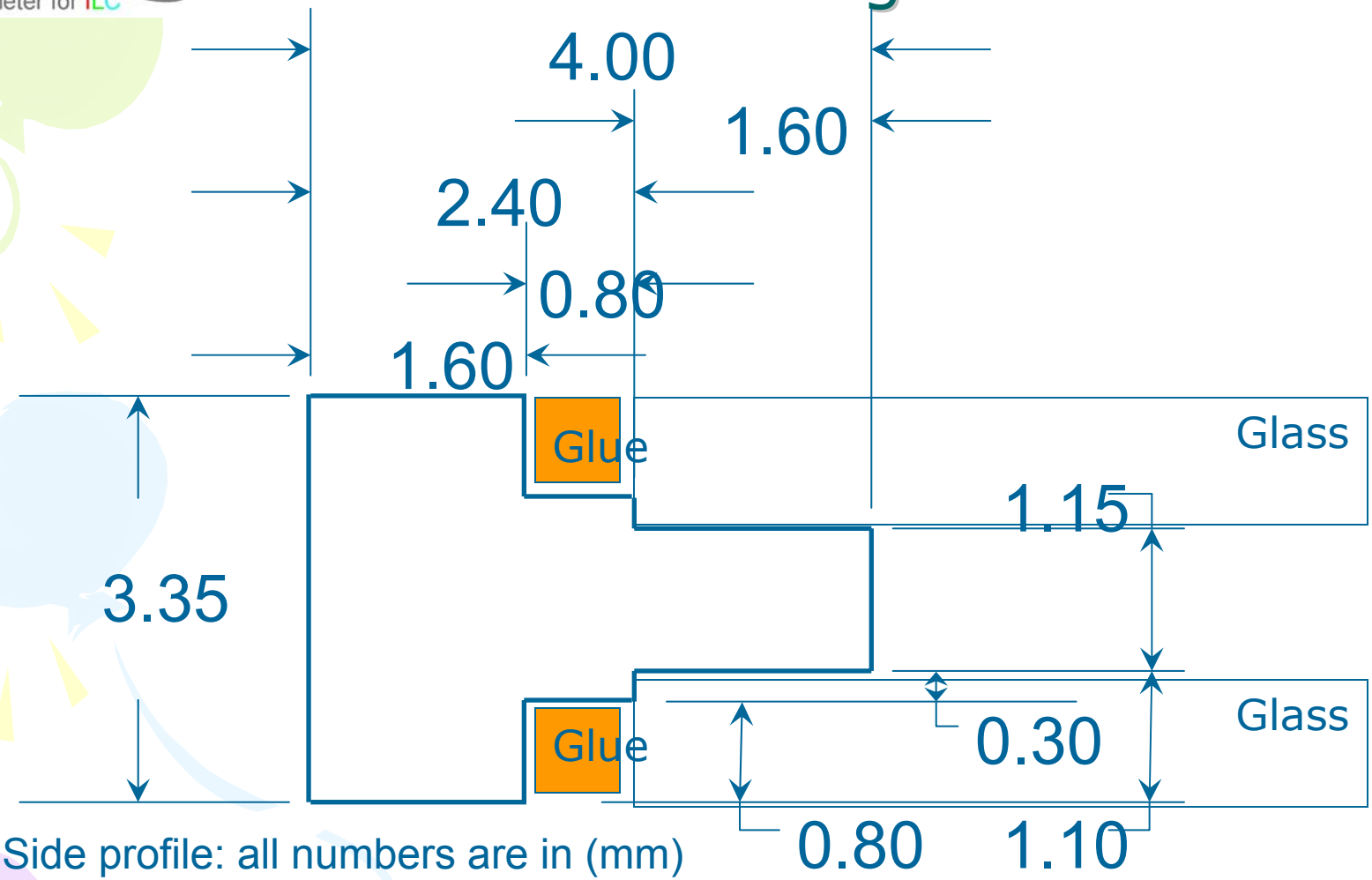
- If funding permits, given current progress
  - The 1st PS stack would (naturally) be: RPC + DCAL based readout
  - The 2nd PS stack would be: GEM + ? Readout
- DCAL readout will be validated through the slice test (Apr.07, MTBF)

Slice test: mechanical design



Design accommodates 20 x 20 cm^2 RPCs as well as 30 x 30 cm^2 GEMs
Stack is assembled, minor adjustment still needed

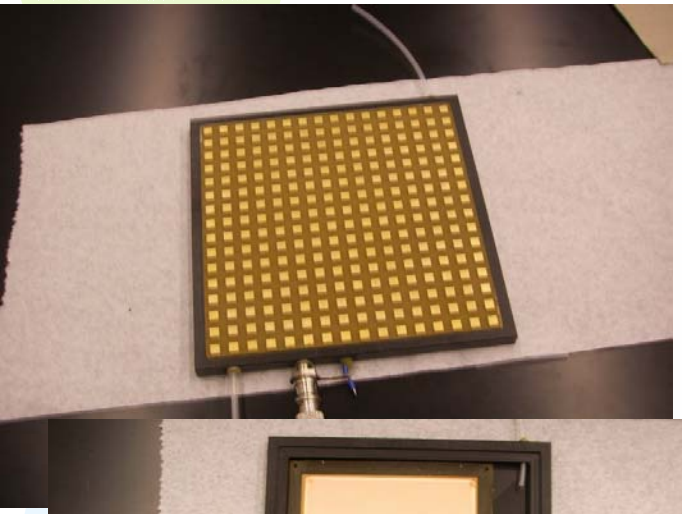
RPC design

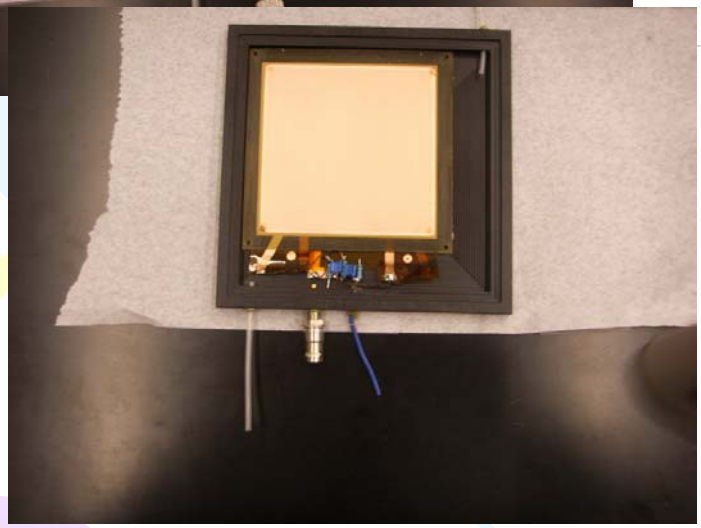


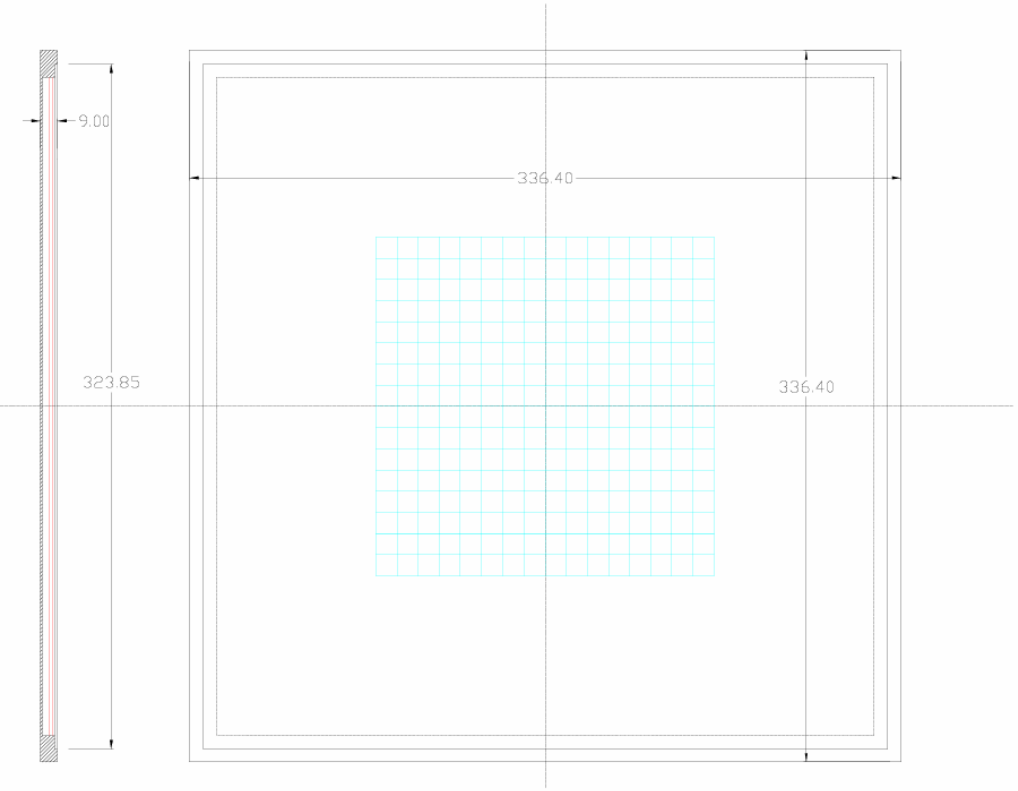
Side profile: all numbers are in (mm)

- New design provide a flush chamber surface
- Easier to assemble and assure gas tightness
- 1st chamber built and tested successfully

GEM chamber design

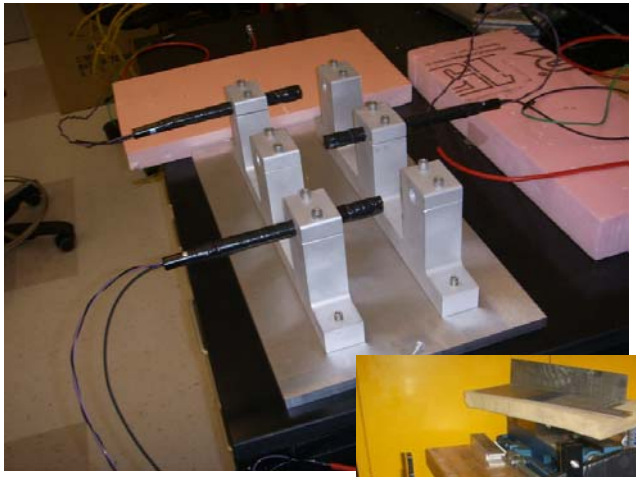






- GEM chamber design done, dimensions fixed
- New test chamber built at UTA
- 2 GEM chambers for slice test are being built

Slice test: Trigger counters, Gas, HV



Beam telescope

J Li, A White, J Yu (UTA)

6 counters (3 x (1 x 1 cm^2) + 2 x (19 x 19 cm^2)
Mounted on rigid structure
all done

HV modules

E Norbeck (Iowa)

Need separate supplies for each chamber
Modules (from FNAL pool) being tested

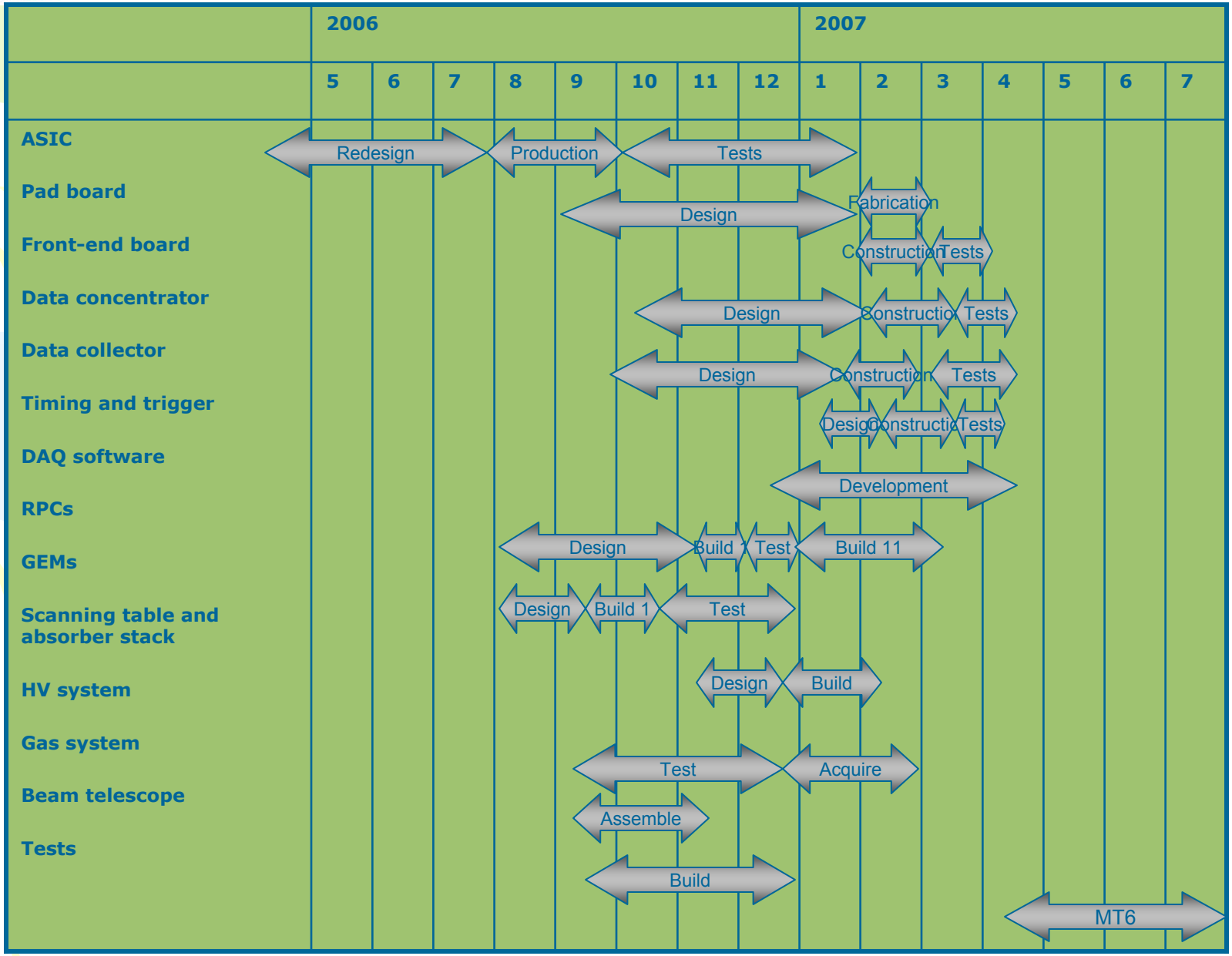
With additional RC-filter perform similarly to our Bertan unit in analog tests (RABBIT system)
Still need to perform tests with digital readout

Gas system

E Norbeck, D Northhacker (Iowa)

Built manifold for 10 chambers
Need approval for gas tanks (safety issue)

Slice test schedule

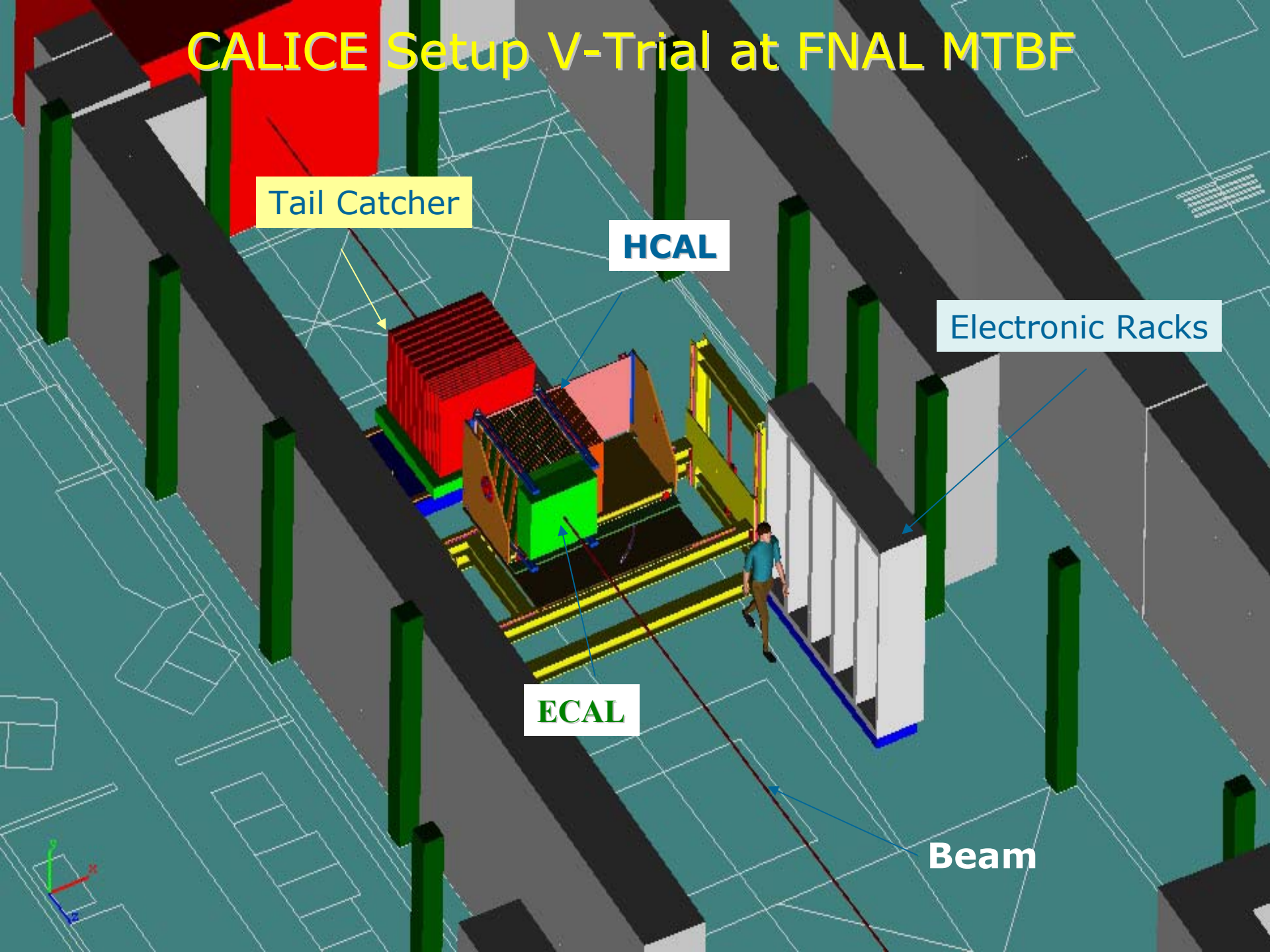


Summary

- DHCal R&D has been carried out for different active mediums
  - RPC efforts: done on R&D
  - GEM: in progress, expect to finish in ~ 1 year
  - MicroMegas: started
- Slice test is the next major test beam activity
  - Mini-calorimeter stack: 8 RPC's + 2 GEM's
  - DCAL readout system: as close as possible to $1m^3$
  - A lot of progress, expect move to test beam in April 2007
  - Validate readout system + some shower data
- Goal: $1m^3$ prototype section test beam
  - 1^{st} stack: RPC + DCAL readout
  - 2^{nd} stack: GEM + ? Readout
  - DCAL readout system: well advanced
  - KPix, HarDROC: alternative readout, chip under development
- Funding: biggest limiting factor…

Backup slides

CALICE Setup V-Trial at FNAL MTBF



Costs and Funding

A) Slice test is funded by LCDRD06, LDRD06 and ANL-HEP, and Fermilab funds

B) Prototype section not yet funded, but…

Stack	Item	Cost	Contingency	Total
RPC stack	**M&S**	607,200	194,600	801,800
	Labor	243,075	99,625	342,700
	Total	**850,275**	**294,225**	**1,144,500**
GEM stack*	**M&S**	400,000	165,000	565,000
* Reusing most of the RPC electronics	**Labor**	280,460	40,700	321,160
	Total	**680,460**	**205,700**	**886,160**
Both stacks	**M&S**	1007,200	359,600	1366,800
	Labor	523,535	140,325	663,860
	Total	**1,530,735**	**499,925**	**2,030,660**

Proposal for supplemental funds for $500k/year over two years submitted to DoE
With continuing resolution, it is not very promising … wait one more year?