WIB firmware status

A. Madorsky for WIB firmware team

General news

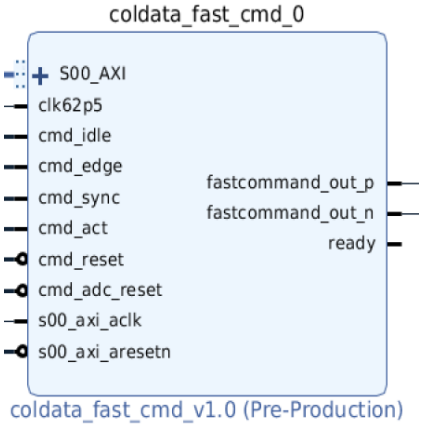
- WIB + COLDATA + COLDADC firmware repository created
  - On Github
- Firmware team has access
  - Including CRYO team
- Please let me know if you need access

- Meeting with CRYO firmware team is coming up
- Poll just finished
- Best time:
  - Tomorrow, June 30th, 11 am Eastern time
- Will send a message to firmware team soon

Simulation status

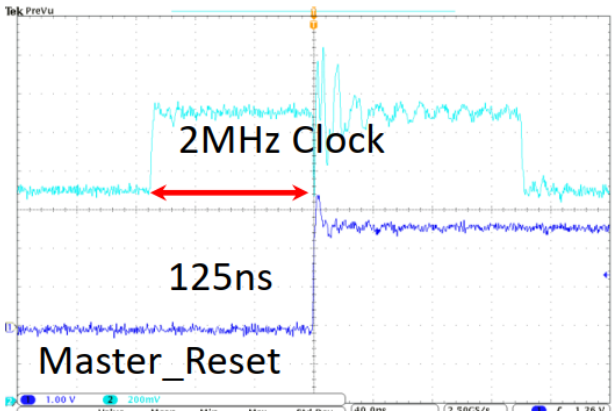
FAST command module

- Implemented FAST command module as IP
- Commands can be triggered via:
  - software
  - by firmware signal (pulsing a pin)
- ColdADC rev 1 requires special synchronization sequence:
  - Step 1: 2MHz clock edge alignment
  - Step 2: Master reset with precise fixed timing relative to step 1
- Implemented this sequence as a single command in FAST command IP

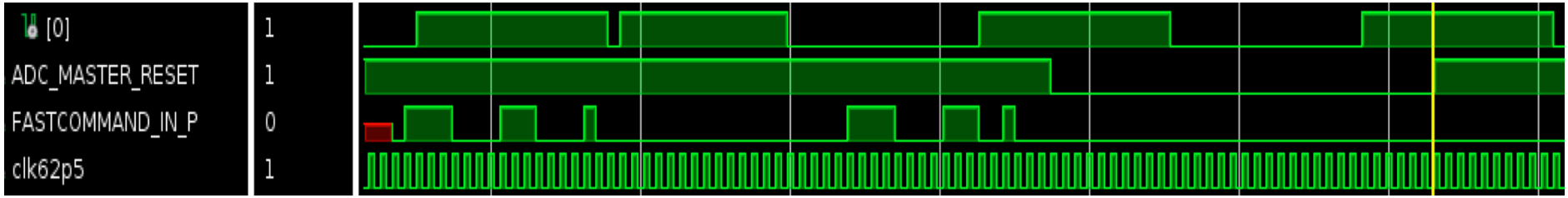


ColdADC sync procedure

From slide by
Shanshan Gao
(received from David)



WIB simulation



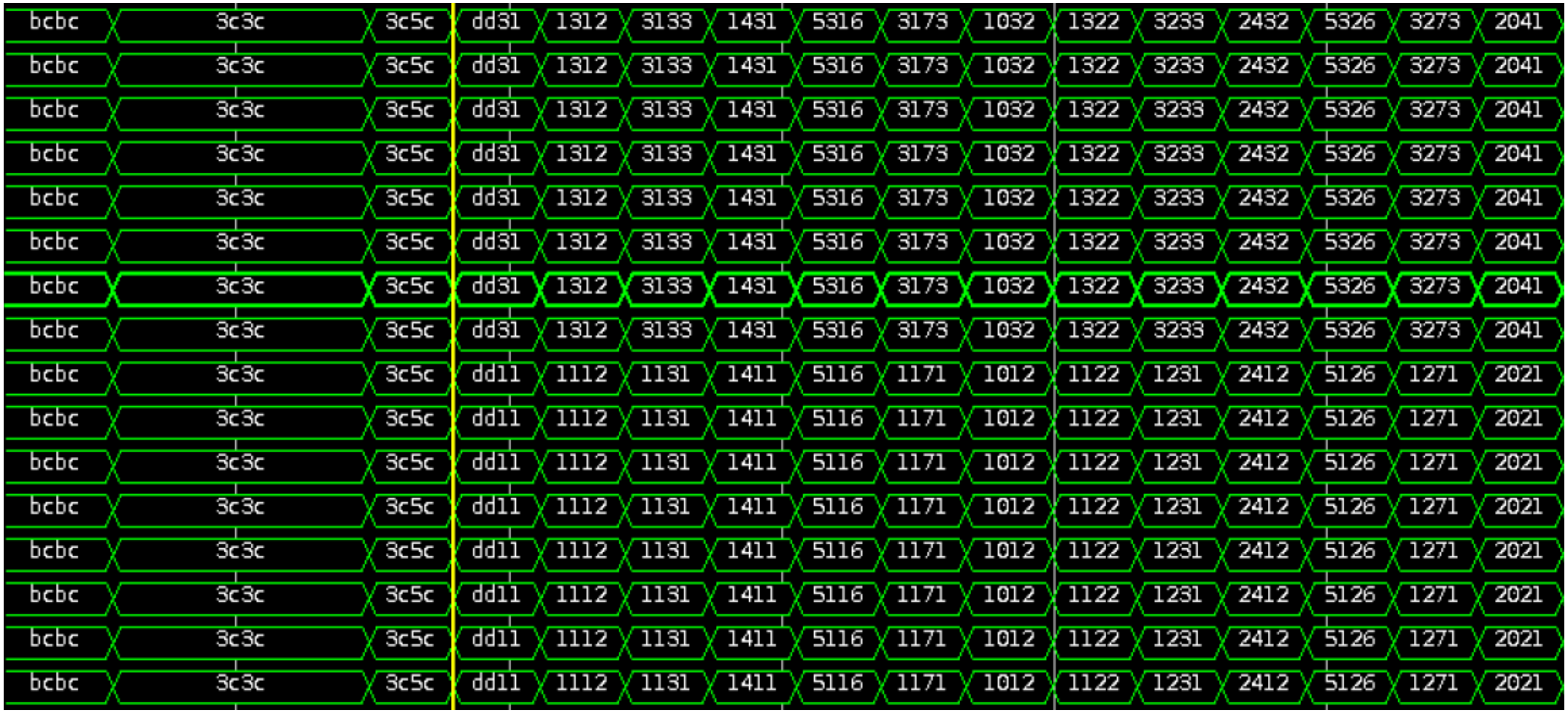
Simulation status

ColdADC outputs

- Reprogrammed to send test patterns
- Supposed to be a combination of power voltages
- Instead, see this:
  - Output 0: “ABCD”
  - Output 1: “1234”
- Seems like this was done for simulation only?
- Can see these patterns propagating all the way to WIB RX outputs
- Next, supplied my simple test patterns to digital ADC inputs in ColdADC
- Pattern = {

```
adc_num,     // 4 bits, 1..4
output_num,  // 4 bits. 1..2
frame_num,   // 4 bits  0..7
4'b0};       // will be removed in Frame12
```

WIB RX outputs, Frame-12 mode



bcbc	3c3c	3c5c	dd31	1312	3133	1431	5316	3173	1032	1322	3233	2432	5326	3273	2041
bcbc	3c3c	3c5c	dd31	1312	3133	1431	5316	3173	1032	1322	3233	2432	5326	3273	2041
bcbc	3c3c	3c5c	dd31	1312	3133	1431	5316	3173	1032	1322	3233	2432	5326	3273	2041
bcbc	3c3c	3c5c	dd31	1312	3133	1431	5316	3173	1032	1322	3233	2432	5326	3273	2041
bcbc	3c3c	3c5c	dd31	1312	3133	1431	5316	3173	1032	1322	3233	2432	5326	3273	2041
bcbc	3c3c	3c5c	dd31	1312	3133	1431	5316	3173	1032	1322	3233	2432	5326	3273	2041
bcbc	3c3c	3c5c	dd31	1312	3133	1431	5316	3173	1032	1322	3233	2432	5326	3273	2041
bcbc	3c3c	3c5c	dd31	1312	3133	1431	5316	3173	1032	1322	3233	2432	5326	3273	2041
bcbc	3c3c	3c5c	dd11	1112	1131	1411	5116	1171	1012	1122	1231	2412	5126	1271	2021
bcbc	3c3c	3c5c	dd11	1112	1131	1411	5116	1171	1012	1122	1231	2412	5126	1271	2021
bcbc	3c3c	3c5c	dd11	1112	1131	1411	5116	1171	1012	1122	1231	2412	5126	1271	2021
bcbc	3c3c	3c5c	dd11	1112	1131	1411	5116	1171	1012	1122	1231	2412	5126	1271	2021
bcbc	3c3c	3c5c	dd11	1112	1131	1411	5116	1171	1012	1122	1231	2412	5126	1271	2021
bcbc	3c3c	3c5c	dd11	1112	1131	1411	5116	1171	1012	1122	1231	2412	5126	1271	2021
bcbc	3c3c	3c5c	dd11	1112	1131	1411	5116	1171	1012	1122	1231	2412	5126	1271	2021
bcbc	3c3c	3c5c	dd11	1112	1131	1411	5116	1171	1012	1122	1231	2412	5126	1271	2021

Pattern decoding (bottom trace):

111-112-113-114-115-116-117-110-121-122…etc

Each ADC readout takes 3 nibbles

Patterns received correctly, but:

Note incorrect frame sequence (red)

Next steps

- **Design frame decoders:**
  - **FRAME-12**
  - **FRAME-14**
  - **FRAME-15**