

Dataprep: simulation and calibration

ProtoDUNE-SP sim/RECO

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BNL

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Introduction

Two topics today:

- Dataprep in simulation
 - New module
 - Tail removal
- Updates on calibration
 - New data
 - Charge sharing

Dataprep in simulation

The current dataprep for “real” data:

```
"digitReader",           # Read RawDigit
"pdsp_sticky_codes_ped", # Flag sticky codes
"pd_adcPedestalFit",     # Find pedestal
"adcSampleCalibration", # Subtract pedestal and apply charge calibration
"pdsp_adcMitigate",      # Mitigate sticky codes
"pdsp_timingMitigate",   # Mitigate FEMB302 timing
"adcCorrectUndershootKe", # correct undershoot
"pdsp_noiseRemovalKe"    # Remove high frequency noise and coherent noise
"adcKeepAllSignalFinder", # Keep all signal (no ROIs)
"adcScaleKeToAdc",       # Scale samples to nominal ADC counts
"pdsp_RemoveBadChannels" # Set bad channels to 0 ADC
```

We would like to also run dataprep in simulation

- Study the effect of these tools on data with truth info
- Mitigate and correct where effects are present in simulation

Dataprep configuration has been added to dunetpc

- Includes tail removal but not (yet) calib, timing/SC mitigation, CNR
- Need to modify default sim reco to use the configuration

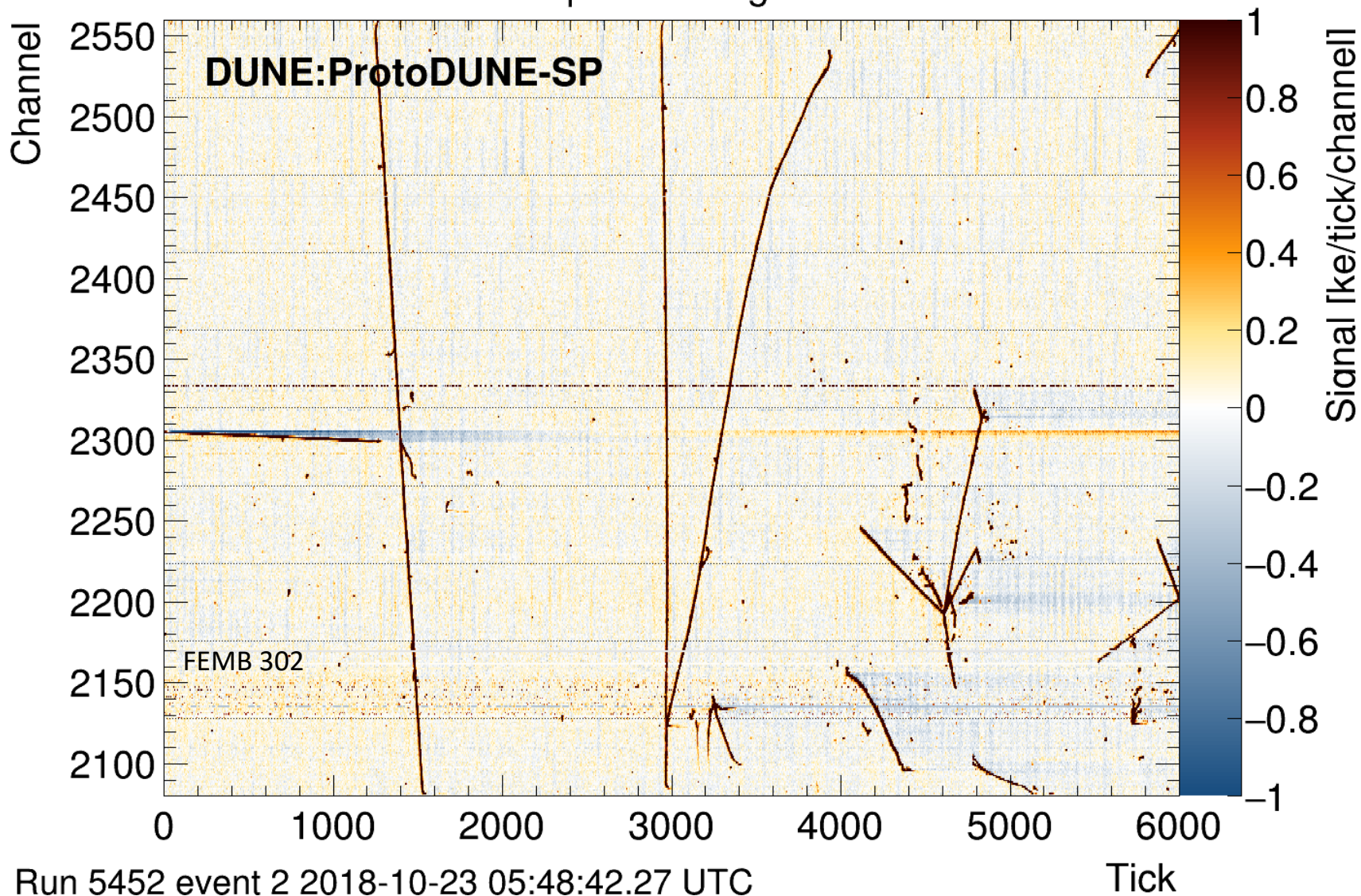
Tail removal in simulation

Running dataprep makes it easy to study performance

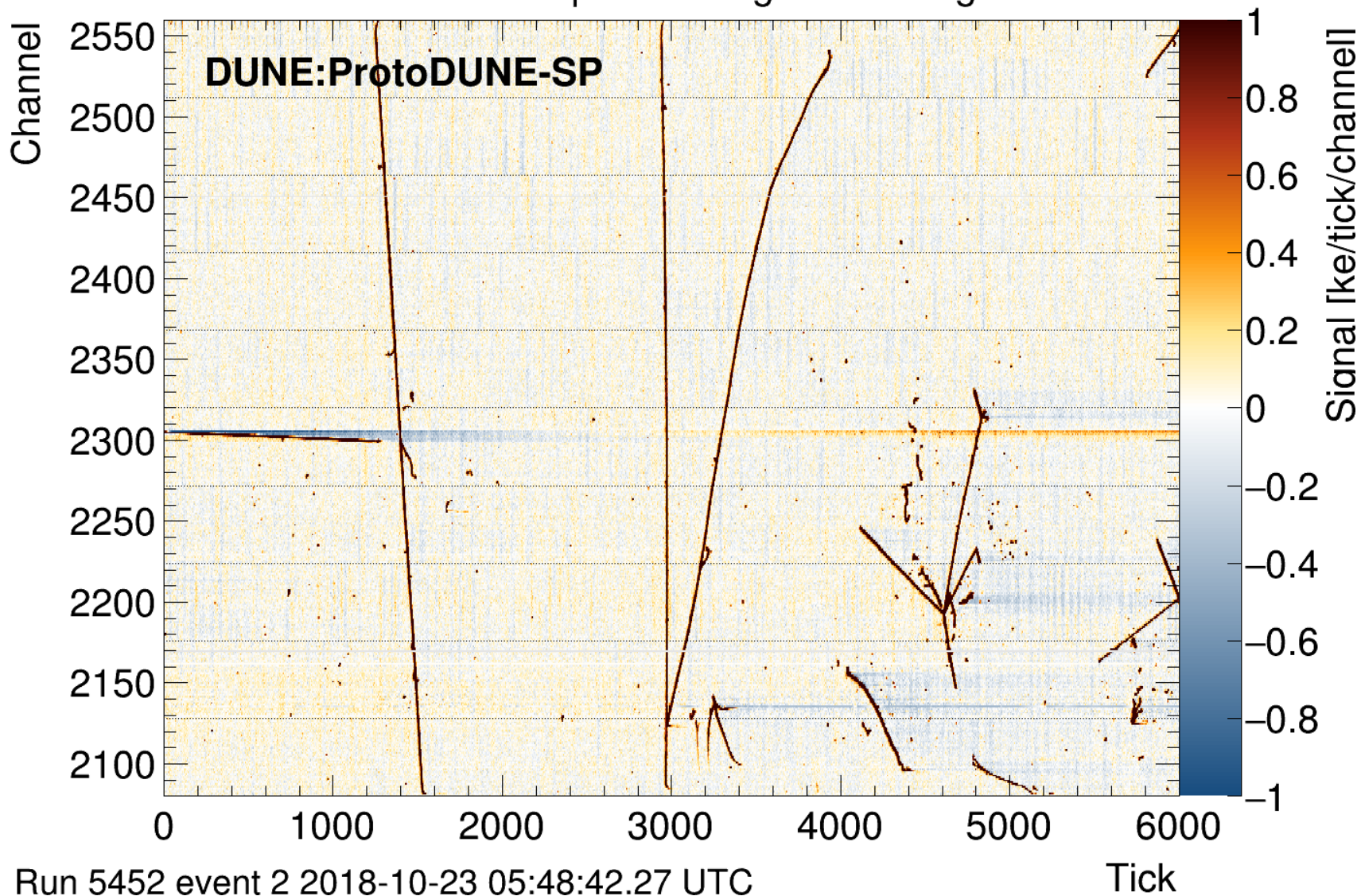
- Insert event display between different stages of reco
- E.g. see following displays from performance note

Data displays from performance note

APA 3 collection plane charge after calibration



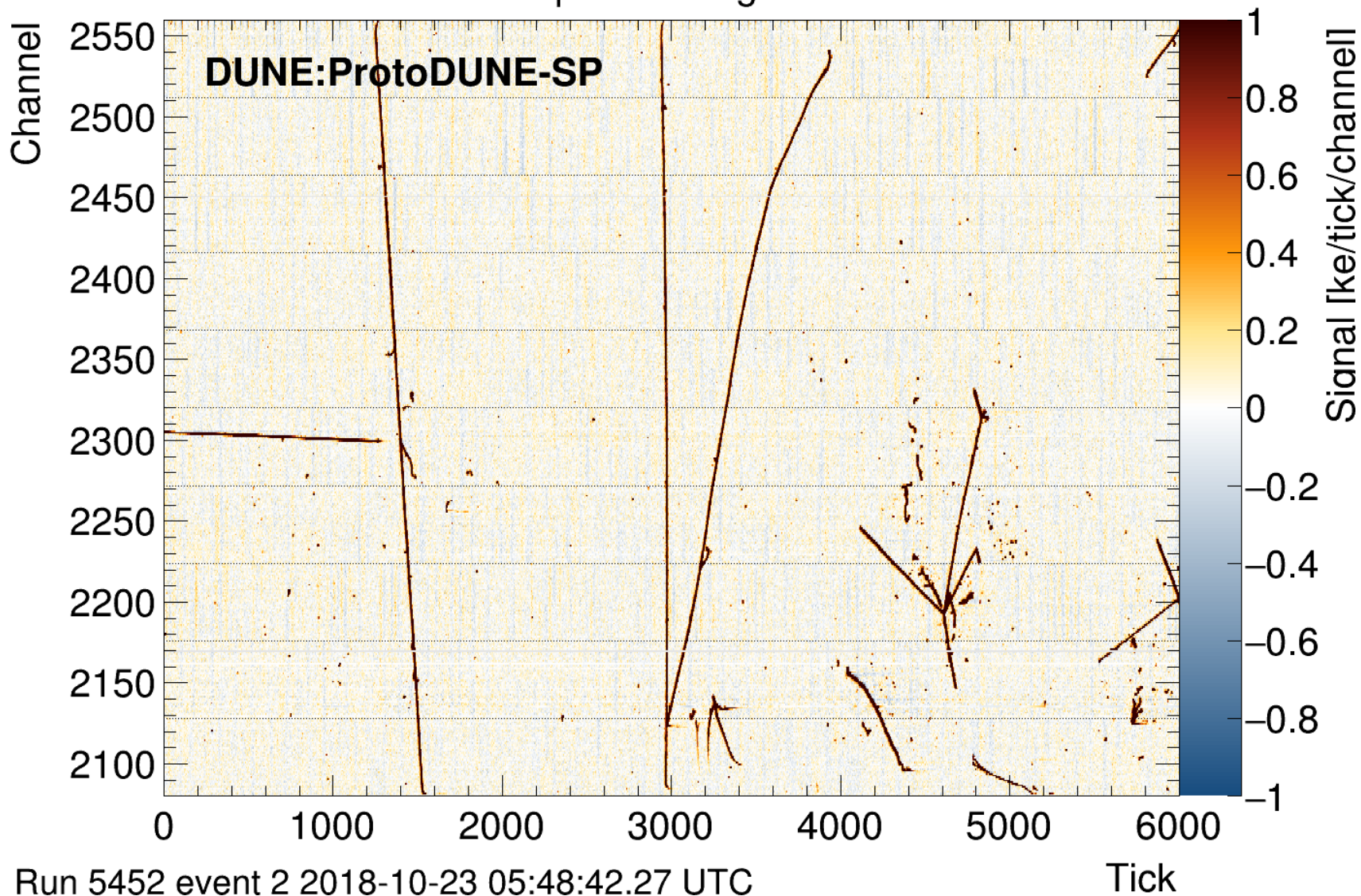
APA 3 collection plane charge after mitigation



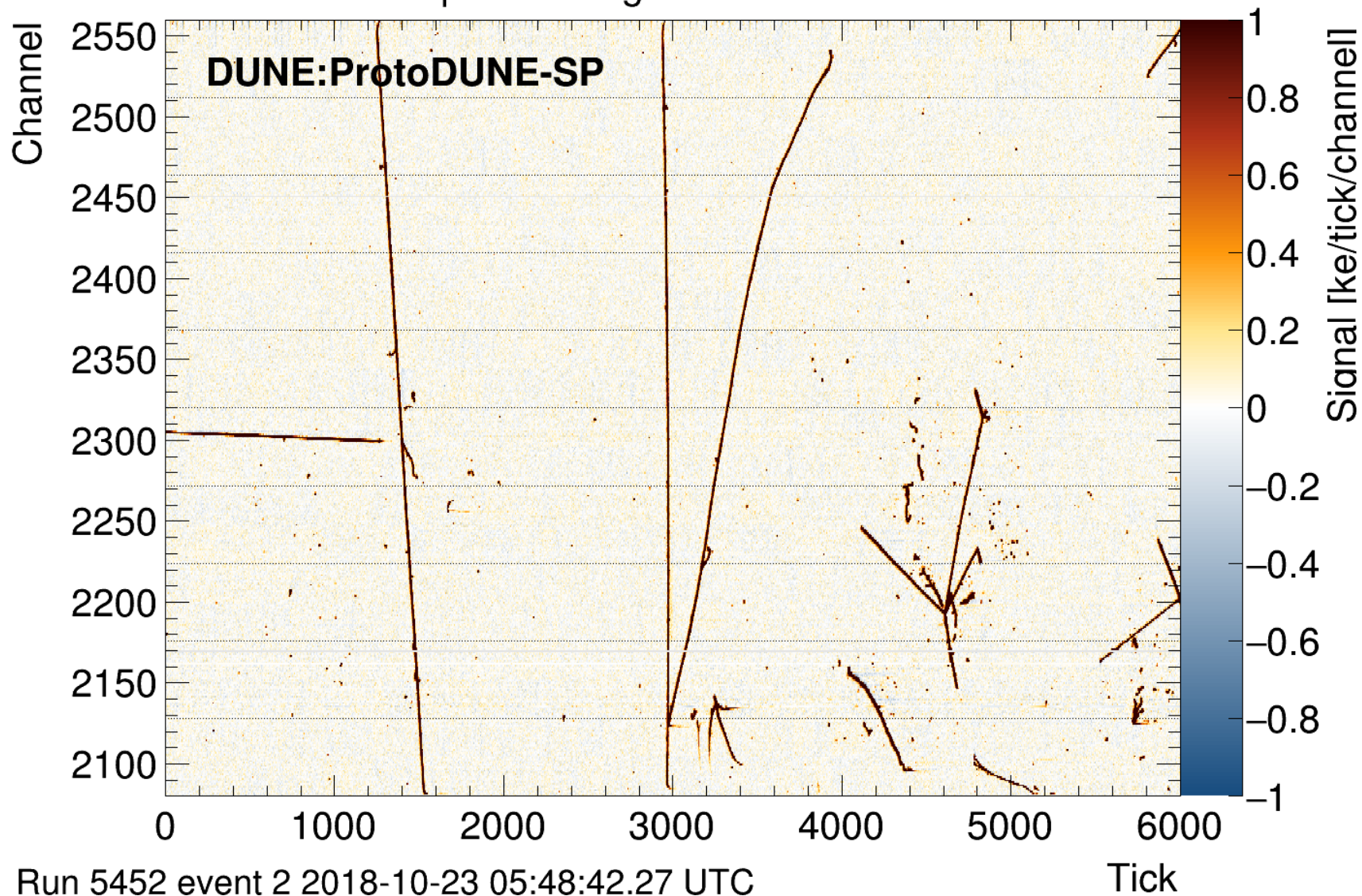
Run 5452 event 2 2018-10-23 05:48:42.27 UTC

Tick

APA 3 collection plane charge after tail removal



APA 3 collection plane charge after correlated noise removal



Tail removal in simulation (2)

Running dataprep makes it easy to study performance

- Insert event display between different stages of reco
- E.g. see preceding displays from performance note

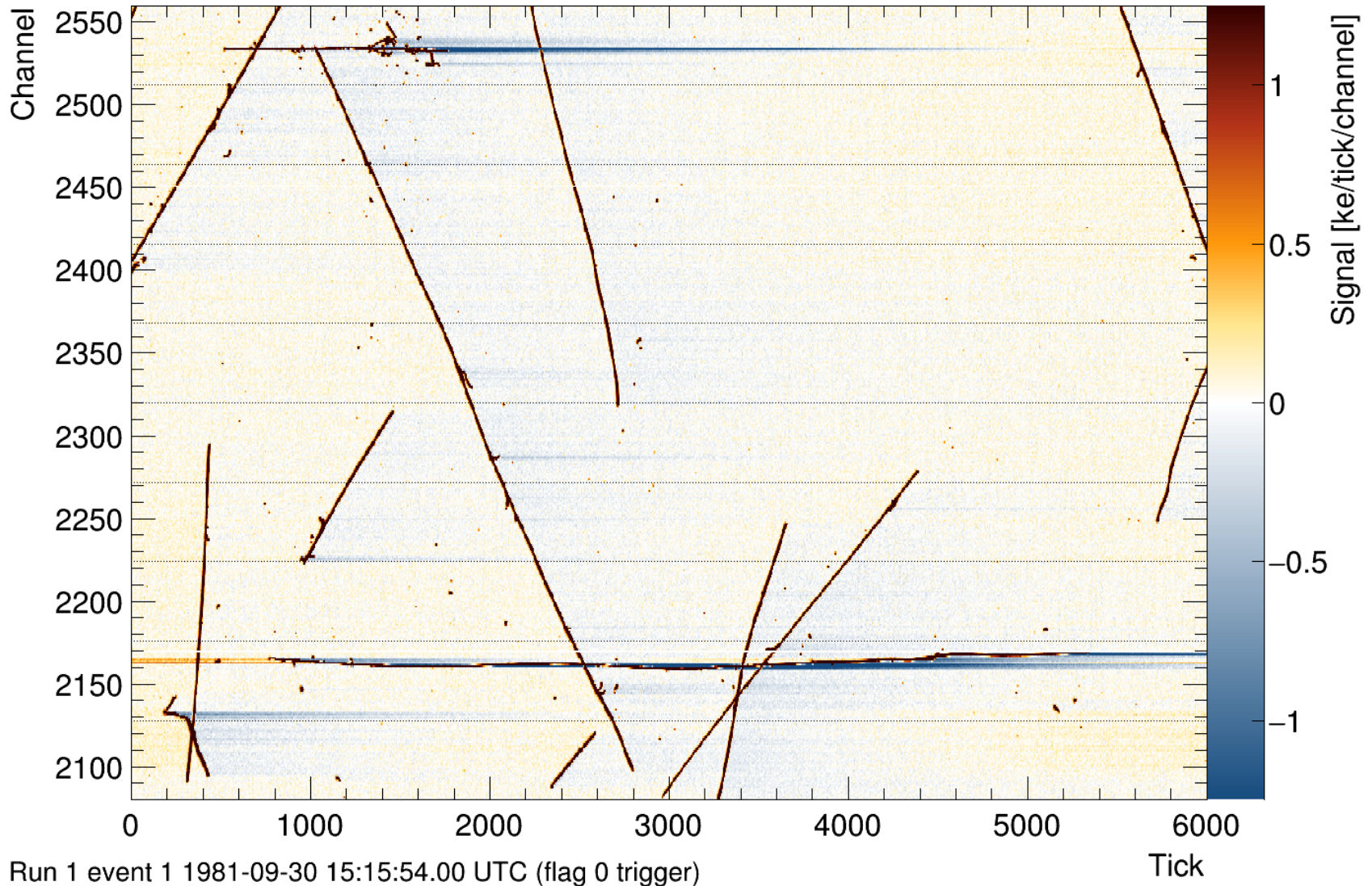
I have started to do the same for simulated data

- Look before and after tail removal
- See following slides
- Already learning something: the tail removal appears less effective in simulation
 - Results show for two different implementations
 - Old from Tom, new from me
 - New is little better but neither works as well
 - Presumably there is a problem with tail simulation

Simulation displays

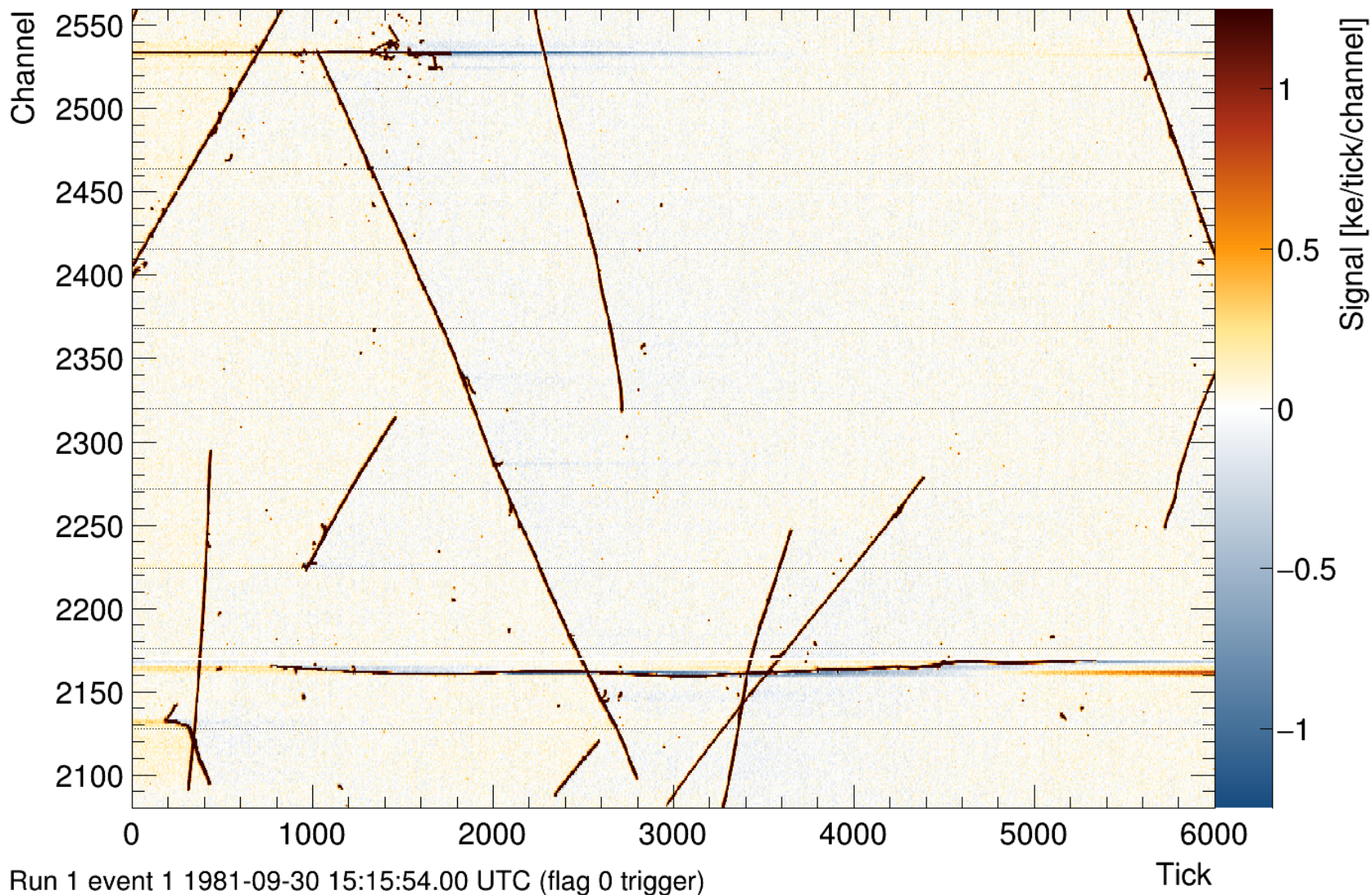
No tail removal

Prepared ADC for TPC plane 0z (APA 3: US-RaS)



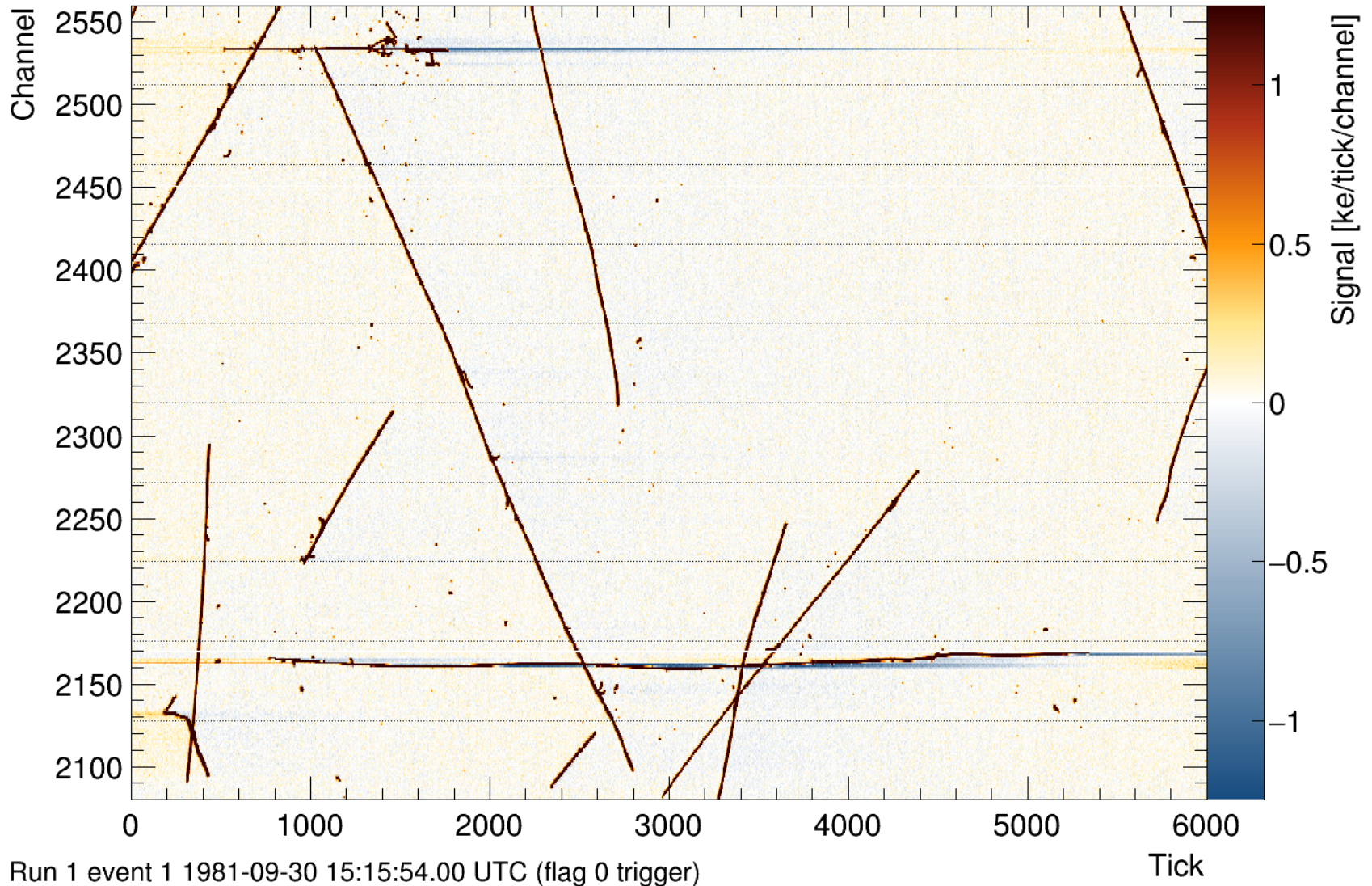
Old tail removal

Prepared ADC for TPC plane 0z (APA 3: US-RaS)



New tail removal

Prepared ADC for TPC plane 0z (APA 3: US-RaS)



New calibration data

New calibration data

Another set of pulser data was taken this month

- External pulser
- Runs 11526 - 115646
- DAC settings 1, 2, ..., 18, 21, 25, 30
- Similar datasets taken in Dec 2018, May 2019 and Dec 2019

I have begun processing the new data

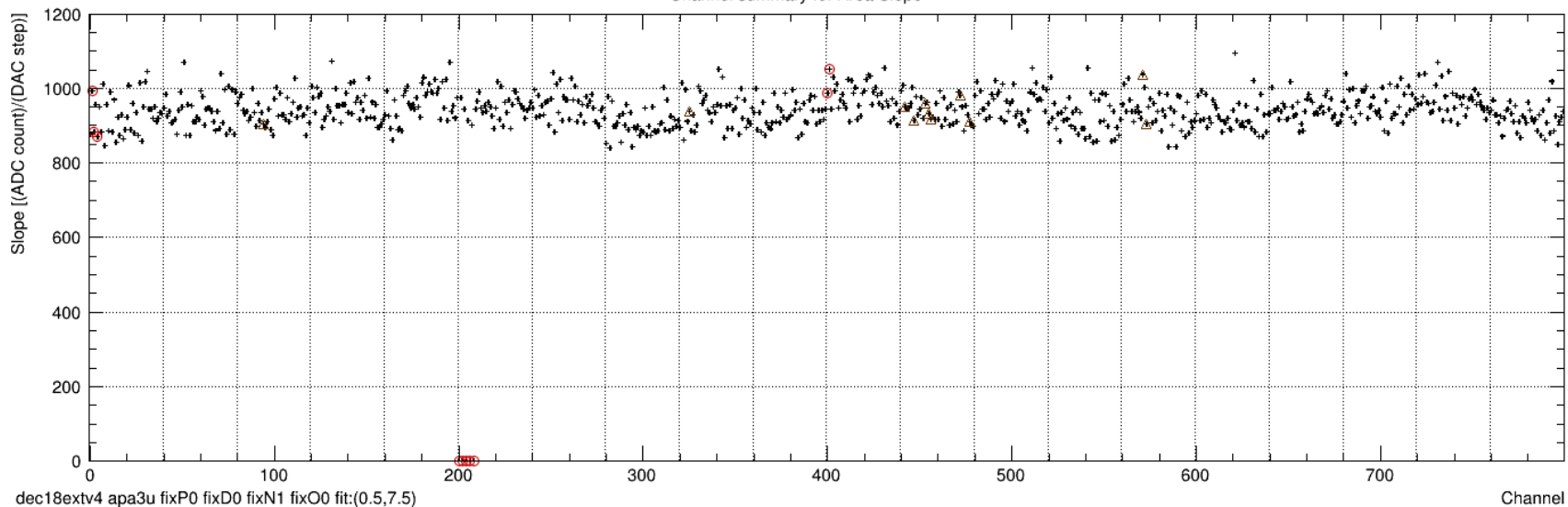
- Lar jobs to mean area for each run (DAC setting)
- Root script builds and fits graphs to obtain gain for each channel
- Code now in gitub dladams/dunececalib
 - Similar to that used to process earlier data

Comparison with old data

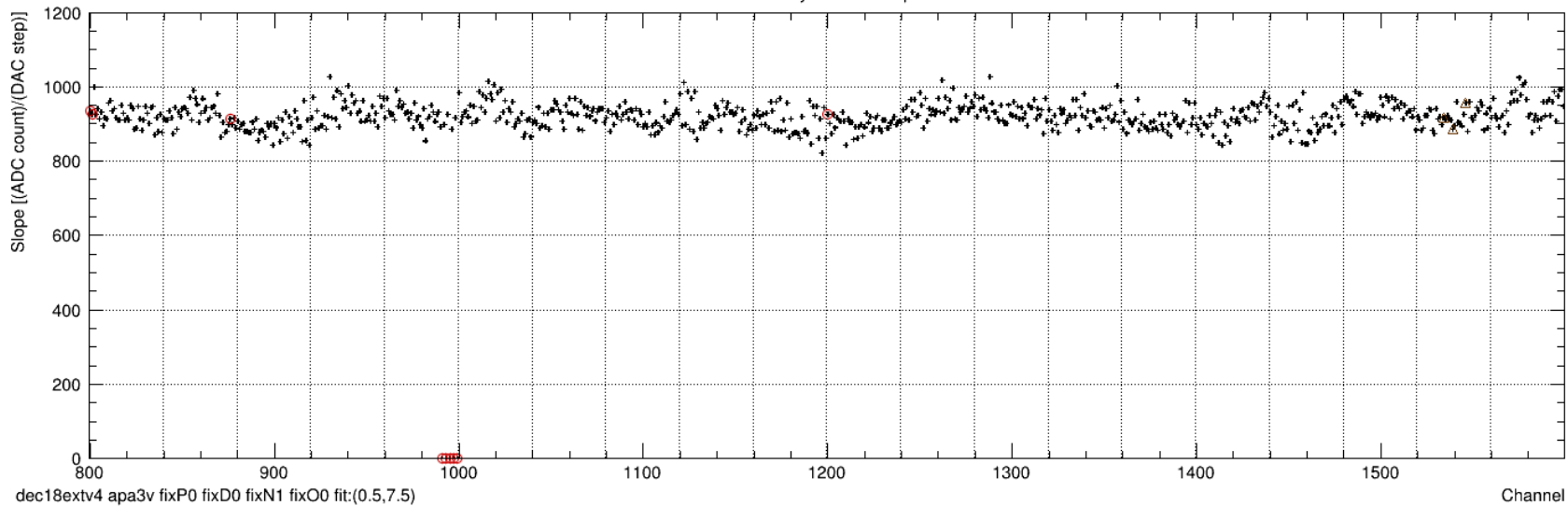
- Following slides show APA 3 slopes (ADC/DAC) for new and first data
 - Dec 2018 data is current fits with mean areas from Dec 2019 processing
- New results are similar with some channels varying by $\sim 1\%$
 - Variation is often across a full FEMB (\rightarrow change in pulser?)

APA 3 induction, Dec 2018, tight ROI

Channel summary for Area Slope

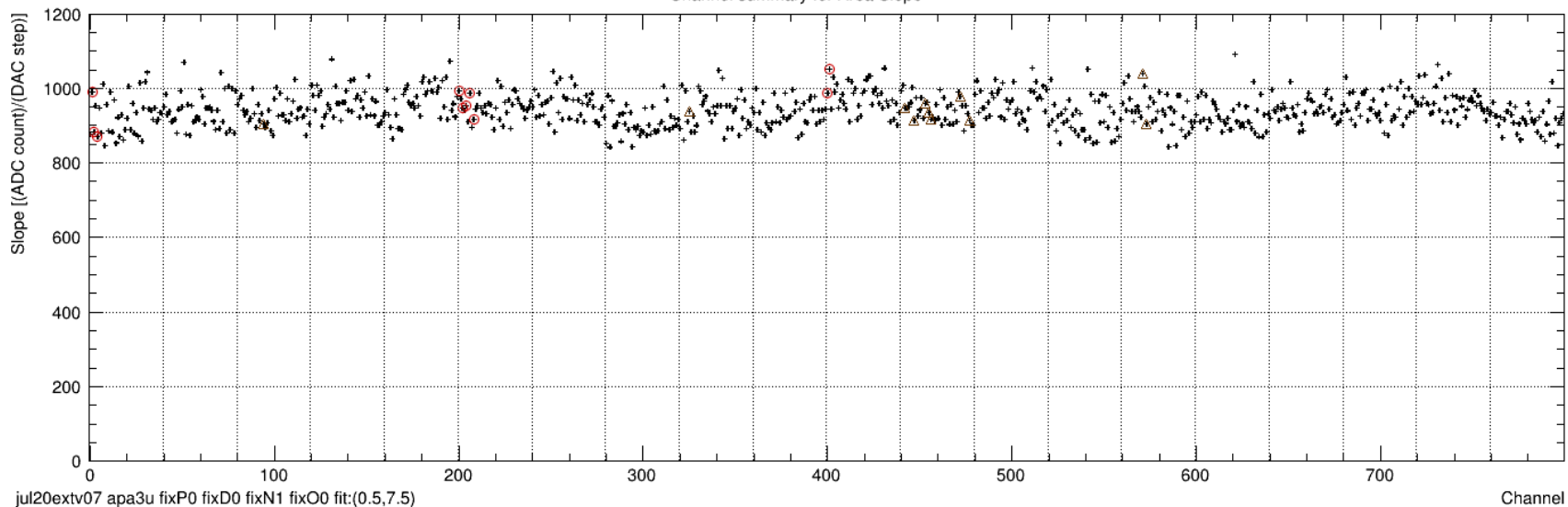


Channel summary for Area Slope

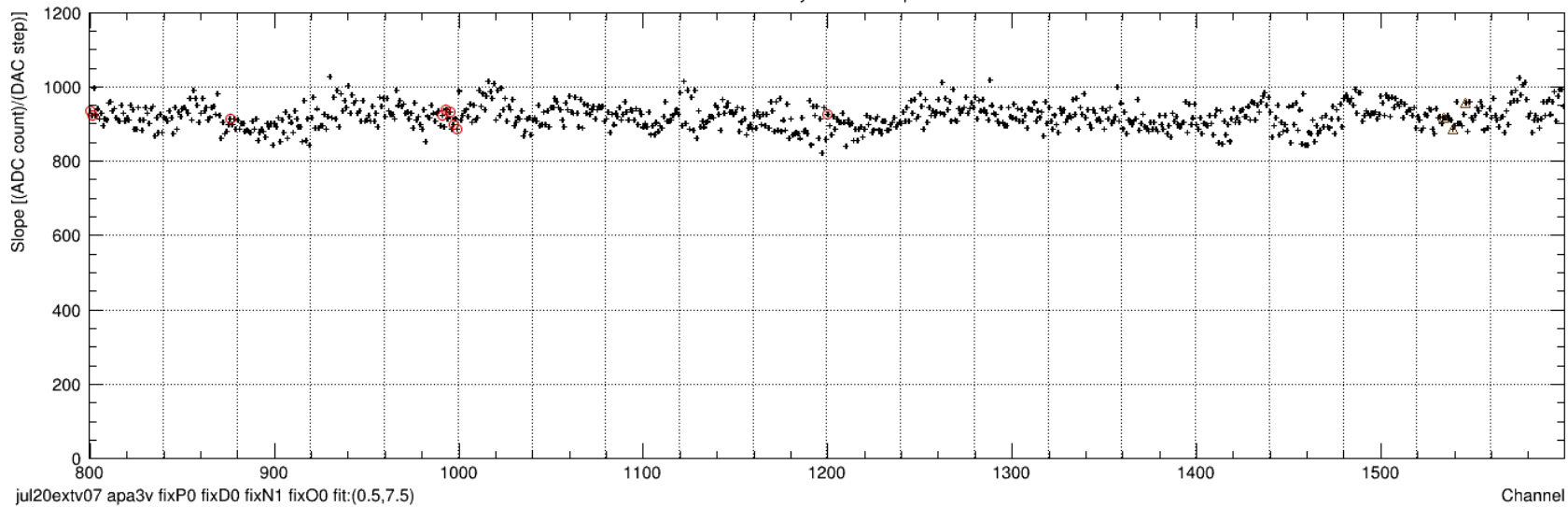


APA 3 induction, July 2020, tight ROI

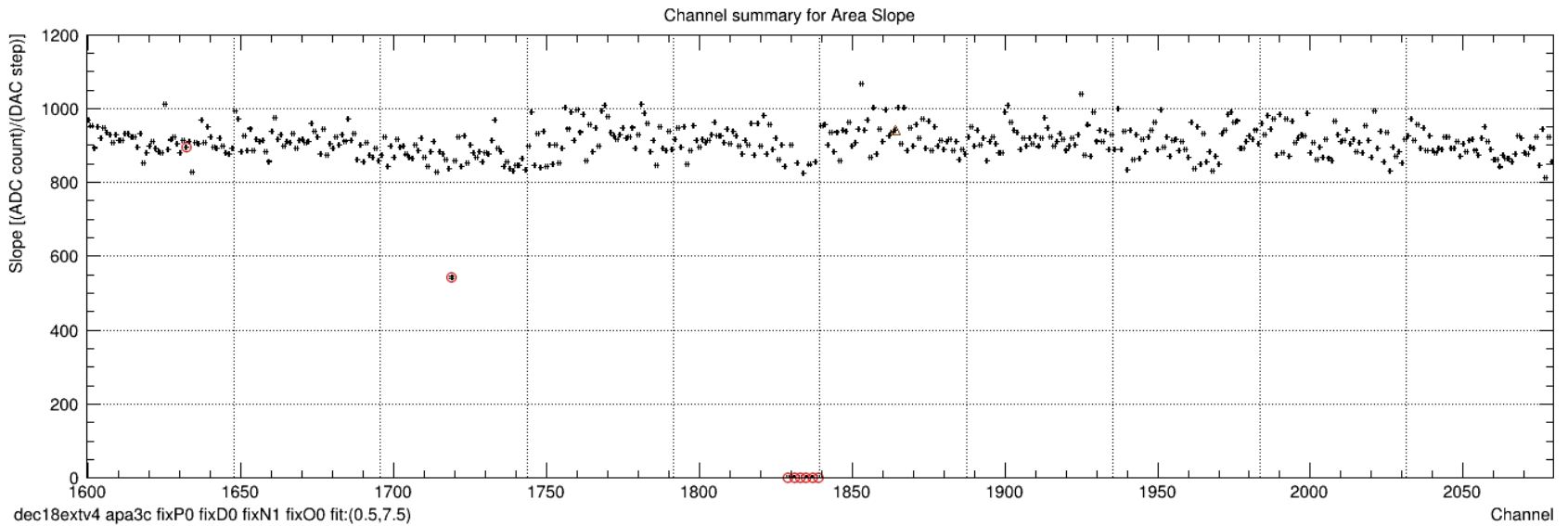
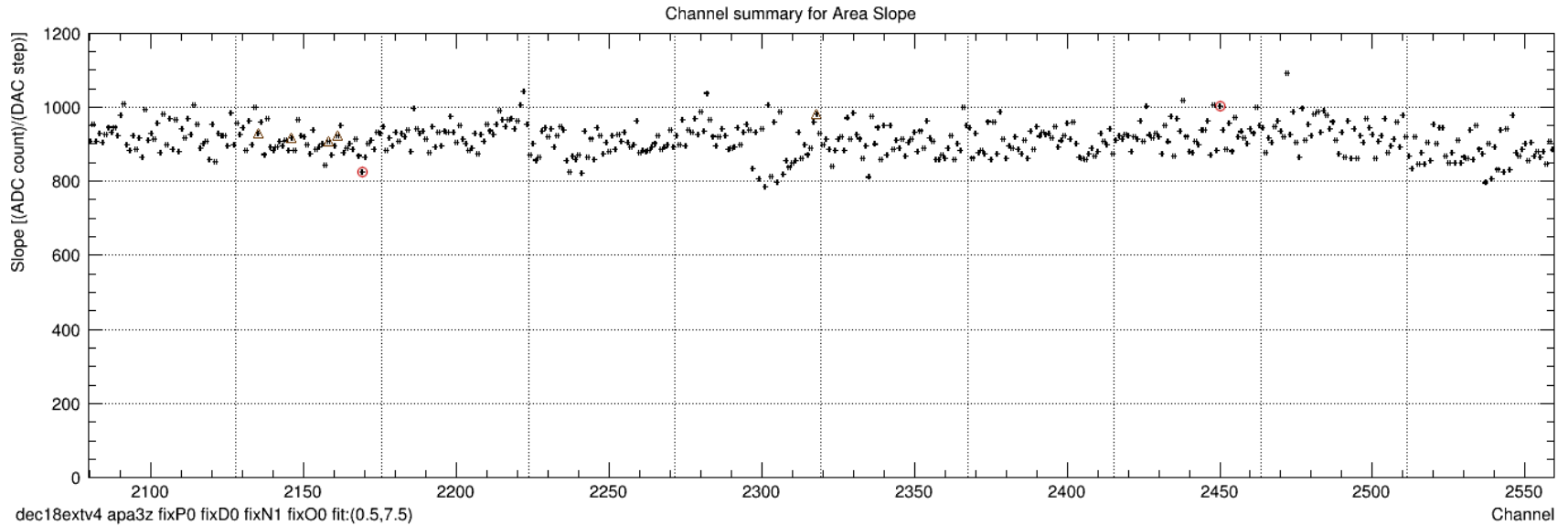
Channel summary for Area Slope



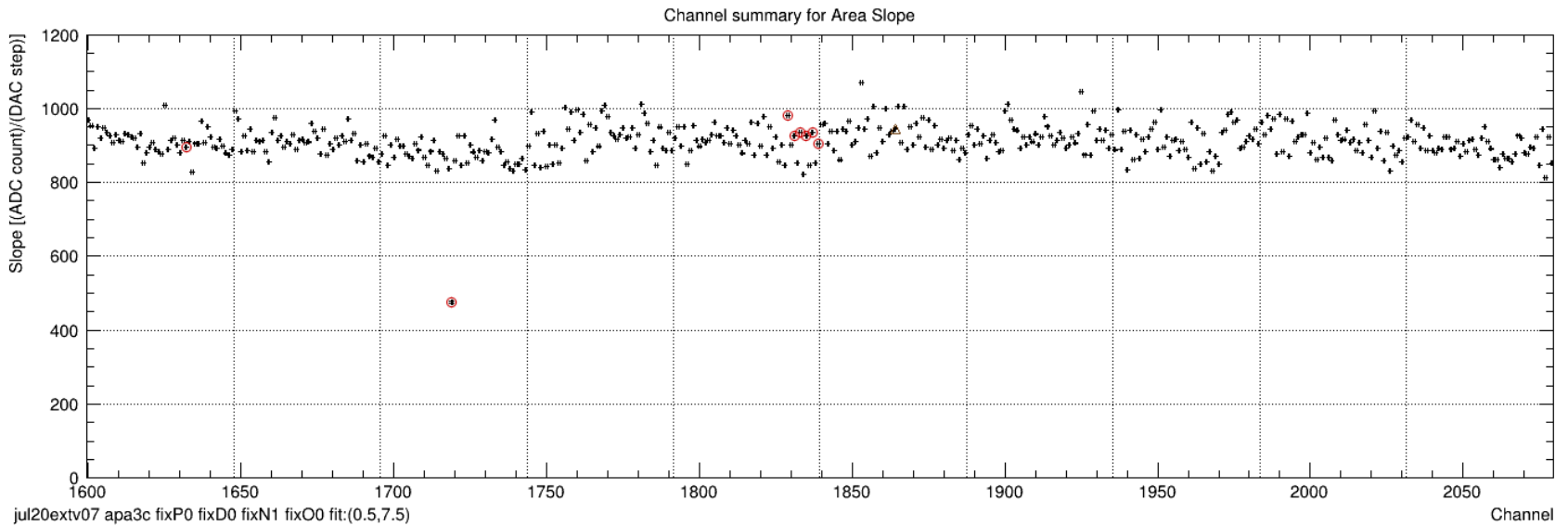
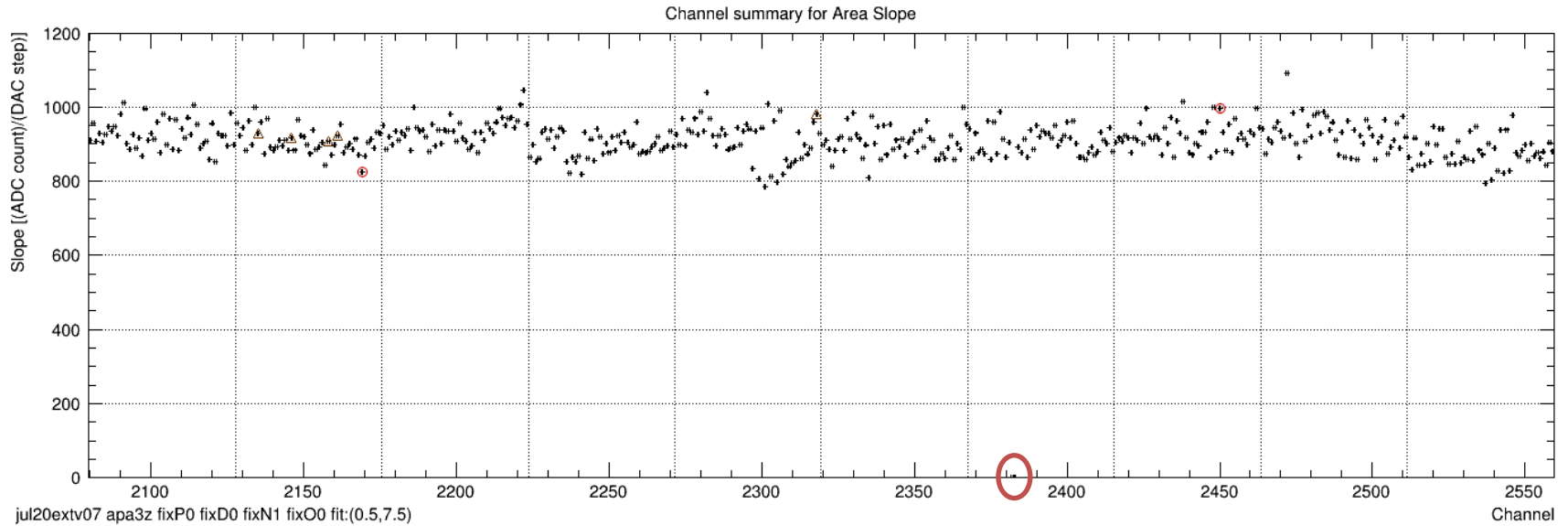
Channel summary for Area Slope



APA 3 collection, Dec 2018, tight ROI



APA 3 collection, July 2020, tight ROI



Calibration normalization

Calibration normalization

Cold CE group showed new charge injection parameters

- May 26 presentation at meeting on charge injection
 - https://indico.fnal.gov/event/43483/contributions/186922/attachments/128664/155790/Calibration_Pulse_V4_2.pdf
- Change in the charge injection capacitance:
 - $183 \rightarrow (187.8 \pm 1.4)$ fF
 - Using the nominal resistors for DAC setting 7, the step size changes:
 - $3.448 \rightarrow 3.539$ fC/(DAC step)
 - 2.6% increase in the calibrated charge
- New calibration will be released soon with this increase

Calibration normalization (2)

Charge sharing between CE and wire planes is also important

- See my talk at the May 26 meeting:
 - https://indico.fnal.gov/event/43483/contributions/186928/attachments/128665/155791/adams_duneci_20200526_pdcplib.pdf
- Scale up calibrated charge to account for signal lost to wire planes
- From that talk:

View	C_{wire} [pF]	C_{amp} [nF]	Q_{lost}/Q	Q/Q_{cal}	Revised Q/Q_{cal}
u	200	3.31	5.7%	1.060	1.025
v	200	22.0	0.9%	1.009	1.004
x	150	3.31	4.3%	1.045	1.020

- But some (about half?) of the capacitance is to wires in the same plane and we don't want to double count that contribution when we integrate over multiple wires
 - My guess at the corrections to use are shown in the table on the right
 - Should we include these in our calibrated charge?