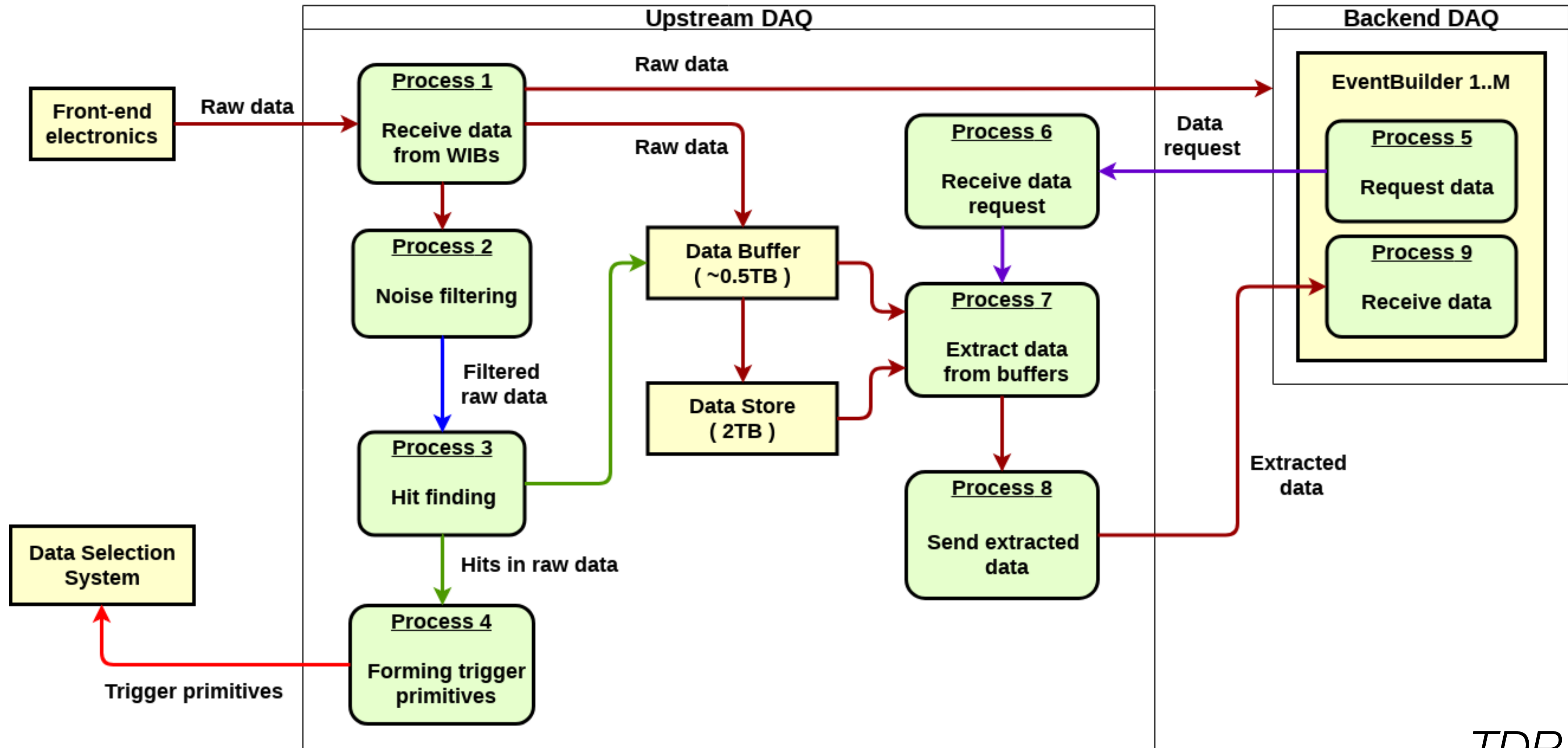


Upstream DAQ Technology Review

J. Brooke, R. Sipos

High-Level Upstream DAQ Design



Goals

1. Review progress on implementation of Upstream DAQ components:

- Trigger primitive generation
 - Latency (10s) buffer
 - SNB (100s) buffer
 - Data request handling
- A great deal of impressive work has been done !
- ## 2. Identify/revise baseline design for each component
- Starting with technical review in this workshop
 - Followed by discussion with stakeholders & DUNE DAQ coordination team before concluding

Readout Infrastructure (per FD module)

- 1 barrack underground (max 125 kW, 16 racks)
- Approx 80 servers (at least 2U) to readout 150 APAs + PDS
- Each server will readout 2 APAs using *1 or 2* FELIX PCIe cards
 - TDR includes additional co-processors hosted on PCIe cards
 - Now anticipate all processing to be on the PCI card itself
- Triggered data sent to storage & high-level filter on the surface

Readout System Variants

<i>Combination</i>	<i>HitFinding</i>	<i>10s buffer</i>	<i>SNB store</i>
A	Host	Host	Host
B	FPGA	Host	Host
C	FPGA	FPGA	FPGA

- Viable combinations of FW/SW implementation of the functional elements
 - (In order to maintain un-directional data flow between PCI board and host)

Readout Modes

1. **Standard trigger requests**

- Time window variable on event-by-event basis: few us to few s
- Not time-ordered

2. **Debug/calibration streams**

- Stream full bandwidth from single link to output based on headers
- Configurable streaming

3. **Supernova burst**

- Stream all inputs to local storage following SNB trigger
 - TDR foresees latency of 10s, time window of 100s

Readout Failure Scenarios

1. **Low-level FE failure**

- Single link failure

2. **Link alignment errors**

- Missing data blocks/non-consecutive timestamps

3. **Uncompressable data**

- Data from an FEB cannot be compressed

- This list is incomplete; should be treated as a starting point for understanding resilience

Criteria

- Broad categories
 - Features
 - Adaptability
 - Reliability
 - Long term support
 - Resource requirements
- Detailed questions on the review document
 - https://indico.fnal.gov/event/44240/attachments/131513/161079/DUNE_Upstream_DAQ_-_Readout_Technology_evaluation.pdf

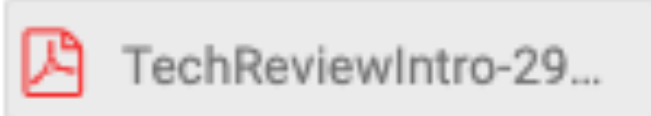

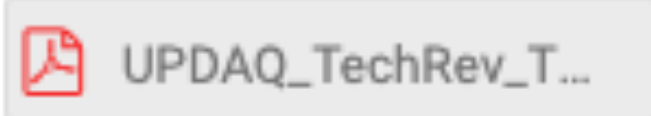

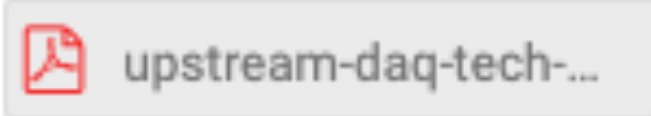


Physics Performance

- Physics performance not included in criteria
- A **single** trigger primitive algorithm has been implemented in both FW and SW
 - Physics performance expected to be **identical**
 - Modulo bugs etc.
- Amount of ‘spare’ resources may have an impact in future
 - **If** these resources can be successfully deployed in a way that increases physics impact

Cost

- Cost not included in criteria
 - Clearly, the ***design must be implemented with available funding***
 - However, information to consistently cost the options is not currently available
- One goal of the review is to understand requirements in terms of ***resources*** and ***specifications***
- This should (we hope) allow a full costing after the review workshop
 - Will organise this with representatives from funding institutes/countries, ie. UK, CERN, Canada

Workshop Agenda

WEDNESDAY, 29 JULY		
8:00 AM → 8:15 AM	Introduction Speakers: Jim Brooke, Roland Sipos (CERN) 	🕒 15m 
8:15 AM → 9:00 AM	Trigger Primitive Generation - Firmware Speakers: Dr Konstantinos Manolopoulos (Rutherford Appleton Laboratory), Konstantinos Manolopoulos (Rutherford Appleton Laboratory) 	🕒 45m 
9:15 AM → 10:00 AM	Trigger Primitive Generation - Software Speaker: Philip Rodrigues (University of Oxford) 	🕒 45m 
10:15 AM → 10:30 AM	Coffee break	🕒 15m
10:30 AM → 11:30 AM	Discussion	🕒 1h 

Workshop Agenda

THURSDAY, 30 JULY



8:00 AM

→ 8:45 AM

10s/100s Buffer - Software

🕒 45m



Speakers: Adam Abed Abud (University of Liverpool, CERN), Adam Abed Abud

latency_buffer_SNB...

9:00 AM

→ 9:45 AM

10s/100s Buffer - Firmware

🕒 45m



Speakers: David Cussans (University of Bristol), Erdem Motuk, Erdem Motuk

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10:00 AM

→ 10:15 AM

Coffee break

🕒 15m

10:15 AM

→ 11:15 AM

Discussion

🕒 1h



11:15 AM

→ 11:30 AM

Closeout

🕒 15m



Workshop Agenda

THURSDAY, 30 JULY

8:00 AM → 8:45 AM 10s/100s Buffer - Software

45m

- Agenda includes time for questions **after** the talks
- Time for discussion scheduled at the end of each session

9:00

- If more time is needed - please help identify topics
 - We can schedule time in forthcoming UD meetings

10:00

- We will record the sessions on Zoom and upload to agenda afterwards

10:15

11:15 AM → 11:30 AM Closeout

15m