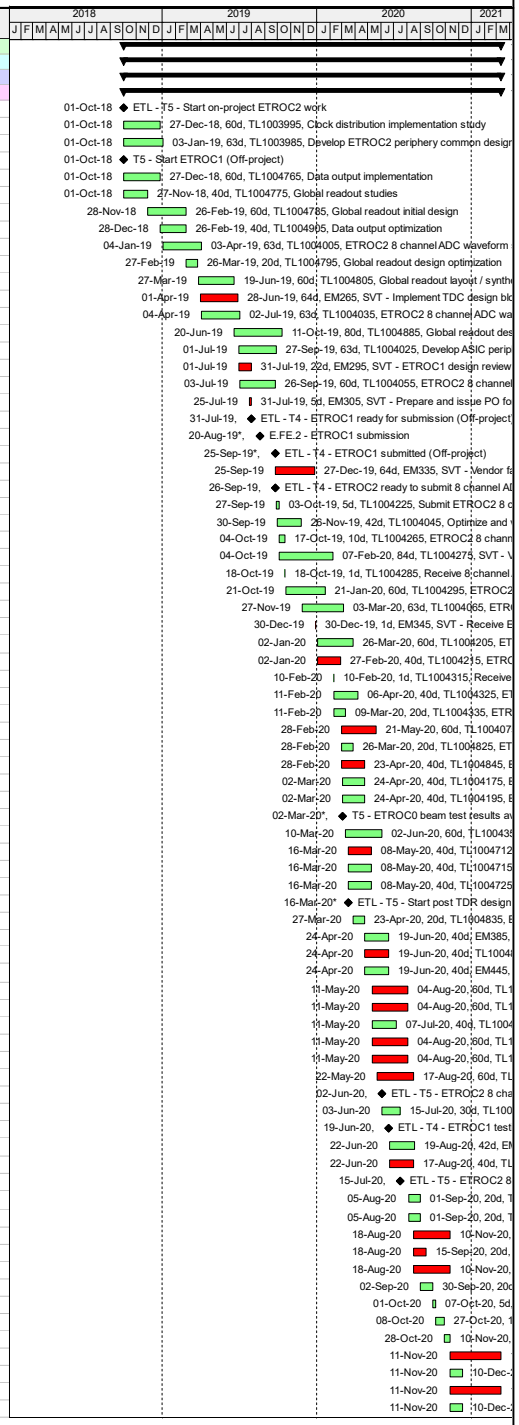
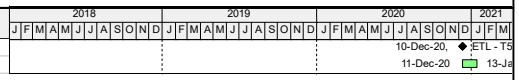
Activity ID	Activity Name	Responsibl Institution	Perform Institutio	Planned Start	Planned Duration	Planned Labor Units	Planned Labor Cost	Planned Nonlabor Units	Planned Nonlabor Cost	Planned Material Cost	Estimate Type	Resource IDs
DOE-CD1-402.8-FC2	402.8 TL - Timing Layer (at DOE CD1) - Copy for FC-11Oct19			01-Oct-18	612d	5936h	$907,994.96	12017h	$407,531.75	$32,735.80		
DOE-CD1-402.8-FC2.4	ETL - Endcap Timing Layer			01-Oct-18	612d	5936h	$907,994.96	12017h	$407,531.75	$32,735.80		
DOE-CD1-402.8-FC2.4.2	ETL - Frontend ASICs			01-Oct-18	612d	5936h	$907,994.96	12017h	$407,531.75	$32,735.80		
DOE-CD1-402.8-FC2.4.2.5	ETL - Frontend ASICs v2 development (CD-2)			01-Oct-18	612d	5936h	$907,994.96	12017h	$407,531.75	$32,735.80		
TL1003975	ETL - T5 - Start on-project ETROC2 work			01-Oct-18	0d	0h	$0.00	0h	$0.00	$0.00		
TL1003995	Clock distribution implementation study	FN	FN	01-Oct-18	60d	144h	$22,113.16	0h	$0.00	$0.00	L1	FNd_ASIC_DESIGN_EN
TL1003985	Develop ETROC2 periphery common design blocks - FNAL	FN	FN	01-Oct-18	63d	864h	$132,678.95	0h	$0.00	$0.00	L1	FNd_ASIC_DESIGN_EN
EM205	T5 - Start ETROC1 (Off-project)			01-Oct-18	0d	0h	$0.00	0h	$0.00	$0.00		
TL1004765	Data output implementation	FN	FN	01-Oct-18	60d	144h	$22,113.16	0h	$0.00	$0.00	L1	FNd_ASIC_DESIGN_EN
TL1004775	Global readout studies	FN	FN	01-Oct-18	40d	160h	$24,570.18	0h	$0.00	$0.00	L1	FNd_ASIC_DESIGN_EN
TL1004785	Global readout initial design	FN	FN	28-Nov-18	60d	240h	$36,855.26	0h	$0.00	$0.00	L1	FNd_ASIC_DESIGN_EN
TL1004905	Data output optimization	FN	FN	28-Dec-18	40d	160h	$24,570.18	0h	$0.00	$0.00	L1	FNd_ASIC_DESIGN_EN
TL1004005	ETROC2 8 channel ADC waveform sampling design (FSC)	FN	SM	04-Jan-19	63d	0h	$0.00	887h	$25,725.66	$0.00	L1	CMS-HL_FN_SM_P_ENG_GRAD_STUD
TL1004795	Global readout design optimization	FN	FN	27-Feb-19	20d	80h	$12,285.09	0h	$0.00	$0.00	L1	FNd_ASIC_DESIGN_EN
TL1004805	Global readout layout / synthesis	FN	FN	27-Mar-19	60d	240h	$36,855.26	0h	$0.00	$0.00	L1	FNd_ASIC_DESIGN_EN
EM265	SVT - Implement TDC design blocks (Off-project)			01-Apr-19	64d	0h	$0.00	0h	$0.00	$0.00		
TL1004035	ETROC2 8 channel ADC waveform sampling improvements (FSC)	FN	SM	04-Apr-19	63d	0h	$0.00	282h	$8,178.85	$0.00	L1	CMS-HL_FN_SM_P_ENG_GRAD_STUD
TL1004885	Global readout design simulation / verification	FN	FN	20-Jun-19	80d	320h	$49,340.13	0h	$0.00	$0.00	L1	FNd_ASIC_DESIGN_EN
TL1004025	Develop ASIC periphery common design blocks - SMU	FN	SM	01-Jul-19	63d	0h	$0.00	887h	$24,602.45	$0.00	L4	CMS-HL_FN_SM_P_PHYS_GRAD_STUD
EM295	SVT - ETROC1 design review (Off-project)			01-Jul-19	22d	0h	$0.00	0h	$0.00	$0.00		
TL1004055	ETROC2 8 channel ADC waveform sampling initial rad-hard version design (FSC)	FN	SM	03-Jul-19	60d	0h	$0.00	845h	$24,507.53	$0.00	L1	CMS-HL_FN_SM_P_ENG_GRAD_STUD
EM305	SVT - Prepare and issue PO for ETROC1 (Off-project)			25-Jul-19	5d	0h	$0.00	0h	$0.00	$0.00		
EM315	ETL - T4 - ETROC1 ready for submission (Off-project)				0d	0h	$0.00	0h	$0.00	$0.00		
EM455	E.FE.2 - ETROC1 submission				0d	0h	$0.00	0h	$0.00	$0.00		
EM325	ETL - T4 - ETROC1 submitted (Off-project)				0d	0h	$0.00	0h	$0.00	$0.00		
EM335	SVT - Vendor fabricates ETROC1 (Off-project)			25-Sep-19	64d	0h	$0.00	0h	$0.00	$0.00		
TL1004095	ETL - T4 - ETROC2 ready to submit 8 channel ADC waveform sampling mini-ASIC				0d	0h	$0.00	0h	$0.00	$0.00		
TL1004225	Submit ETROC2 8 channel ADC waveform sampling mini-ASIC	FN	SM	27-Sep-19	5d	0h	$0.00	70h	$2,069.25	$0.00	L1	CMS-HL_FN_SM_P_ENG_GRAD_STUD
TL1004045	Optimize and verify ASIC periphery common design blocks	FN	FN	30-Sep-19	42d	576h	$91,573.04	0h	$0.00	$0.00	L4	FNd_ASIC_DESIGN_EN, FNd_ASIC_DESIGN_E
TL1004265	ETROC2 8 channel ADC waveform sampling testing specification	FN	SM	04-Oct-19	10d	0h	$0.00	70h	$2,095.28	$0.00	L3	CMS-HL_FN_SM_P_ENG_GRAD_STUD
TL1004275	SVT - Vendor fabricates 8 channel ADC waveform mini-ASIC	FN	SM	04-Oct-19	84d	0h	$0.00	0h	$0.00	$0.00		
TL1004285	Receive 8 channel ADC waveform sampling mini-ASIC testing hardware (FSC)	FN	FN	18-Oct-19	1d	0h	$0.00	0h	$0.00	$6,639.00	M1	FN_MS_STND_FY19
TL1004295	ETROC2 8 channel ADC waveform sampling testing plateform development	FN	SM	21-Oct-19	60d	0h	$0.00	845h	$25,292.96	$0.00	L4	CMS-HL_FN_SM_P_ENG_GRAD_STUD
TL1004065	ETROC2 Periphery integration	FN	FN	27-Nov-19	63d	216h	$34,368.43	0h	$0.00	$0.00	L4	FNd_ASIC_DESIGN_EN
EM345	SVT - Receive ETROC1 (Off-project)			30-Dec-19	1d	0h	$0.00	0h	$0.00	$0.00		
TL1004205	ETROC1: TDC block functional testing - SMU	FN	SM	02-Jan-20	60d	0h	$0.00	282h	$8,072.81	$0.00	L4	CMS-HL_FN_SM_P_PHYS_GRAD_STUD
TL1004215	ETROC1: Preamp + discriminator + TDC full chain single channel functional testing - SMU	FN	SM	02-Jan-20	40d	0h	$0.00	282h	$8,072.81	$0.00	L4	CMS-HL_FN_SM_P_PHYS_GRAD_STUD
TL1004315	Receive ETROC2 8 channel ADC waveform sampling mini-ASCI (FSC)	FN	FN	10-Feb-20	1d	0h	$0.00	0h	$0.00	$23,900.40	M3	FN_MS_STND_FY19
TL1004325	ETROC2 8 channel ADC waveform sampling mini-ASIC testing	FN	SM	11-Feb-20	40d	0h	$0.00	564h	$16,881.93	$0.00	L4	CMS-HL_FN_SM_P_ENG_GRAD_STUD
TL1004335	ETROC2 8 channel ADC waveform sampling mini-ASIC irradiation (FSC)	FN	SM	11-Feb-20	20d	0h	$0.00	564h	$16,881.93	$0.00	L4	CMS-HL_FN_SM_P_ENG_GRAD_STUD
TL1004075	DAQ with pixel level readout inital design	FN	FN	28-Feb-20	60d	240h	$38,187.14	0h	$0.00	$0.00	L4	FNd_ASIC_DESIGN_EN
TL1004825	ETROC1: Preamp + discriminator + TDC full chain single channel testing with wire bonde	FN	SM	28-Feb-20	20d	0h	$0.00	80h	$2,290.16	$0.00	L4	CMS-HL_FN_SM_P_PHYS_GRAD_STUD
TL1004845	ETROC1: 4x4 array testing with bump bonded sensor, initial functional testing	FN	SM	28-Feb-20	40d	0h	$0.00	282h	$8,072.81	$0.00	L4	CMS-HL_FN_SM_P_PHYS_GRAD_STUD
TL1004175	ETROC2 Preamp design optimization	FN	FN	02-Mar-20	40d	160h	$25,458.10	0h	$0.00	$0.00	L4	FNd_ASIC_DESIGN_EN
TL1004195	ETROC2 Discriminator design optimization	FN	FN	02-Mar-20	40d	160h	$25,458.10	0h	$0.00	$0.00	L4	FNd_ASIC_DESIGN_EN
EM435	T5 - ETROC0 beam test results available				0d	0h	$0.00	0h	$0.00	$0.00		
TL1004355	Design modifications to rad-hard version of ADC waveform sampling (FSC)	FN	SM	10-Mar-20	60d	0h	$0.00	845h	$25,292.96	$0.00	L4	CMS-HL_FN_SM_P_ENG_GRAD_STUD
TL1004712	Clock generation / distribution design studies	FN	FN	16-Mar-20	40d	176h	$25,458.10	0h	$0.00	$0.00		FNd_ASIC_DESIGN_EN, FN_U_PT_EXP_PHYS
TL1004715	Floor plan studies	FN	FN	16-Mar-20	40d	176h	$25,458.10	0h	$0.00	$0.00	L4	FNd_ASIC_DESIGN_EN, FN_U_PT_EXP_PHYS
TL1004725	Power distribution initial design study	FN	FN	16-Mar-20	40d	176h	$25,458.10	0h	$0.00	$0.00	L4	FNd_ASIC_DESIGN_EN, FN_U_PT_EXP_PHYS
TL1004815	ETL - T5 - Start post TDR design			16-Mar-20	0d	0h	$0.00	0h	$0.00	$0.00		
TL1004835	ETROC1: Preamp + discriminator + TDC full chain single channel beam test - SMU	FN	SM	27-Mar-20	20d	0h	$0.00	80h	$2,290.16	$0.00	L4	CMS-HL_FN_SM_P_PHYS_GRAD_STUD
EM385	Irradiate ETROC1 for single pixel full chain testing	FN	SM	24-Apr-20	40d	0h	$0.00	160h	$4,580.32	$0.00	L4	CMS-HL_FN_SM_P_PHYS_GRAD_STUD
TL1004855	ETROC1: 4x4 array testing with bump bonded sensor, beam testing	FN	SM	24-Apr-20	40d	0h	$0.00	282h	$8,072.81	$0.00	L4	CMS-HL_FN_SM_P_PHYS_GRAD_STUD
EM445	Irradiate ETROC1 for array testing	FN	SM	24-Apr-20	40d	0h	$0.00	160h	$4,580.32	$0.00		CMS-HL_FN_SM_P_PHYS_GRAD_STUD
TL1004735	Clock generation / distribution design implementation - FNAL	FN	FN	11-May-20	60d	136h	$19,093.57	0h	$0.00	$0.00		FNd_ASIC_DESIGN_EN, FN_U_PT_EXP_PHYS
TL1004745	Clock and fast command implementation - FNAL	FN	FN	11-May-20	60d	136h	$19,093.57	0h	$0.00	$0.00	L4	FNd_ASIC_DESIGN_EN, FN_U_PT_EXP_PHYS
TL1004755	I2C implementation	FN	FN	11-May-20	40d	176h	$25,458.10	0h	$0.00	$0.00	L4	FNd_ASIC_DESIGN_EN, FN_U_PT_EXP_PHYS
TL1007765	Clock generation / distribution design implementation - SMU	FN	SM	11-May-20	60d	0h	$0.00	600h	$22,812.20	$0.00		CMS-HL_FN_SM_P_PHYS_ASIC_DES, CMS-HL
TL1007775	Clock and fast command implementation - SMU	FN	SM	11-May-20	60d	0h	$0.00	600h	$22,812.20	$0.00	L4	CMS-HL_FN_SM_P_PHYS_ASIC_DES, CMS-HL
TL1004895	DAQ with pixel level readout layout / synthesis	FN	FN	22-May-20	60d	264h	$38,187.14	0h	$0.00	$0.00	L4	FNd_ASIC_DESIGN_EN, FN_U_PT_EXP_PHYS
TL1004385	ETL - T5 - ETROC2 8 channel rad-hard ADC waveform sampling design done				0d	0h	$0.00	0h	$0.00	$0.00		
TL1004395	Integration of 8 channel rad-hard ADC waveform sampling	FN	SM	03-Jun-20	30d	0h	$0.00	140h	$4,190.55	$0.00	L4	CMS-HL_FN_SM_P_ENG_GRAD_STUD
EM415	ETL - T4 - ETROC1 testing results available (Off-project)				0d	0h	$0.00	0h	$0.00	$0.00		
EM395	ETROC2 TDC Optimization			22-Jun-20	42d	0h	$0.00	0h	$0.00	$0.00		
TL1004865	ETROC1: 4x4 array testing with bump bonded sensor, clock distribution studies	FN	SM	22-Jun-20	40d	0h	$0.00	282h	$8,072.81	$0.00	L4	CMS-HL_FN_SM_P_PHYS_GRAD_STUD
TL1004405	ETL - T5 - ETROC2 8 channel rad-hard ADC waveform sampling integration done				0d	0h	$0.00	0h	$0.00	$0.00		
TL1004915	ETROC2 emulator design specification - FNAL	FN	FN	05-Aug-20	20d	48h	$6,364.52	0h	$0.00	$0.00	L4	FNd_ELTN_DESIGN_EN, FN_U_PT_EXP_PHYS
TL1007885	ETROC2 emulator design specification - SMU	FN	SM	05-Aug-20	20d	0h	$0.00	40h	$2,814.87	$0.00	L4	CMS-HL_FN_SM_P_PHYS_ASIC_DES
TL1004305	Pixel level integration (preamp + discriminator + TDC + DAQ readout) - FNAL	FN	FN	18-Aug-20	60d	144h	$19,749.13	0h	$0.00	$0.00	L4	FNd_ASIC_DESIGN_EN, FN_U_PT_EXP_PHYS
TL1004875	Clock generation / distribution design optimization	FN	FN	18-Aug-20	20d	88h	$12,729.05	0h	$0.00	$0.00		FNd_ASIC_DESIGN_EN, FN_U_PT_EXP_PHYS
TL1007785	Pixel level integration (preamp + discriminator + TDC + DAQ readout) - SMU	FN	SM	18-Aug-20	60d	0h	$0.00	600h	$23,187.08	$0.00	L4	CMS-HL_FN_SM_P_PHYS_ASIC_DES, CMS-HL
TL1004925	ETROC2 emulator prototype hardware development	FN	SM	02-Sep-20	20d	0h	$0.00	80h	$5,629.74	$0.00	L4	CMS-HL_FN_SM_P_PHYS_ASIC_DES
TL1004935	Prepare and issue PO for ETROC2 emulator prototype hardware	FN	SM	01-Oct-20	5d	0h	$0.00	16h	$1,164.23	$0.00	L4	CMS-HL_FN_SM_P_PHYS_ASIC_DES
TL1004995	SVT - Vendor fabricates ETROC2 emulator prototype hardware	FN	FN	08-Oct-20	14d	0h	$0.00	0h	$0.00	$0.00	L4	
TL1007835	Receive ETROC2 emulator prototype hardware (M&S)	FN	FN	28-Oct-20	10d	0h	$0.00	0h	$0.00	$2,196.40	M4	FN_MS_STND_FY19
TL1004425	ETROC2 global integration / design verification - FNAL	FN	FN	11-Nov-20	80d	672h	$109,066.11	0h	$0.00	$0.00	L4	FNd_ASIC_DESIGN_EN, FN_U_PT_EXP_PHYS
TL1004955	ETROC2 emulator prototype firmware development - FNAL	FN	FN	11-Nov-20	20d	40h	$5,453.31	0h	$0.00	$0.00	L4	FNd_ELTN_DESIGN_EN, FN_U_PT_EXP_PHYS
TL1007795	ETROC2 global integration / design verification - SMU	FN	SM	11-Nov-20	80d	0h	$0.00	1920h	$86,185.41	$0.00	L4	CMS-HL_FN_SM_P_PHYS_ASIC_DES, CMS-HL
TL1007805	ETROC2 emulator prototype firmware development - SMU	FN	SM	11-Nov-20	20d	0h	$0.00	192h	$7,280.49	$0.00	L4	CMS-HL_FN_SM_P_PHYS_ASIC_DES, CMS-HL



© Oracle Corporation

Activity ID	Activity Name	Responsibl Institution	Perform Institutio	Planned Start	Planned Duration	Planned Labor Units	Planned Labor Cost	Planned Nonlabor Units	Planned Nonlabor Cost	Planned Material Cost	Estimate Type	Resource IDs
TL1005025	ETL - T5 - ETROC2 emulator prototype ready				0d	0h	$0.00	0h	$0.00	$0.00		
TL1004965	ETROC2 emulator v1 hardware development	FN	SM	11-Dec-20	20d	0h	$0.00	80h	$5,821.14	$0.00	L4	CMS-HL_FN_SM_P_PHYS_ASIC_DES



Remaining Level of Effort | Remaining Work | Actual Work | Critical Remainin...

TASK filters: ETROC v2 (CD-2), Start Date.

© Oracle Corporation