The CMS High Granularity Endcap Calorimeter for HL-LHC

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Snowmass IF/Calorimetry Monthly Meeting
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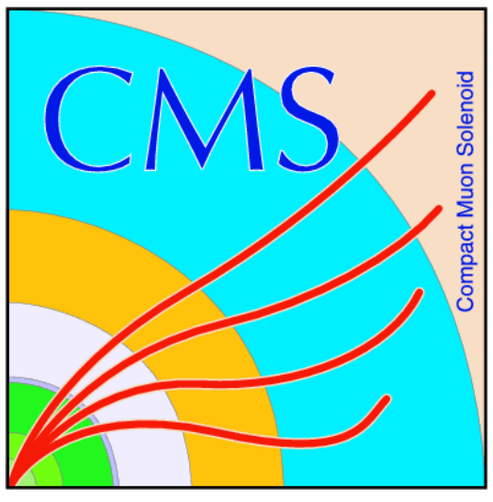
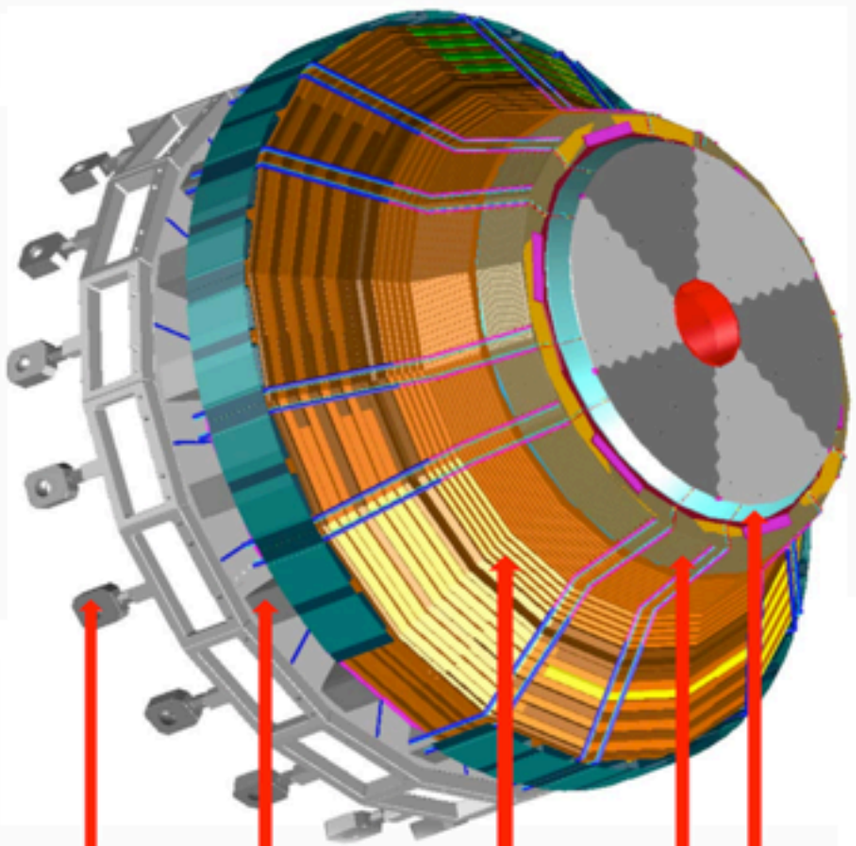
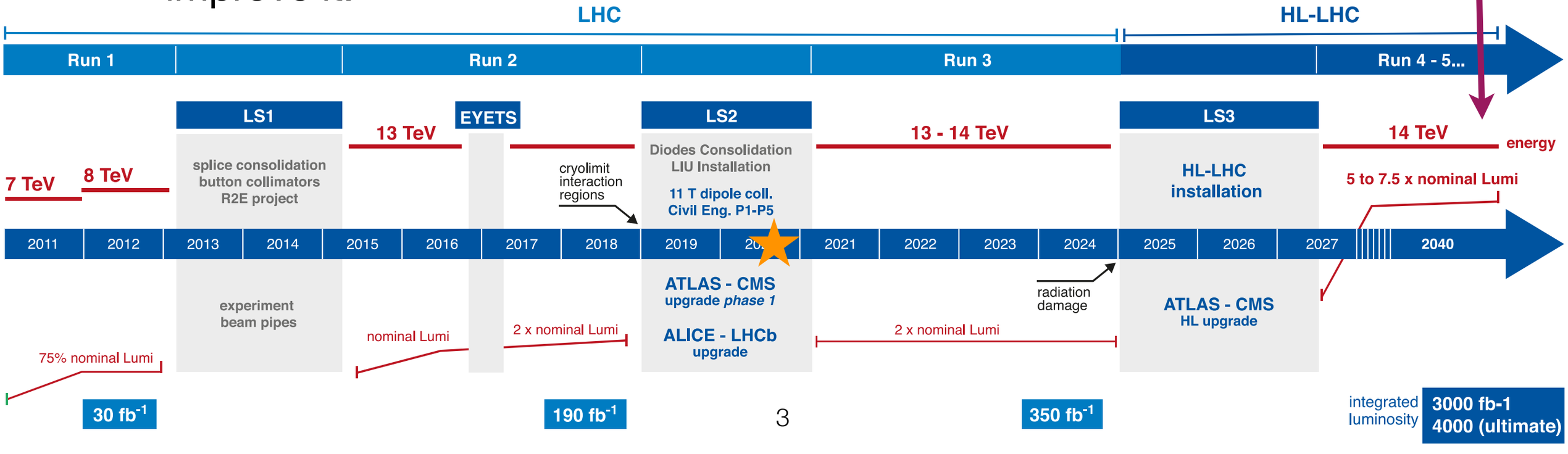




HGCAL

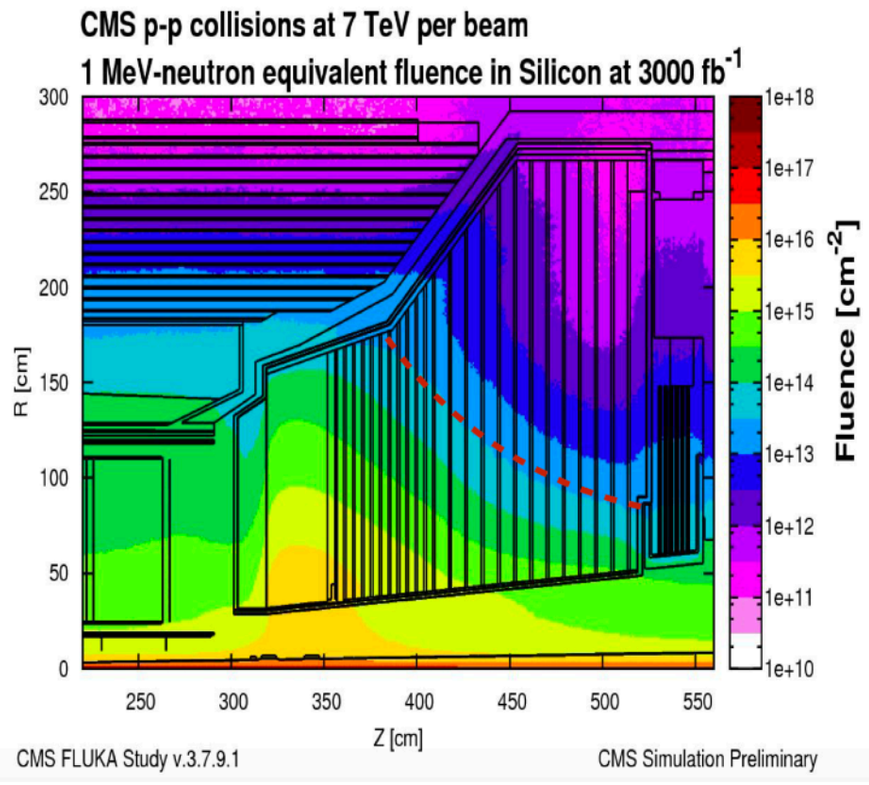
A new endcap calorimeter for the CMS experiment

- High-luminosity LHC comes with higher instantaneous luminosity, and very large integrated luminosity
  - Radiation damage more severe
  - High pileup resulting in higher occupancy
  - Higher data volume and trigger rates
- Existing endcap calorimeters (ECAL+HCAL) were not designed to withstand these conditions, and thus need to be replaced
- Opportunity to not only maintain current physics capabilities, but to improve it!



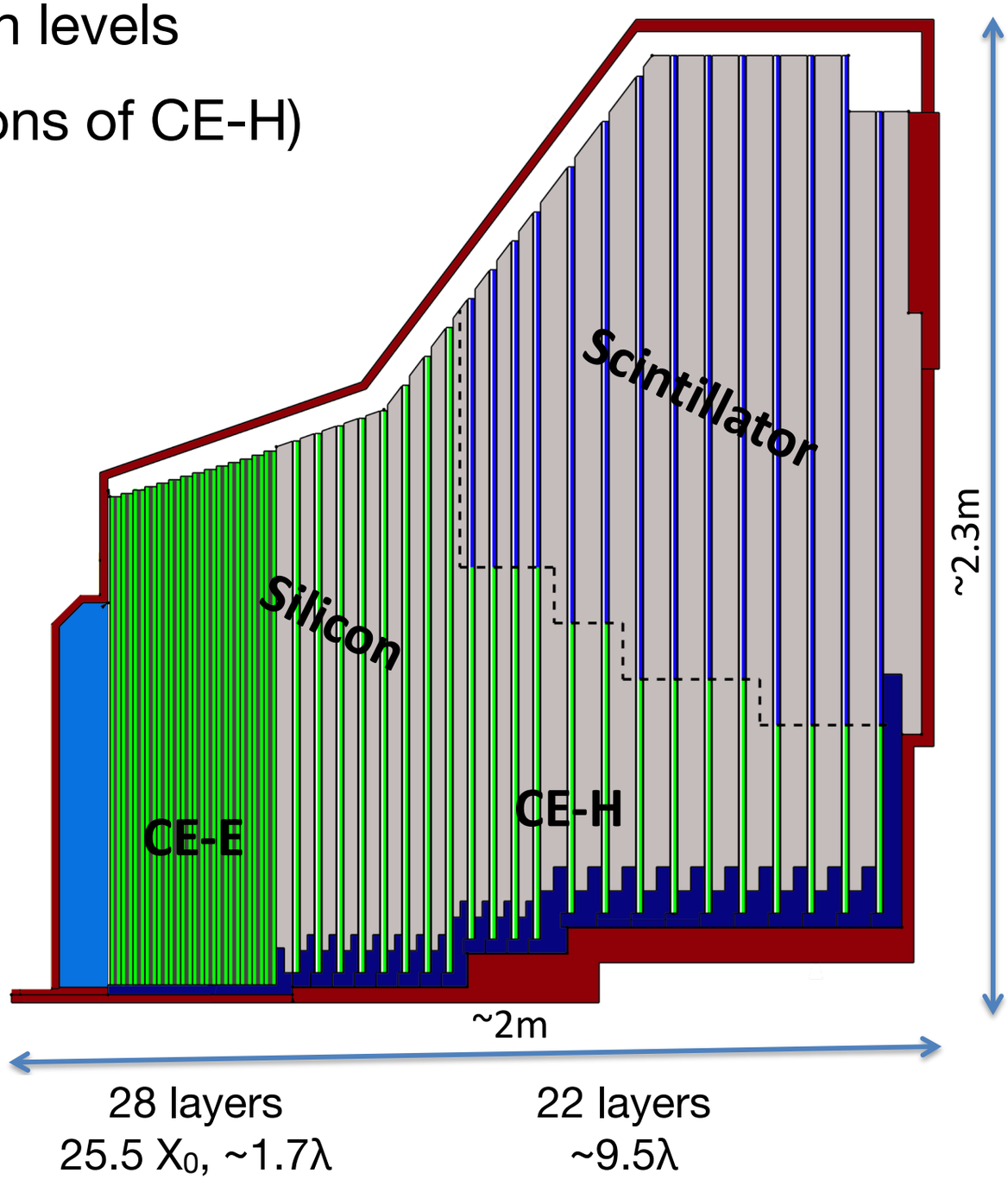
Context and requirements

- The performance of the endcap calorimeter (EC) is crucial for several physics areas:
  - Higgs physics, in particular H→γγ and VBF Higgs production
  - Missing transverse energy resolution at high pileup, for dark-matter searches
  - High granularity for boosted jets, object isolation
  - New capabilities, such as precision timing, for long-lived particle signatures
- Need radiation hard detector material, as well as readout system
  - Fluence up 10^{16} neq/cm^2, dose up to 1.5 MGy
  - Strong dependence on η and z



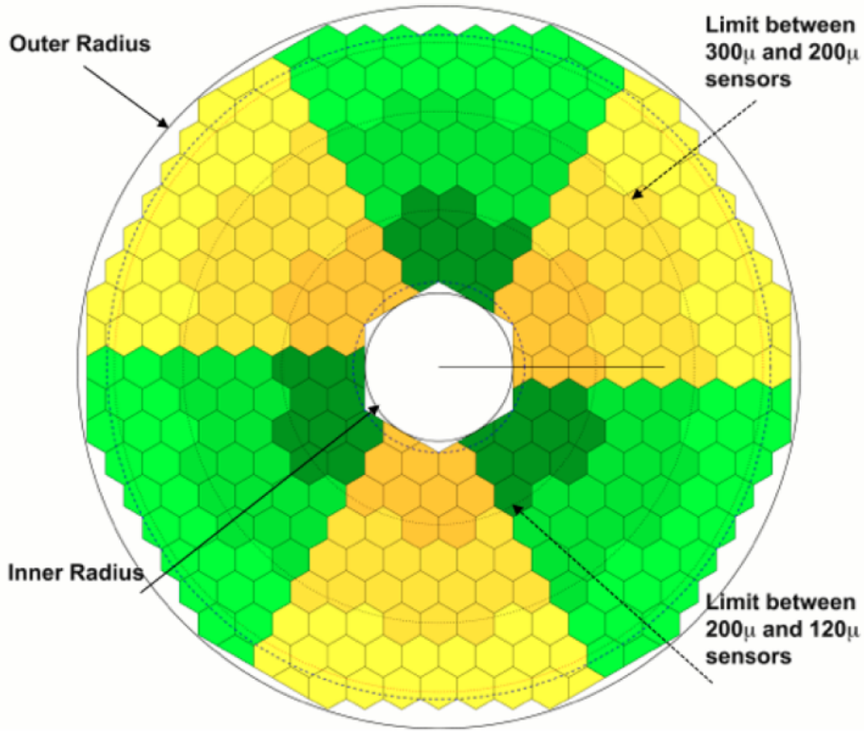
Detector concept

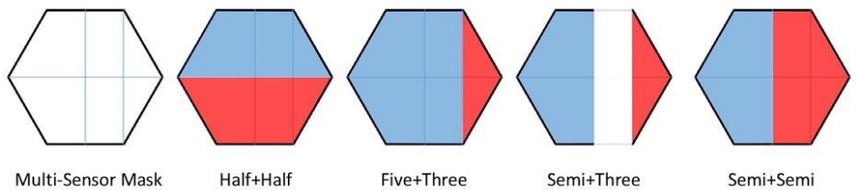
- Integrated ECAL and HCAL, using two types of active material depending on radiation levels
- High radiation zones (CE-E and portions of CE-H)
  - **Silicon** active material
  - EM absorber: lead+tungsten
  - HAD absorber: stainless steel
- Low radiation zones (CE-H)
  - **Scintillator** tile direct readout (**SiPMs**)
- Detector organized into *cassettes* comprised of a Cu cooling plate with multiple Si modules and/or Scint. tile-modules mounted on it
- Dissipated power ~250kW, removed via **CO_2 cooling**, operated at -30°C

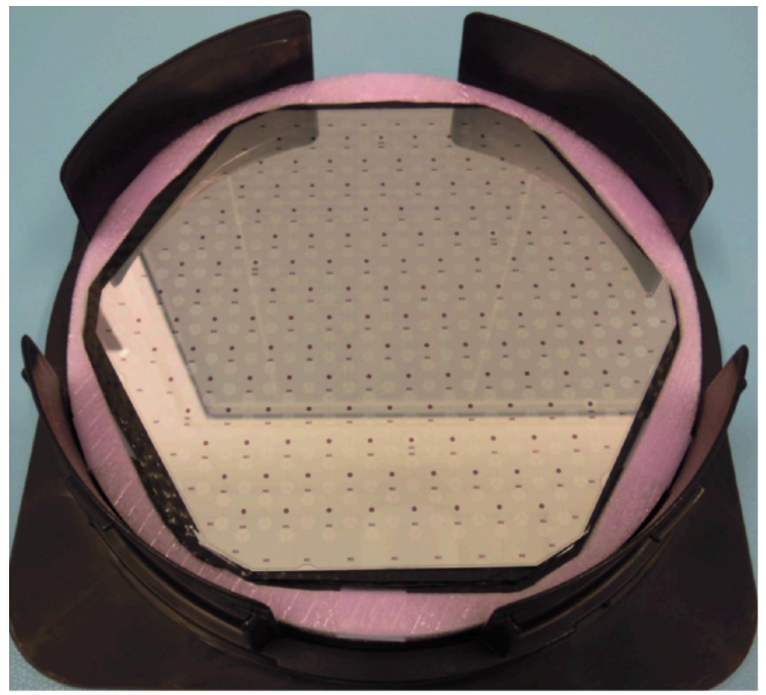


Silicon sensors

- **Hexagonal** sensor geometry to maximize use of circular wafer and aid tiling
- 3 sensor thicknesses (120, 200, 300μm) to accommodate range in fluence
- 2 Pad sizes:
  - 1cm² "Low density" in outer regions
  - 0.5cm² "High density" in the inner region, to equalize load capacitance, reduce leakage current, and improve pattern recognition
- DC coupled, n-on-p sensors to avoid non-Gaussian breakdown noise
- Total of 6M channels across 30k modules
- Also includes multi-geometry sensors to tile inner and outer edges at reasonable cost

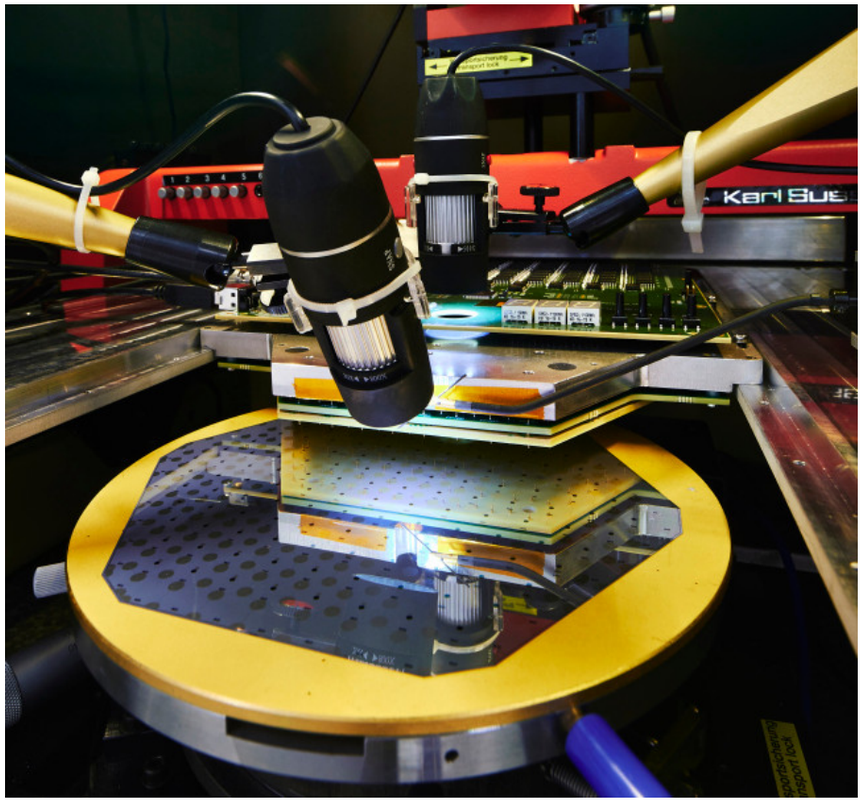






Silicon sensors - status

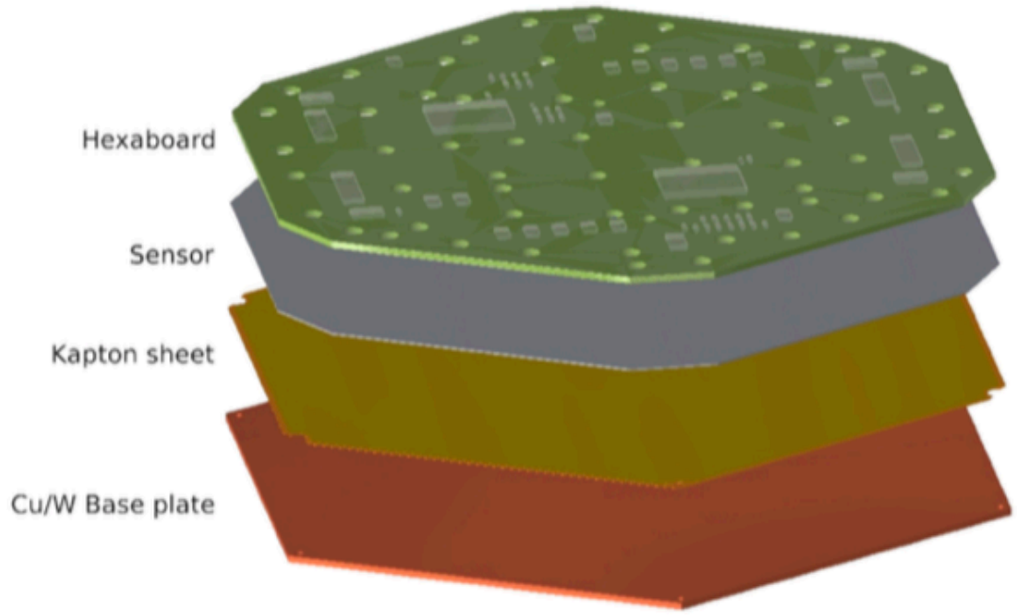
- Initial testing was done with 6” sensors, choice made to use 8” sensors for final system, 2nd round of 8” prototypes have been received recently, and are currently being characterized
- No surprises in radiation testing so far
  - Initial irradiation of full size sensors completed at RINSC
  - Further extensive sensor irradiations this summer
- *Challenge*: backside fragility due to shallow backside implant
  - Reproduced by HPK
  - Design tweaked to minimize impact
  - Possible solution: add kapton layer at HPK, before shipping

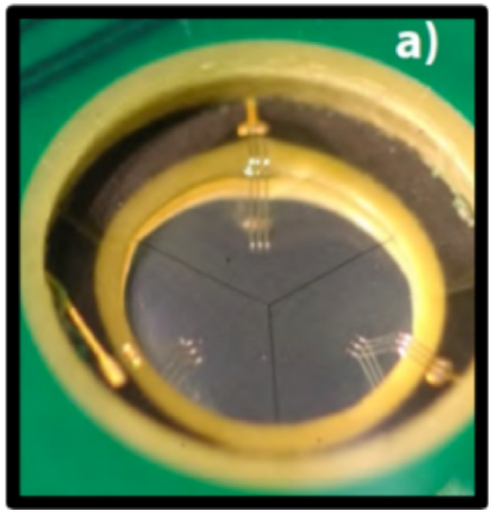


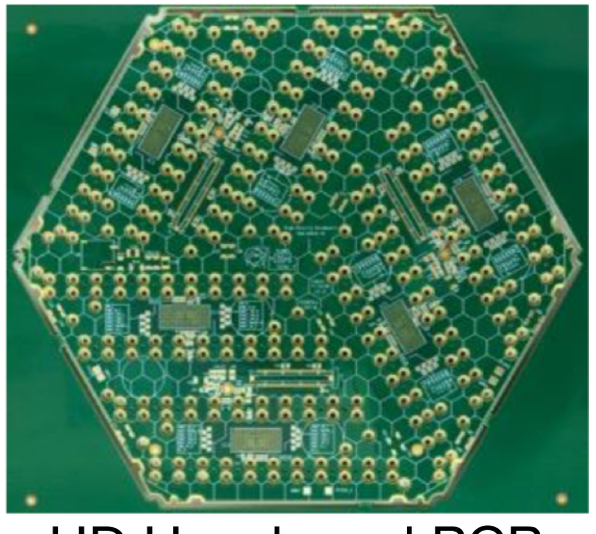
Irradiation at RINSC

Silicon modules

- Silicon modules are a sandwich of:
  - Cu/W base plate
  - Kapton sheet
  - Sensor itself
  - Hexaboard
- Sensors are wirebonded to the hexaboard via holes in the PCB
- Hexaboards contain the HGCROC readout ASIC
  - 3 for LD module
  - 6 for HD module
- Also variety of hexaboards to handle partial modules at the periphery
- Module assembly will be done with automatic gantry at 6 sites



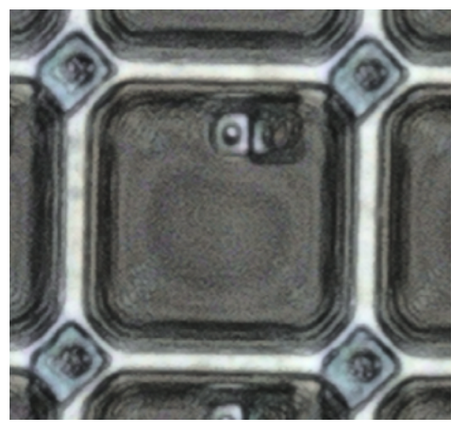




HD Hexaboard PCB

SiPM on (Scintillator) tile

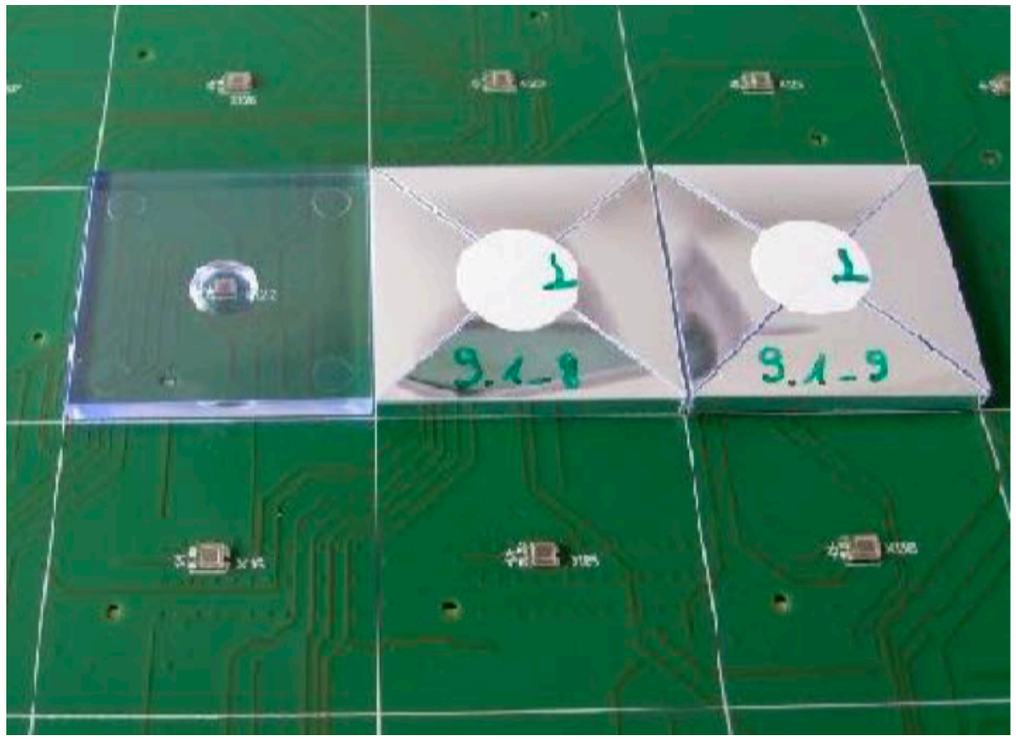
- Cost effective way to instrument full depth of detector (~10λ)
- HL-LHC radiation dose (target up to ~10^{13} neq/cm^2 for CE-H) favors small tiles, resulting in a high granularity detector with applications for particle flow
- High granularity provides the ability to match individual showers with tracker and timing measurements, thus reducing the negative effects of high pileup
- Low-noise photodetectors enable a calibration strategy based on MIP reconstruction.
- CE-H scintillator system 240k channels:
  - Tile sizes: 4–30 cm^2
  - SiPM size 2–4 mm^2
- Size of system requires automation in assembly and testing



Hamamatsu HDR2-15 μm

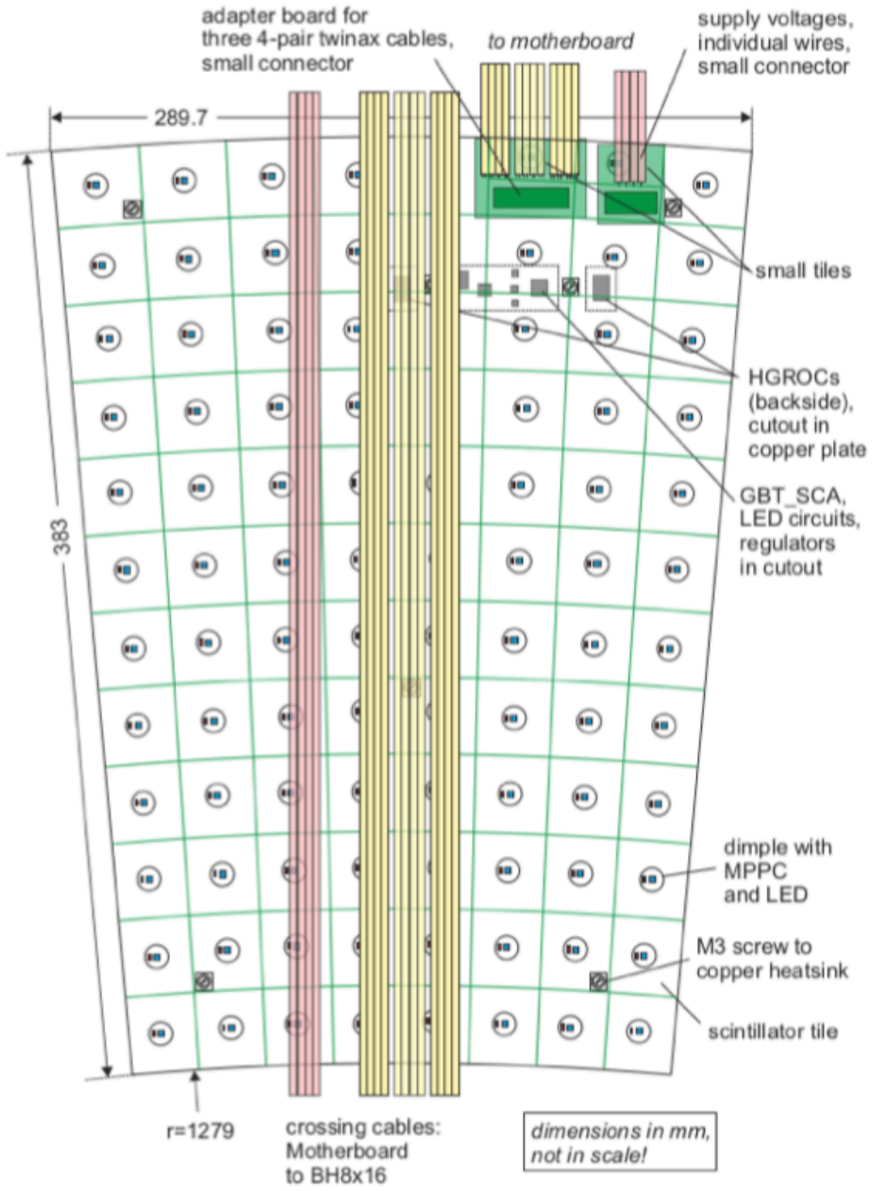
SiPM on (Scintillator) tile

- Scintillation light from tiles directly illuminates the SiPM photodetector underneath. Dimple in tile equalizes response across tile.
  - Will use both cast & molded tiles
- Reflective wrapping (ESR) maximizes light reaching the SiPM.
- Detector inside cold volume to limit SiPM noise after irradiation.



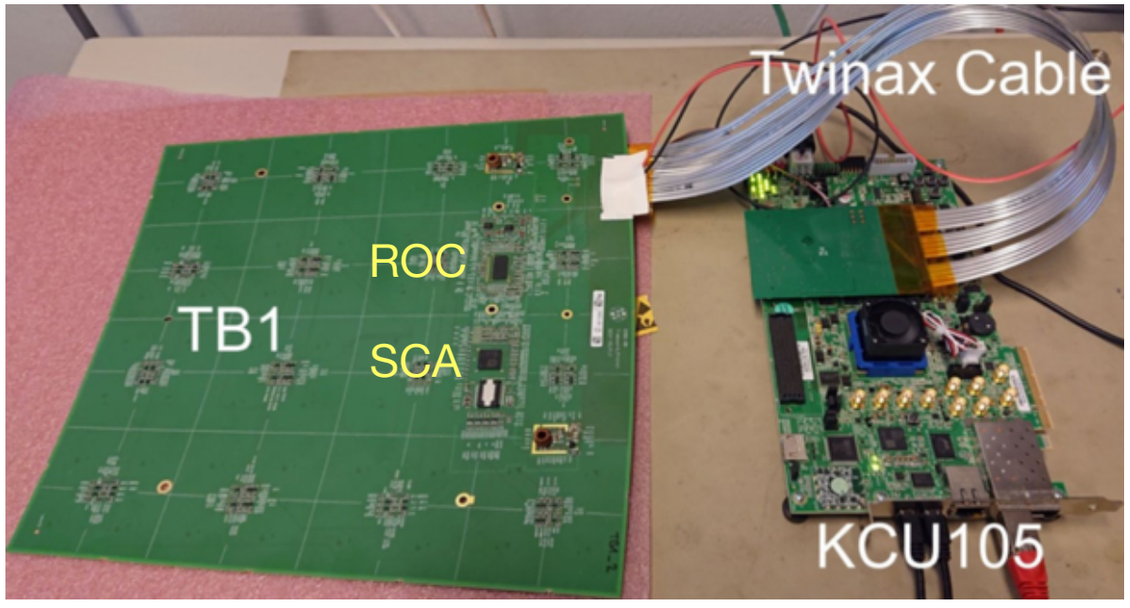
- Smaller tiles result in more light reaching the SiPM. Tile sizes chosen to maintain a good S/N for MIP calibration until end of life.
  → Smaller tiles and larger SiPMs used to maximize light collected in the most radiation-damaged areas.
- Building on expertise from CALICE

Tile modules



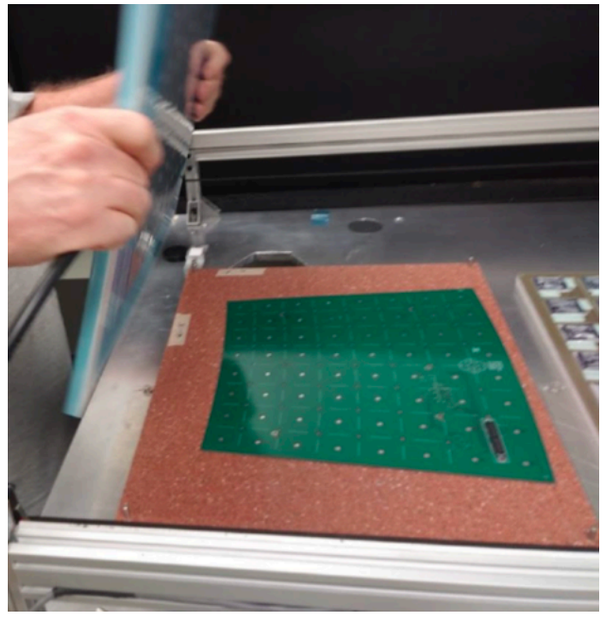
- Active area covered by fan-shaped tile modules that host the SiPM photodetectors and the HGCROC readout chips plus associated controls
- Per-channel LED system for commissioning and monitoring
- Complexity minimized by using standardized list of module types to cover all layers
- First prototype produced, and under test

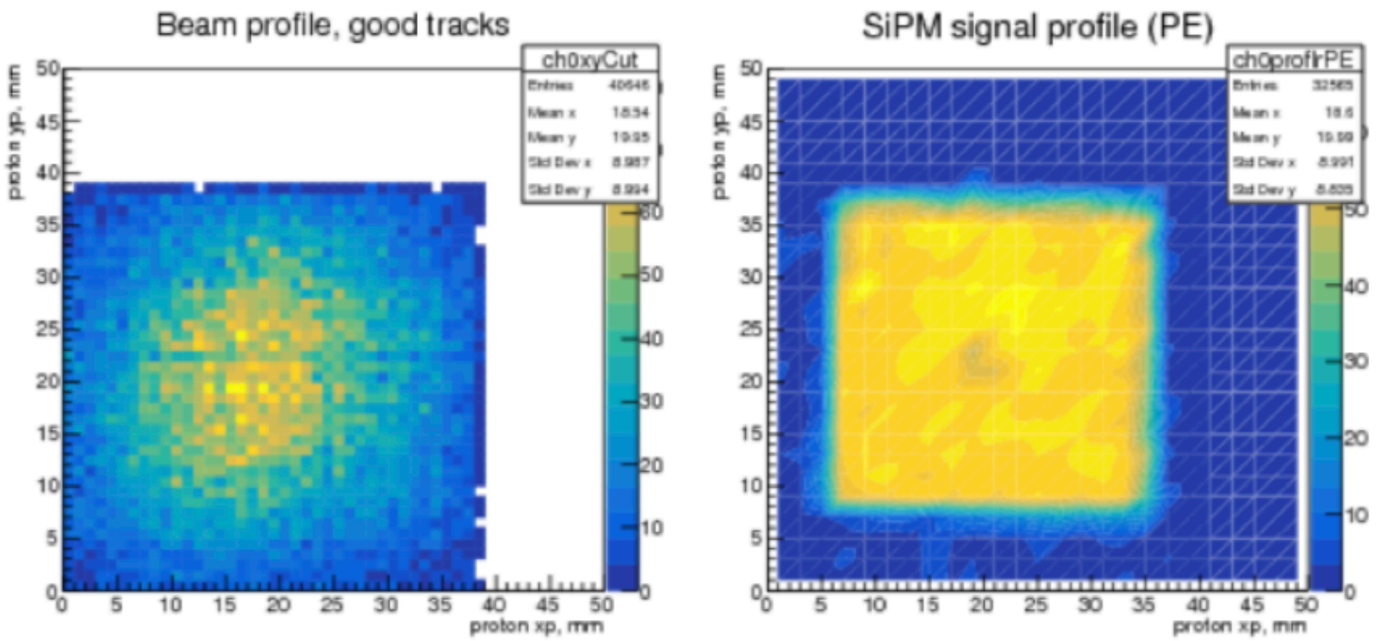
Prototype Tile Board



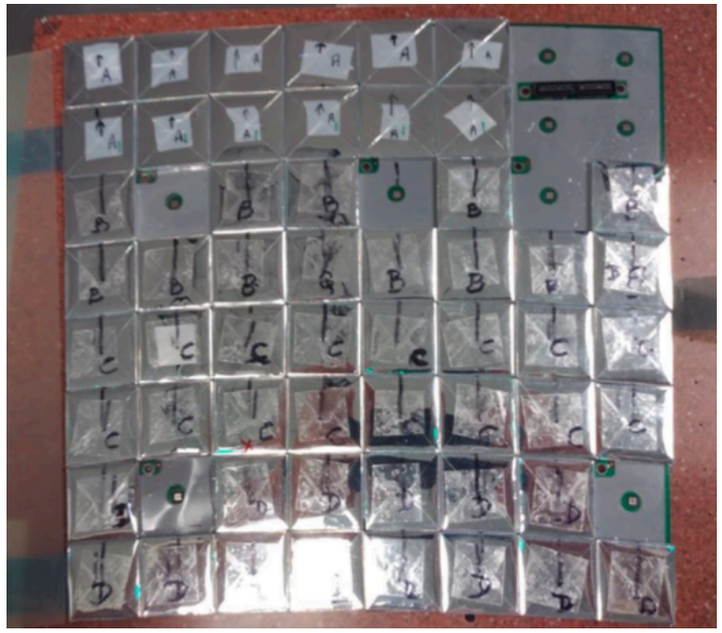
SiPM-on-tile status

- Completed FNAL beam tests in early 2020 with 120 GeV proton beam for scintillator tile studies
- Demonstrated automated tile wrapping and punching of wrappers
- SiPM irradiation campaign ongoing; In line with expectations so far





Test beam results for scintillator tile uniformity, and light yield for various materials



Placing wrapped tiles via pick-and-place machine

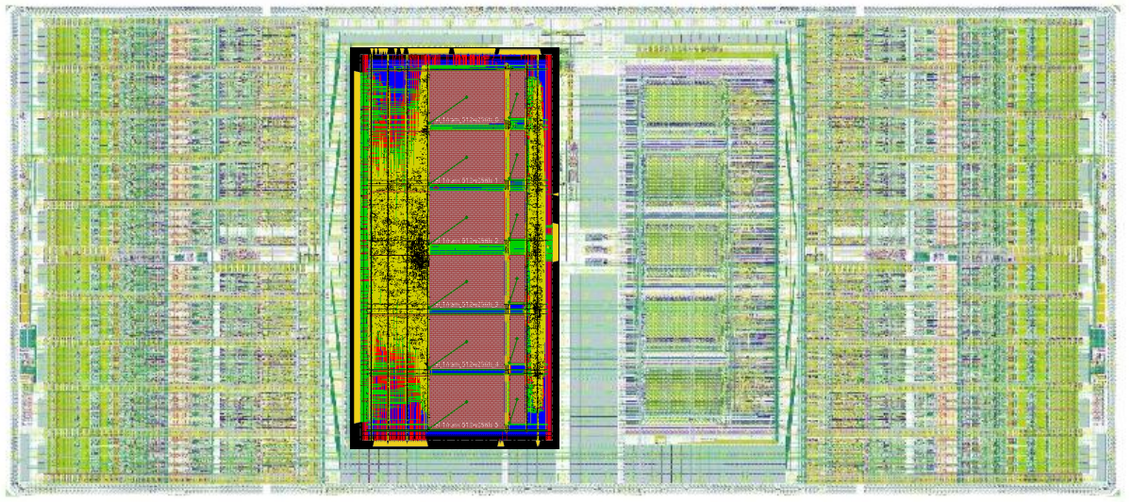
On-detector electronics

- **General principle of data readout:**
  - Digitize signal from Si Sensor/SiPM using readout ASIC (HGCROC)
  - Concentrate data using ECON ASICs to reduce bandwidth
    - 40 MHz trigger data: ECON-T aggregates, selects, compresses, serializes, and transmits to lpGBT
    - 750kHz DAQ data: On L1 accept, ECON-D applies zero suppression, aggregates, serializes, and transmits to lpGBT
  - Send data to off-detector electronics via lpGBT/VTRX+
- Control path:
  - Fast control from counting room to HGCROC/ECON via lpGBT
  - Slow control of front-end chips via GBT-SCA (through lpGBT)
- **Important constraints:**
  - Very limited physical space
  - Radiation tolerance of ASICs, optical transmitters, DC/DCs

HGCROC

- Analog
  - 72 active channels (+2 for calibration, +4 for Common Mode)
  - *Dynamic Range* ~0.2fC to 10pC; Linearity <1%
    - From single MIP to TeV showers
- Energy Measurement:
  - ADC 10-bit SAR, range 0—100fC
  - TOT range 100fC—10pC, bin size 2.5fC
- TOA: 10-bit TDC, LSB <25ps, 25ns full range
- Slow Control
  - Programmable registers
  - I2C protocol
  - Connected to SCA
- 2 HGCROC versions with different preamps optimized for Si & SiPM readout
- Sequence of prototypes, currently testing HGCROC “V2”, and designing “V3”

- Communication:
  - 320MHz clock
  - Reception of fast commands from lpGBT
- Data Readout Path
  - latency up to 12.5μs
  - 2 outputs @ 1.28Gbps
- Trigger readout Path
  - Trigger primitives
  - max latency of 36bx
  - 4 outputs @ 1.28Gbps



HGCROC V3

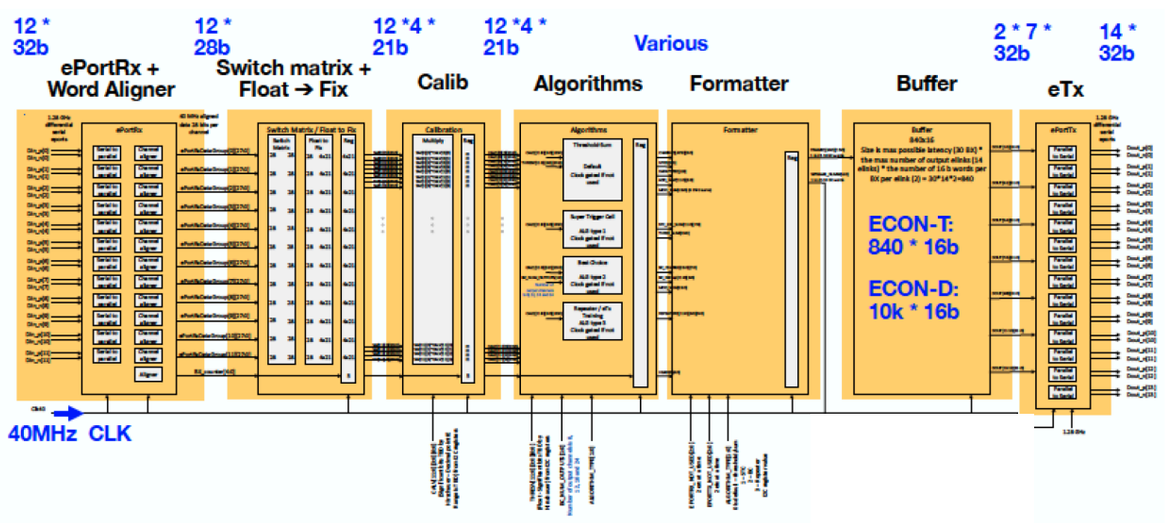
ECON

Concentrator ASIC, comes in two types: ECON-T and ECON-D

- Both have 12 inputs and 14 outputs @1.28 Gbps
- ECON-T: Select & compress interesting HGCROC trigger data for transmission off detector for every bunch crossing (40MHz)
  - Implemented 3 algorithms: (1) variable format algorithm that transmits all TC exceeding a programmable threshold per BX; (2) fixed format, “Super Trigger Cell”; (3) fixed format “Best Choice”
- ECON-D: Receive HGCROC data packets. Perform 0-suppression and concentration of data up to L1 trigger rates of 750kHz

Basic system idea: use 1 ECON-T and 1 ECON-D per 8” module

First prototype to be submitted this Fall



Si Motherboards

Readout electronics in the Si region are hosted on “motherboards”, which are implemented as a modular system

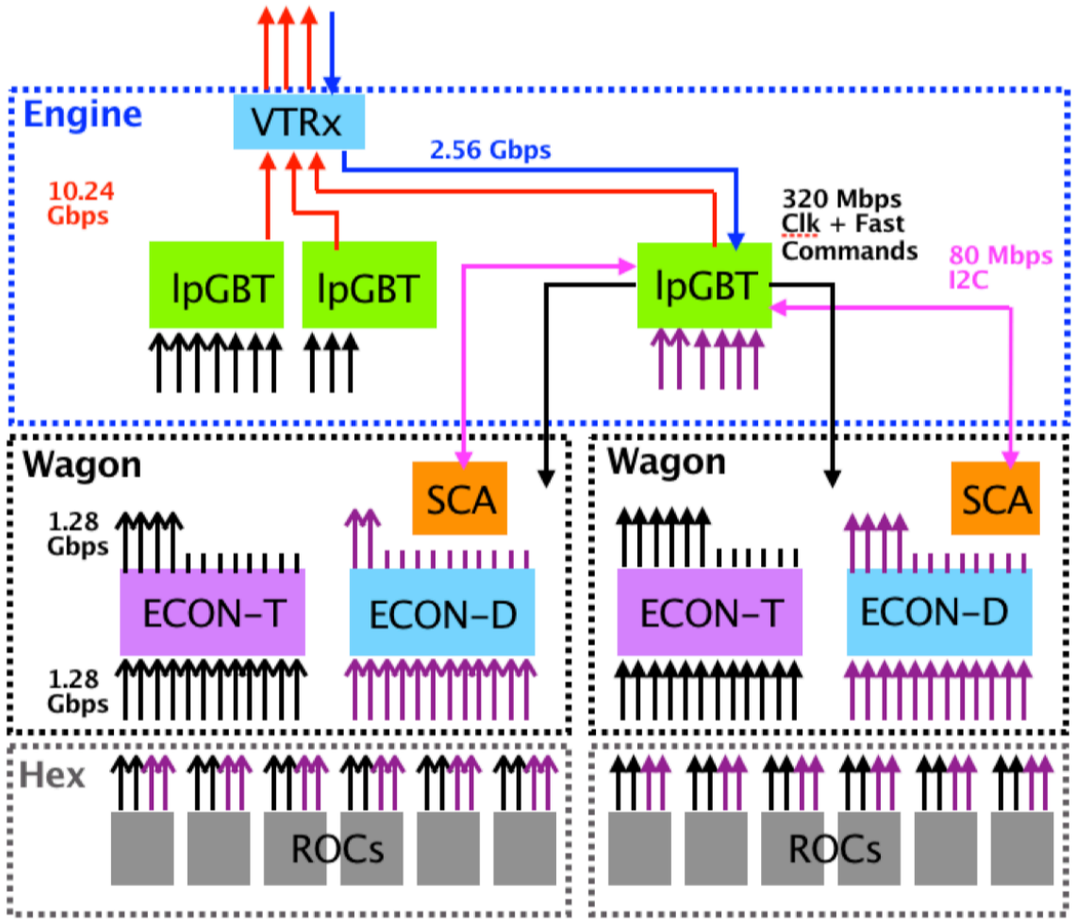
Low density:

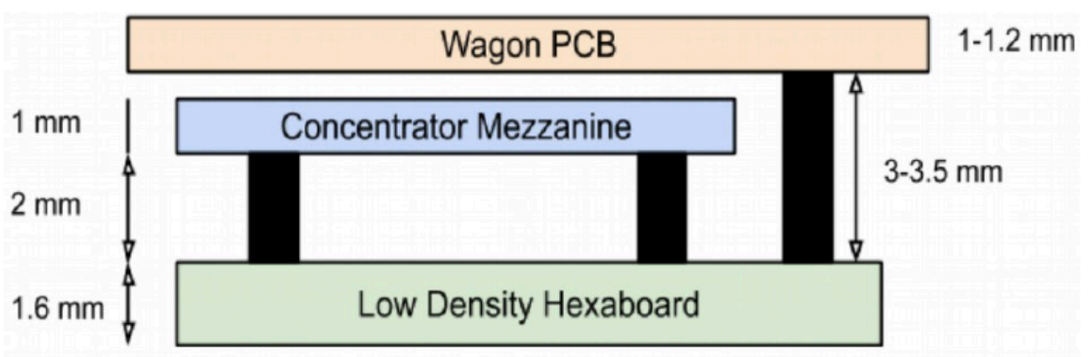
- Engine, with lpGBT and VTRX+
- Wagons, connecting the engine with up to 3 Si modules
- Concentrator mezzanine that hosts the ECONs (1/module)

High density:

- Engine, with ~twice as many lpGBT and VTRX+
- Wagons with ECONs integrated

System is geometrically complex, many wagon varieties are needed

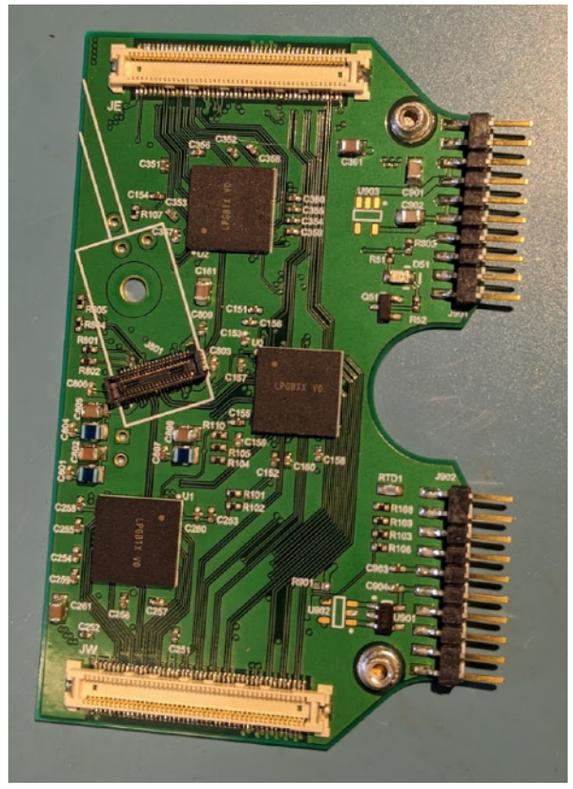


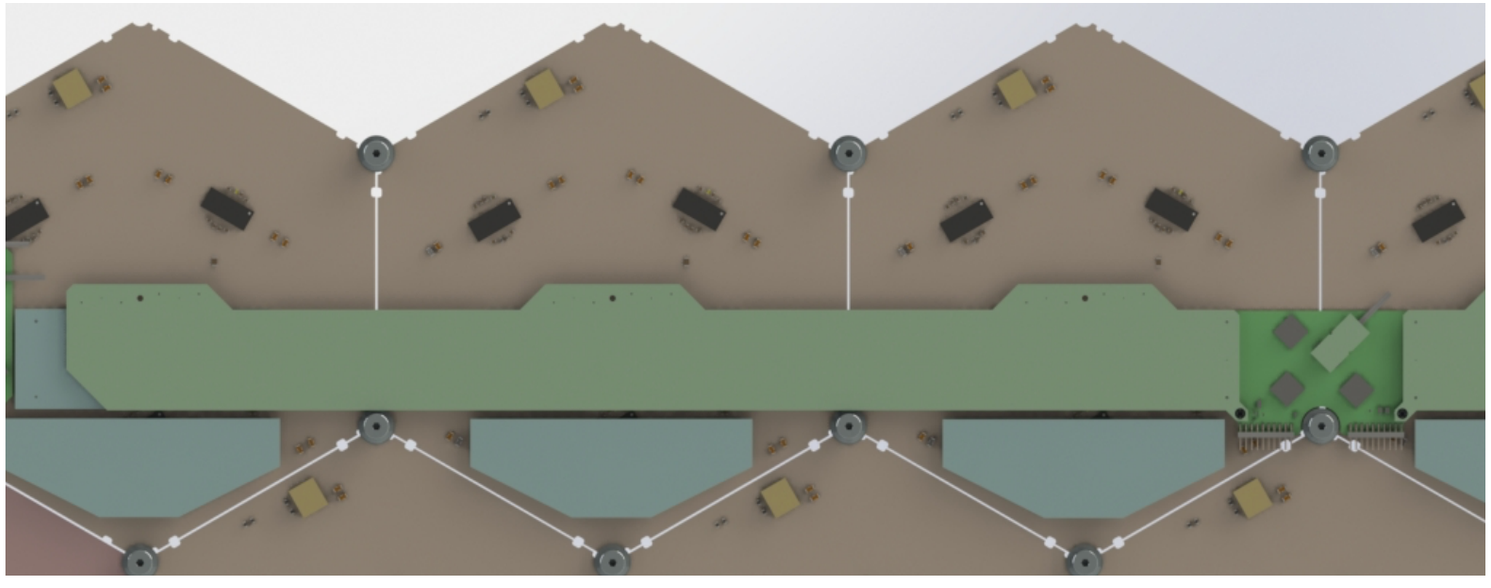


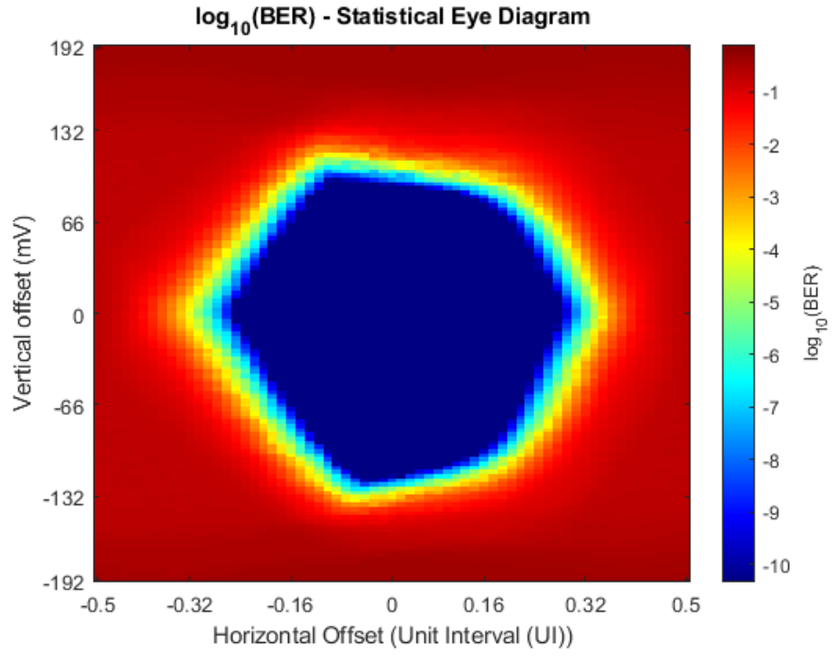
Si Motherboard status

- Two Engine prototypes produced
  - Engine V1 successfully tested
    - 10 Gbps uplink, 2.56Gbps downlink, I2C communication between lpGBTs
  - Engine V2 initial checkout positive
- Designs for two wagons (straight, 3 and 2 modules long) have been completed

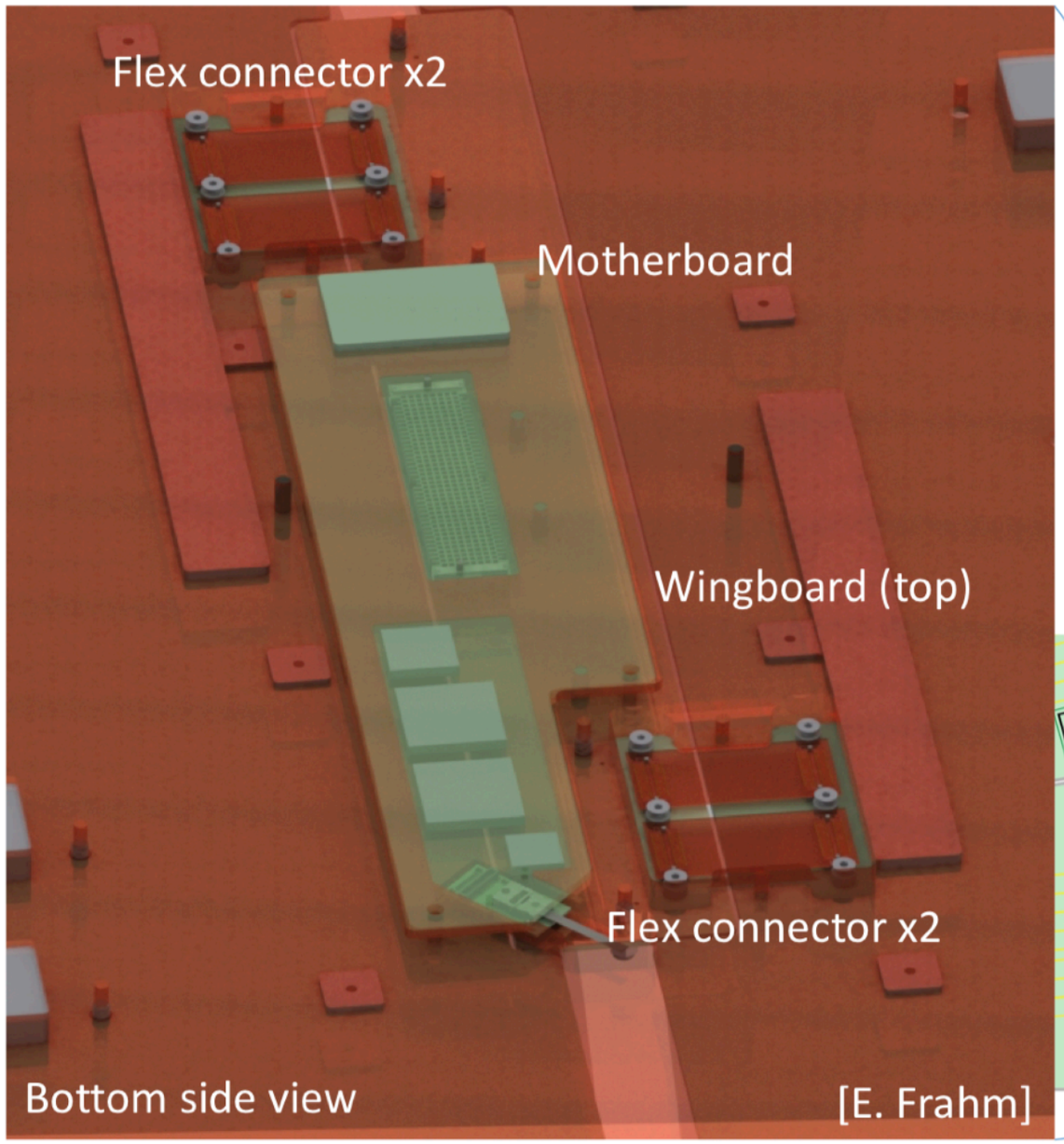
Engine V2



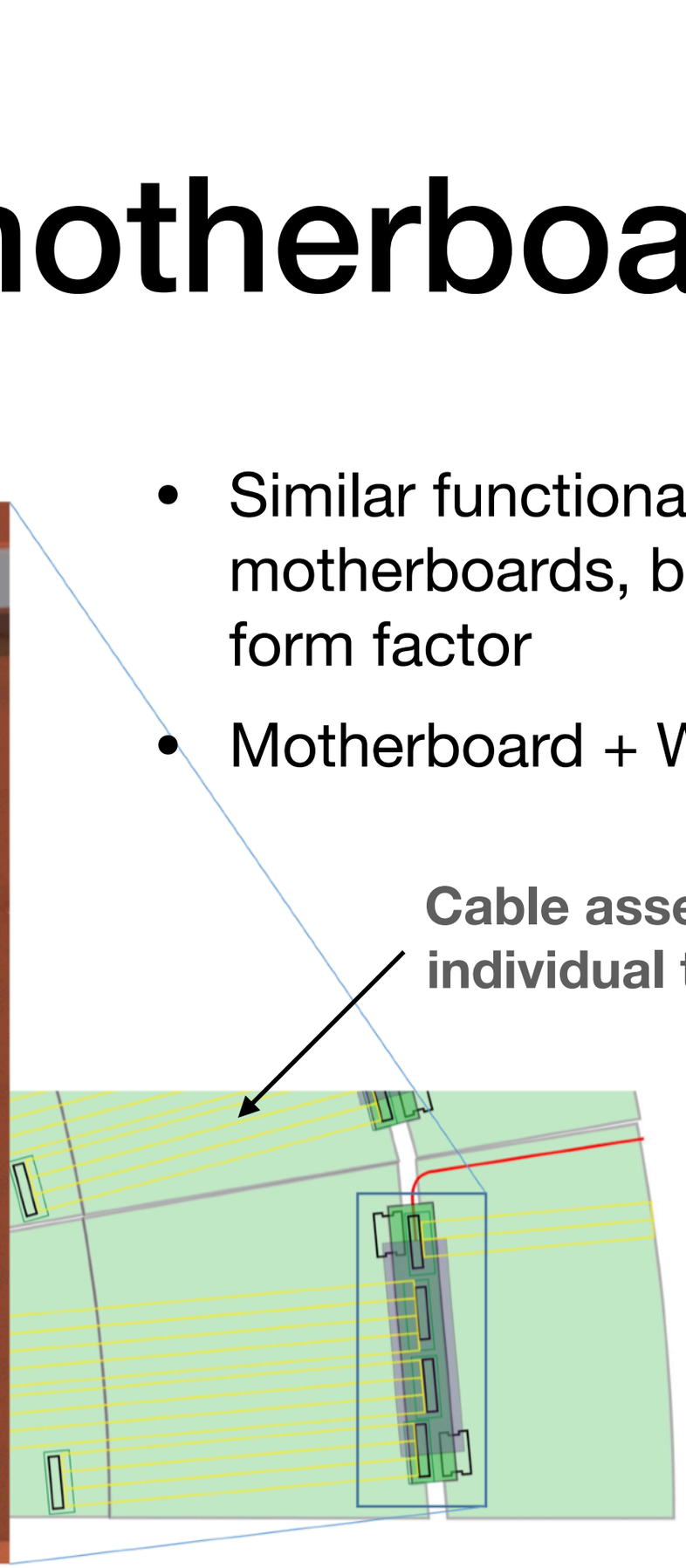




Scintillator motherboards



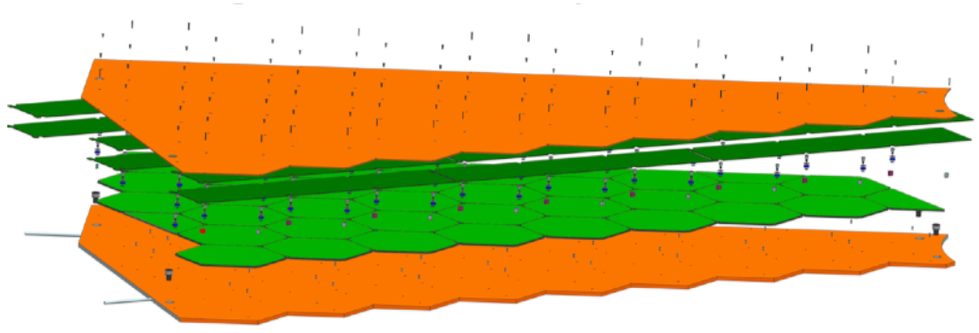
- Similar functionality as for Si motherboards, but different form factor
- Motherboard + Wingboard

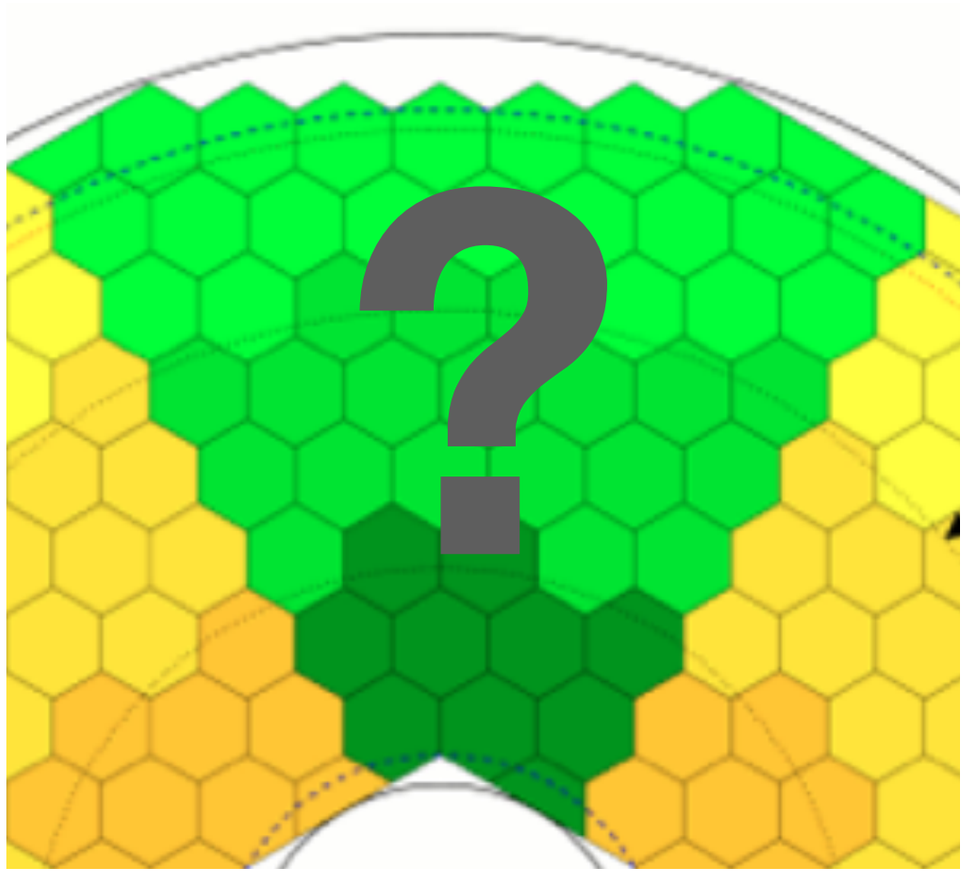


System Integration

Quite a challenging task, especially for the Silicon region

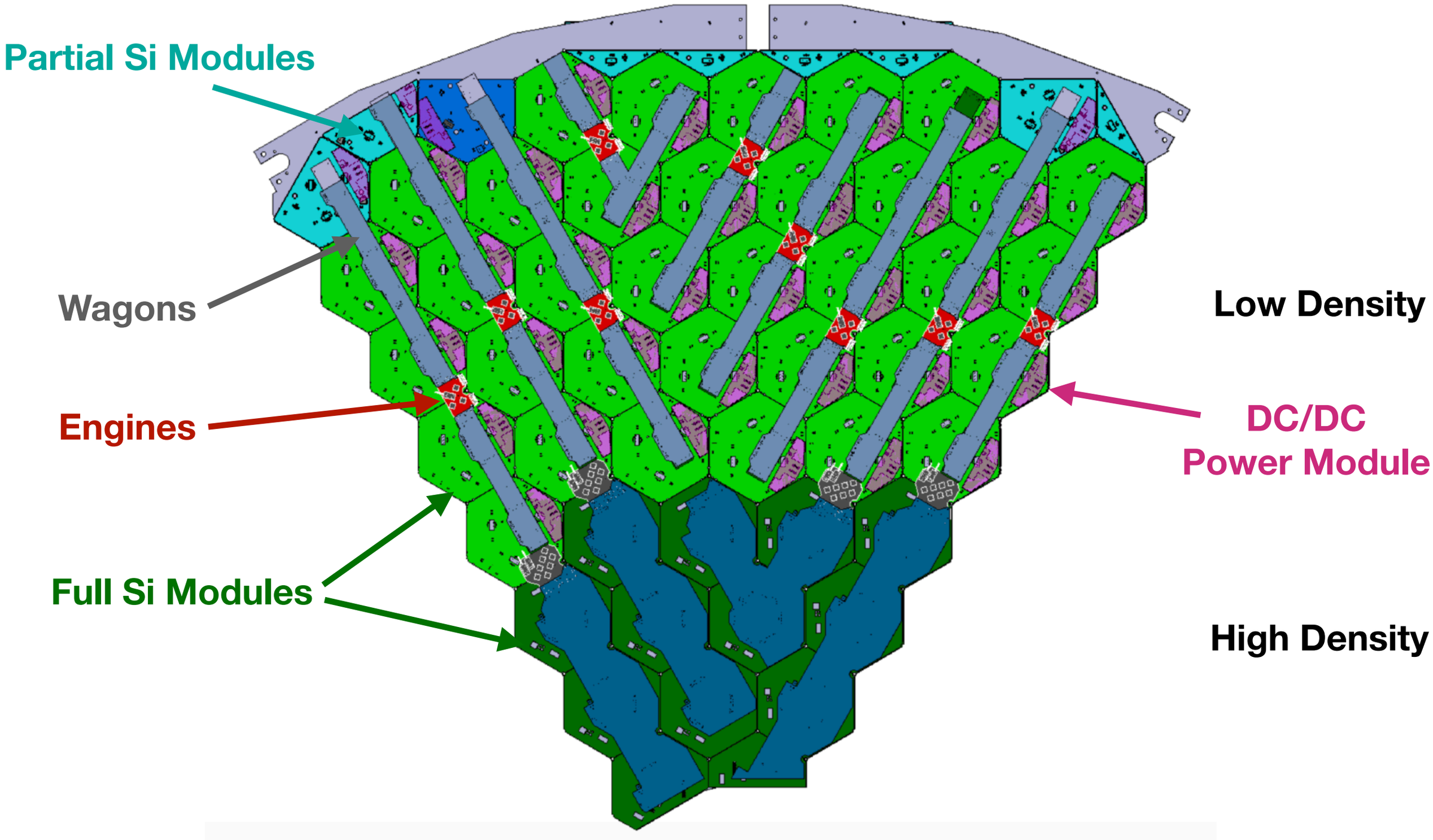
- Nearly every layer is different!
- Hexagonal layout, 60 (CE-E) or 30 (CE-H) degree wedges
- Very limited vertical space (only 5mm clearance above module)
- All signals, as well as LV/BV, have to enter and exit at the outer edge
- DC/DC converters are on-detector, and must fit somewhere
- Need to respect LD vs HD split
- Cannot place VTRX+ nor bpol12V at the very inner edge (radiation tolerance)





All Silicon Cassette

Ongoing integration effort

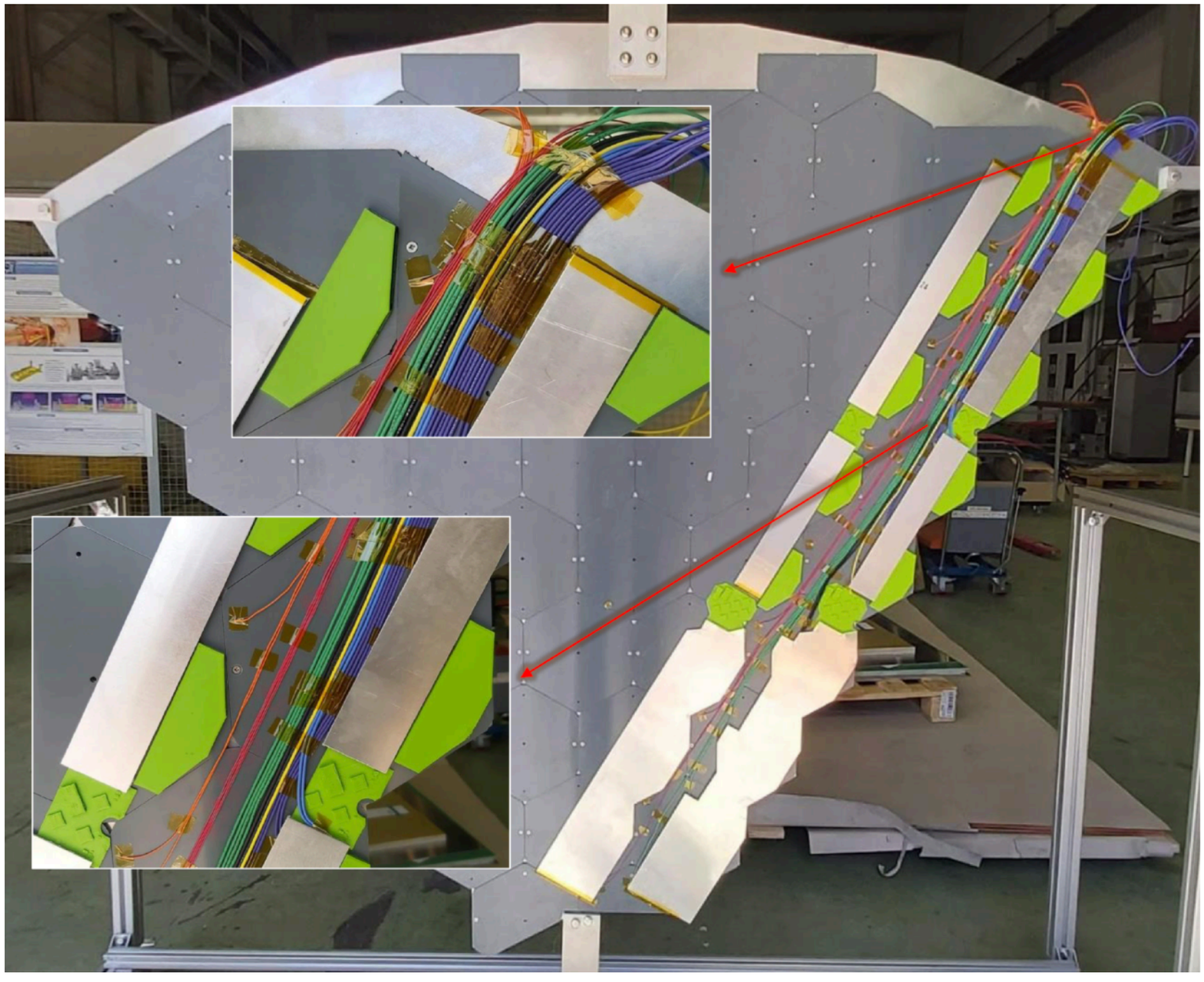


The services challenge

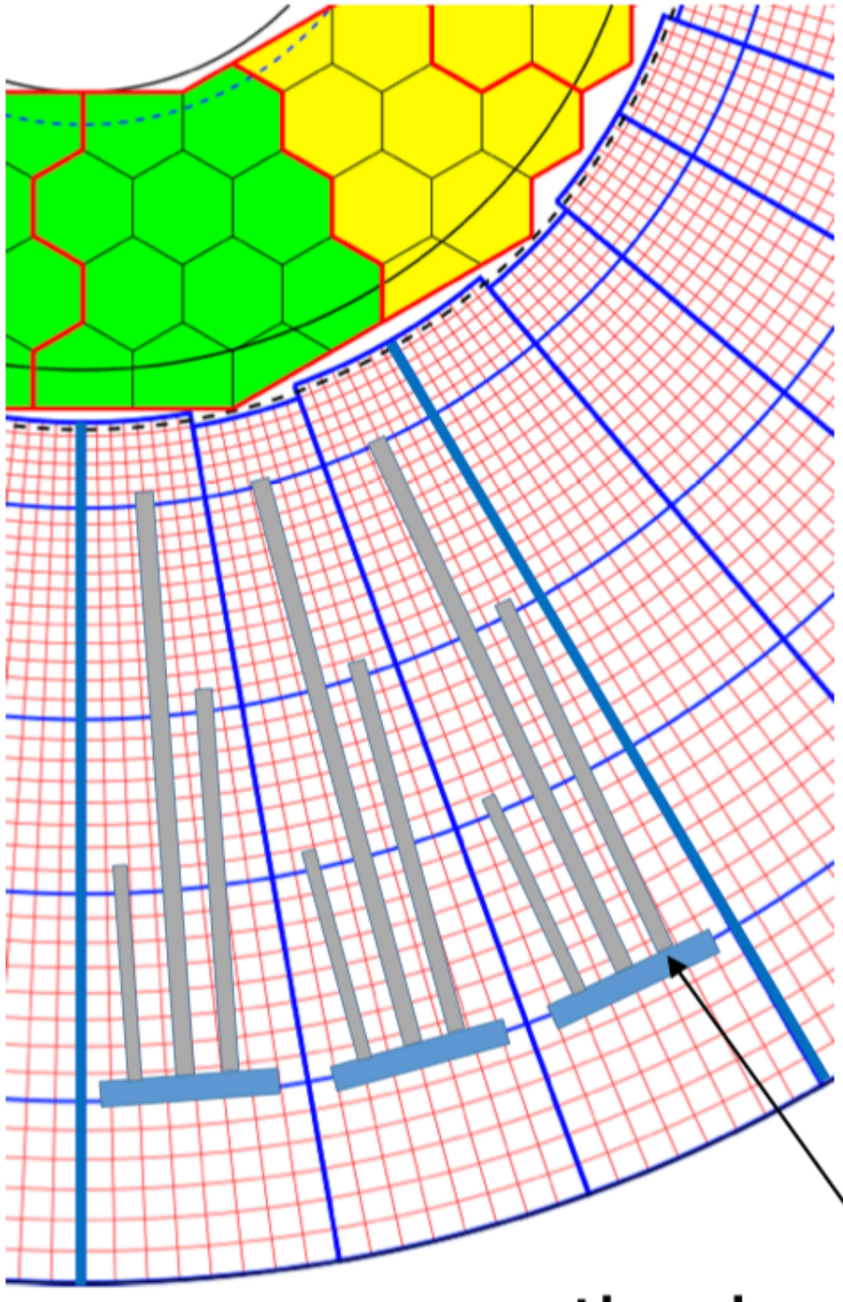
Engines and wagons need to leave enough space available for services routing.

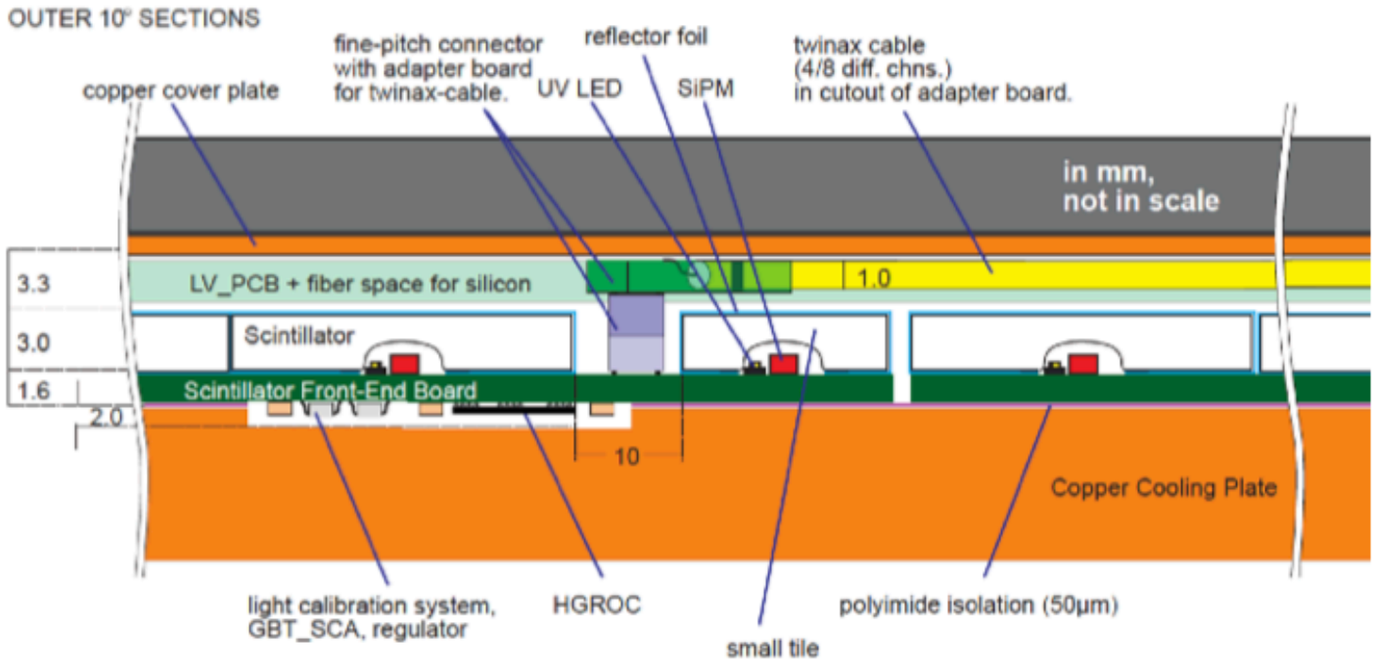
This includes LV, BV, ground, optical fibers, dry gas tube.

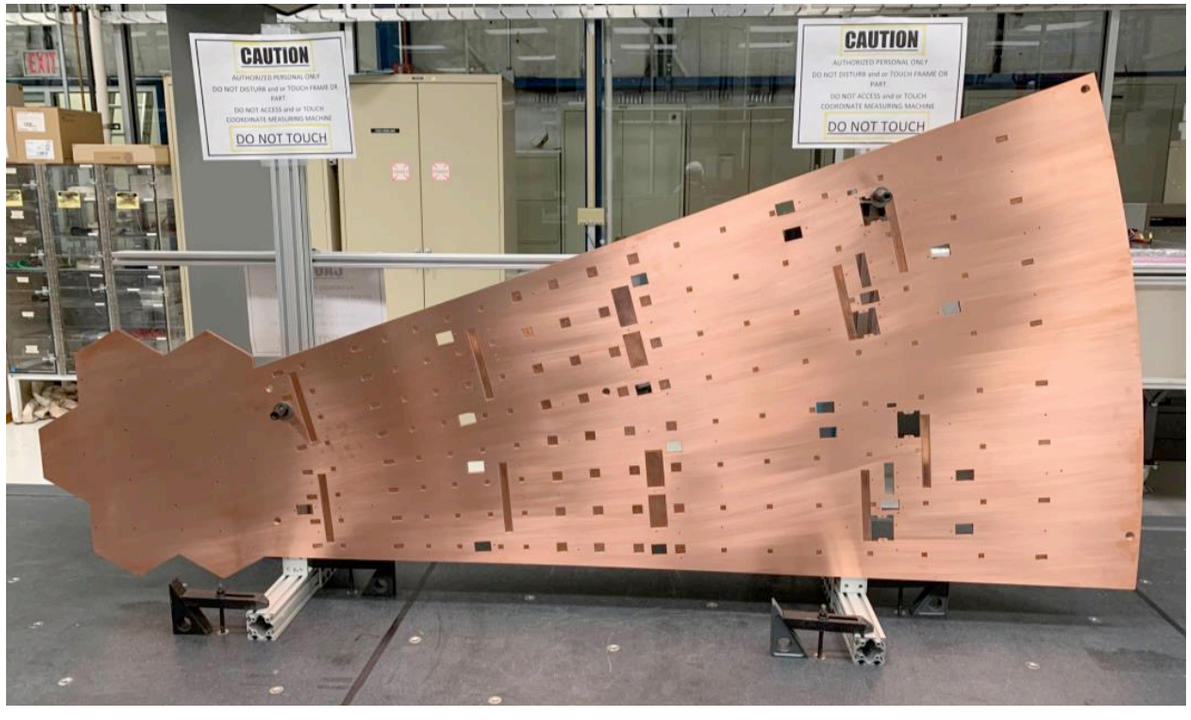
Limited vertical space means that you cannot run over/under most components, e.g. DC/DC coil fills full height budget



Mixed Si/Scint Cassette







Precision timing capabilities

HL-LHC has extremely busy interaction region, ~140-200 pileup

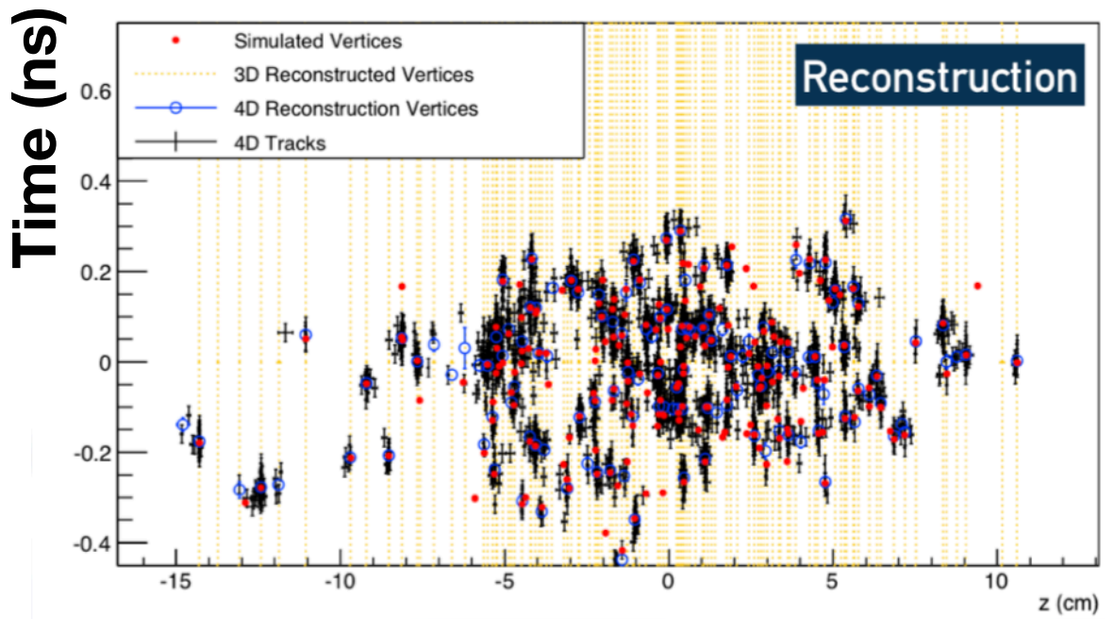
But, vertices are spread in position and time!

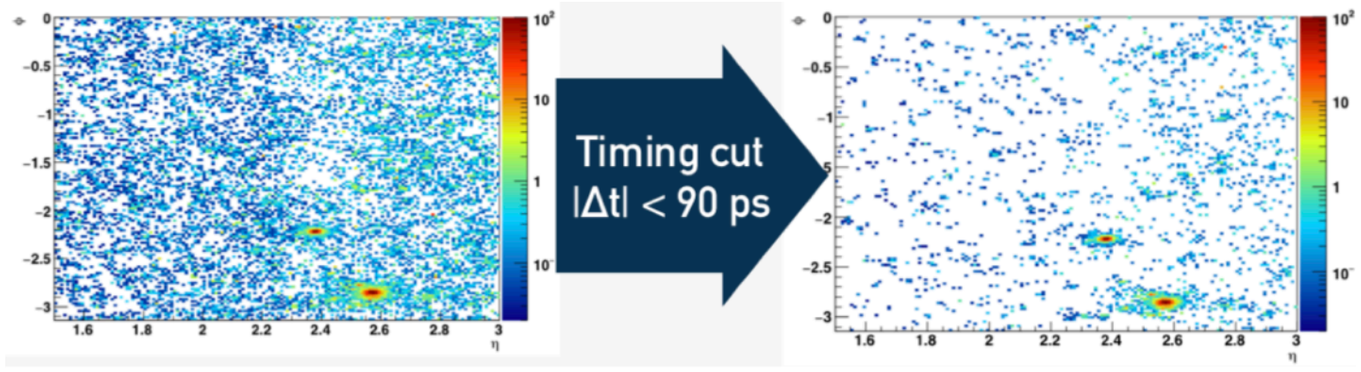
- z: ±50 mm, t: ±150 ps

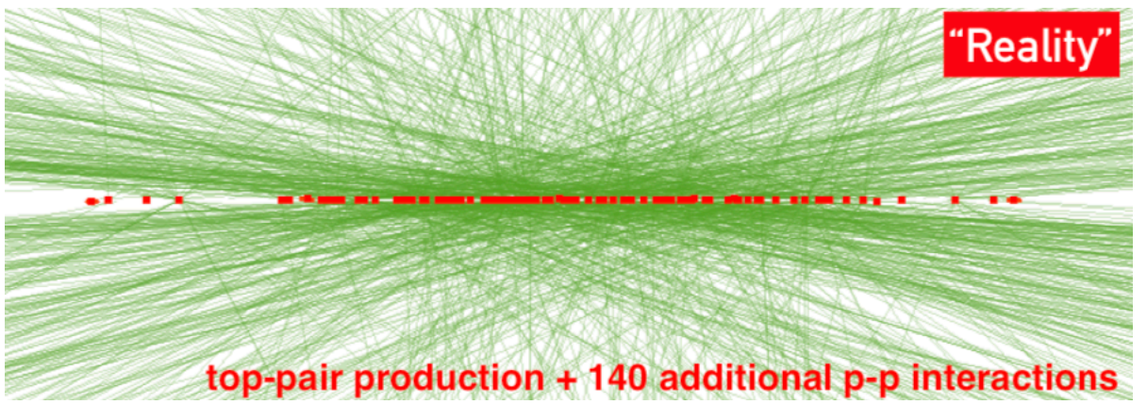
HGCAL is designed to allow for pileup suppression in this environment

- <30ps timing resolution for clusters with p_T > 5 GeV
- Cell sizes 0.5-30cm²

Enabled by TOA in HGCROC (<25ps), low-jitter clock (<15ps)



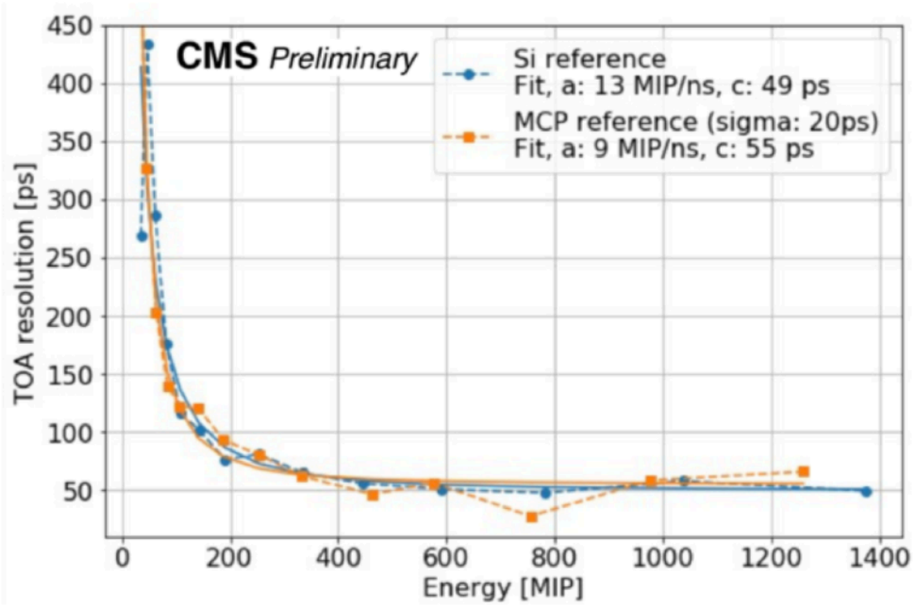




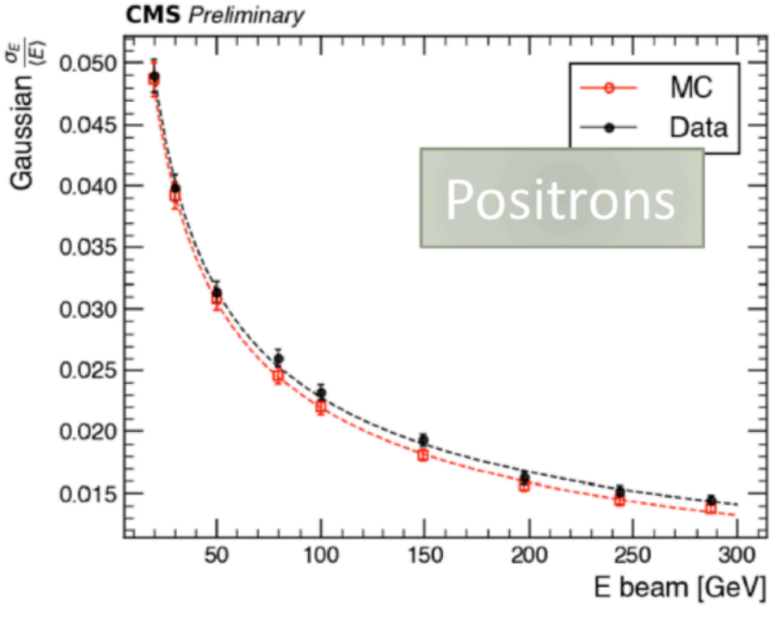
Test beam program

- Several test beam campaigns before LS2, most recently in 2018
  - Measurements of energy and timing resolution
  - Latest test beam analysis included improvements of the ToA calibration and time walk corrections for the timing analysis. Results to appear soon

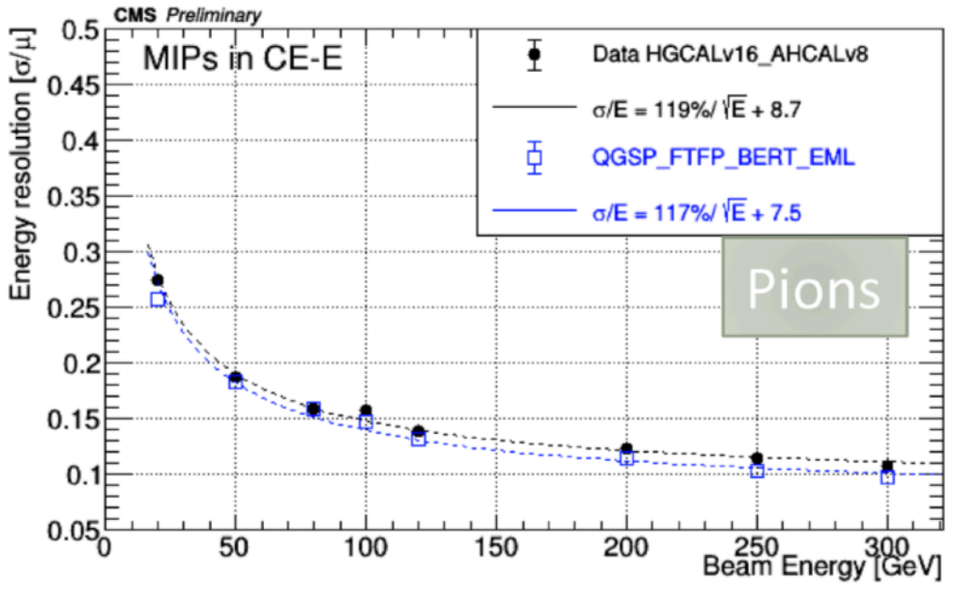
time resolution for a single cell



energy resolution for EM showers

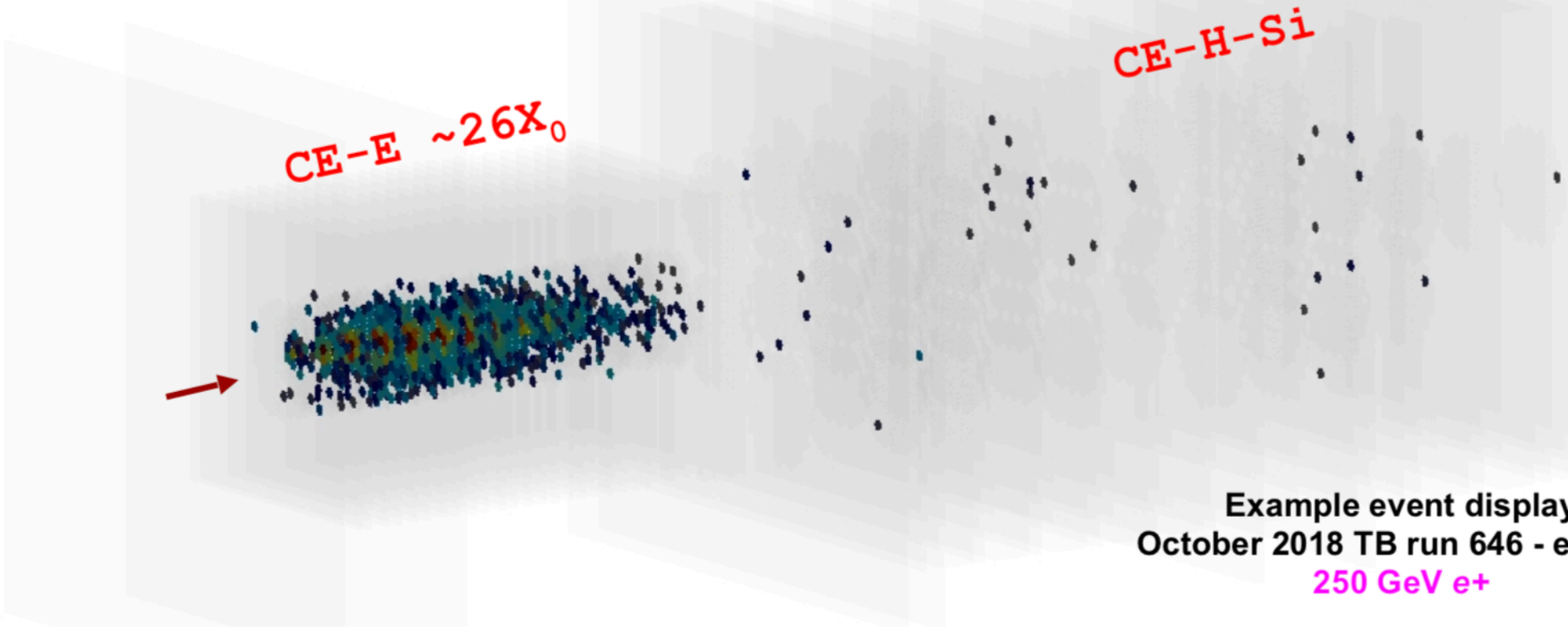


Energy resolution for pions (for showers starting in CE-E)



Example test beam event displays

250 GeV positron



Example event display
October 2018 TB run 646 - event 2
250 GeV e+

Summary

- CMS HGCAL project is on track to be installed ahead of HL-LHC
  - Integrated ECAL + HCAL, using two detector technologies: Silicon sensors + SiPM-on-Scintillator tile
  - Highly granular, with precision timing capabilities, making it a 5D imaging calorimeter
- Radiation environment at the HL-LHC is a challenge
  - Not just for the active material, but also for the on-detector electronics, e.g. ASICs, and in particular optoelectronics and DC/DC converters
  - Large number of channels (and associated high bandwidth) is a challenge for the integration of the overall project
- Fine granularity also brings in new opportunities
  - PF calorimetry, use of advanced machine learning techniques
  - Combined with precision timing allows for new sensitivity to longlived particles