Towards Future Silicon Pixel Detector Readout Chips

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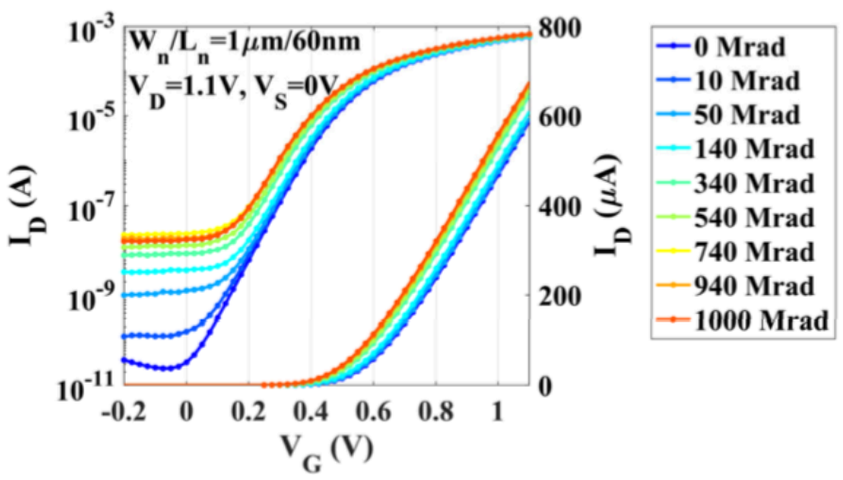
Challenges

- Current state of the art RD53B: 153,600 x 50um by 50um pixels, 5.12Gbps bandwidth, serial powering, 500 Mrad radiation tolerance, 4MHz/1MHz (two level) triggering
- Looking at requirements for future colliders (beyond HL-LHC), need:
  - Higher radiation tolerance (specifically for hadron colliders)
  - High pixel density and by that higher bandwidth
  - Faster trigger (also increasing bandwidth requirement)
    - Major issue: low mass high speed data transmission
  - Larger latency, requiring more memory
  - Smarter trigger (prioritized trigger) to offset bandwidth requirement
  - High timing precision (O(100ps) or less is useful)
- Requirements clearly require us to use smaller and more modern CMOS technologies

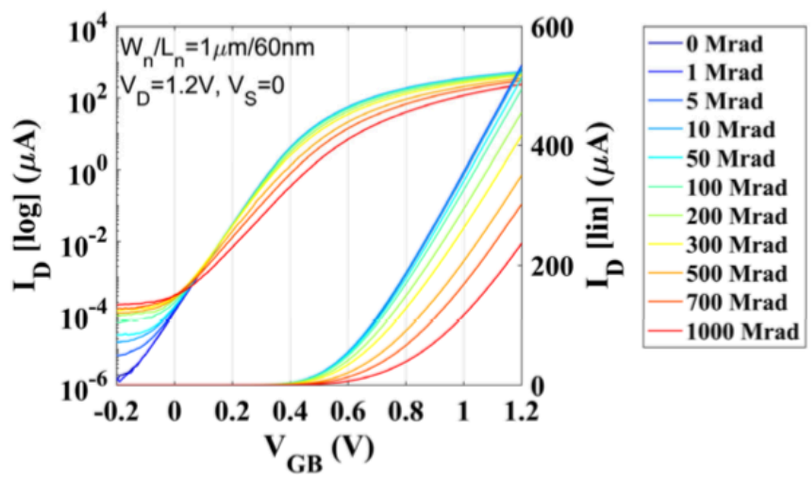
Foundry Access and Radiation Tolerance

- Access to sub-130nm technology very complicated, prevents us from quickly screening large variety of technologies in terms of radiation tolerance
- Luckily radiation tolerance seems to be getting better the smaller the technology
- 28nm was explored after 65nm and looks suitable for the next generation of readout chips

- 1µm/60nm from TSMC 28 nm bulk CMOS



- 1µm/60nm from TSMC 65 nm bulk CMOS



1µm/60nm	$V_{DS}=V_{DD}$	V_T Var.	SubS Var.	I_{off} ($V_{GB}=0$)	I_{on} Var. ($V_{GB}=V_{DD}$)
28nm	1.1 V	–13%	15%	537x	+15%
65nm(ref)	1.2 V	+39%	47%	10x	–55%

https://indico.cern.ch/event/681247/contributions/2926579/attachments/1638607/2615422/Enz_ACES_TID_effects_28nm_bulk_CMOS_cenz.pdf

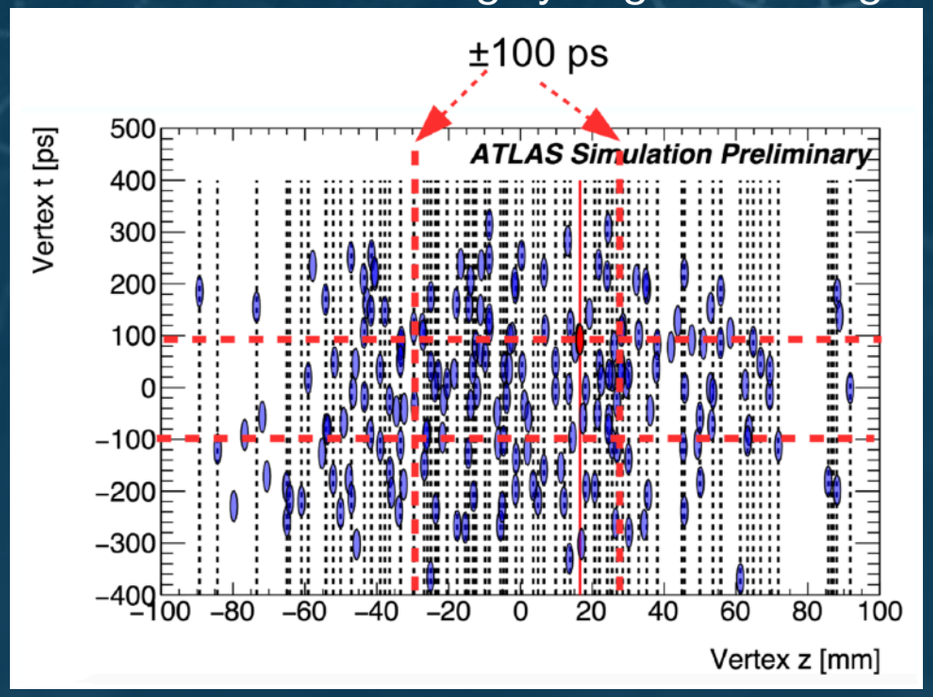
28nm Prototyping Plans at LBNL

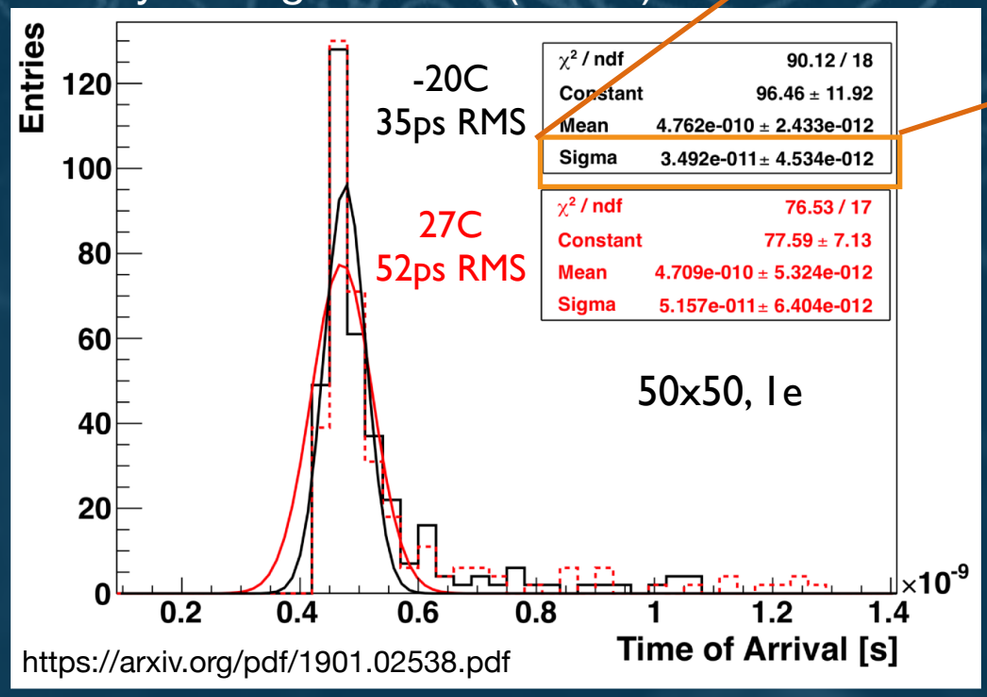
- Development targeting replacement of ATLAS ITk inner pixel system (approx. 2030 after HL-LHC Run 4 or 5)
- Focussing on addition of precision timing feature and increased radiation tolerance while maintaining all other performance specification
  - First prototype will inform us if this capability is within the capabilities of a lower power analog front-end

Specification	RD53B (65nm)	28nm Prototype	Comment
Pixel size	50x50um2	50x50um2	50% for analog FE
Pixel capcitance	<100fF	<100fF	Depends on sensor layout
Min. stable threshold	600e	600e	
Min. in-time threshold	1200e	600e	With sensor capacitance
Hit loss from in-pixel pile-up	<1%	<1%	At nominal hit rate of ~3GHz/cm2
Radiation dose	500MRad	1GRad	Delivered at -15˚C
Timing precision	12.5ns	100ps	

Why Precision Timing?

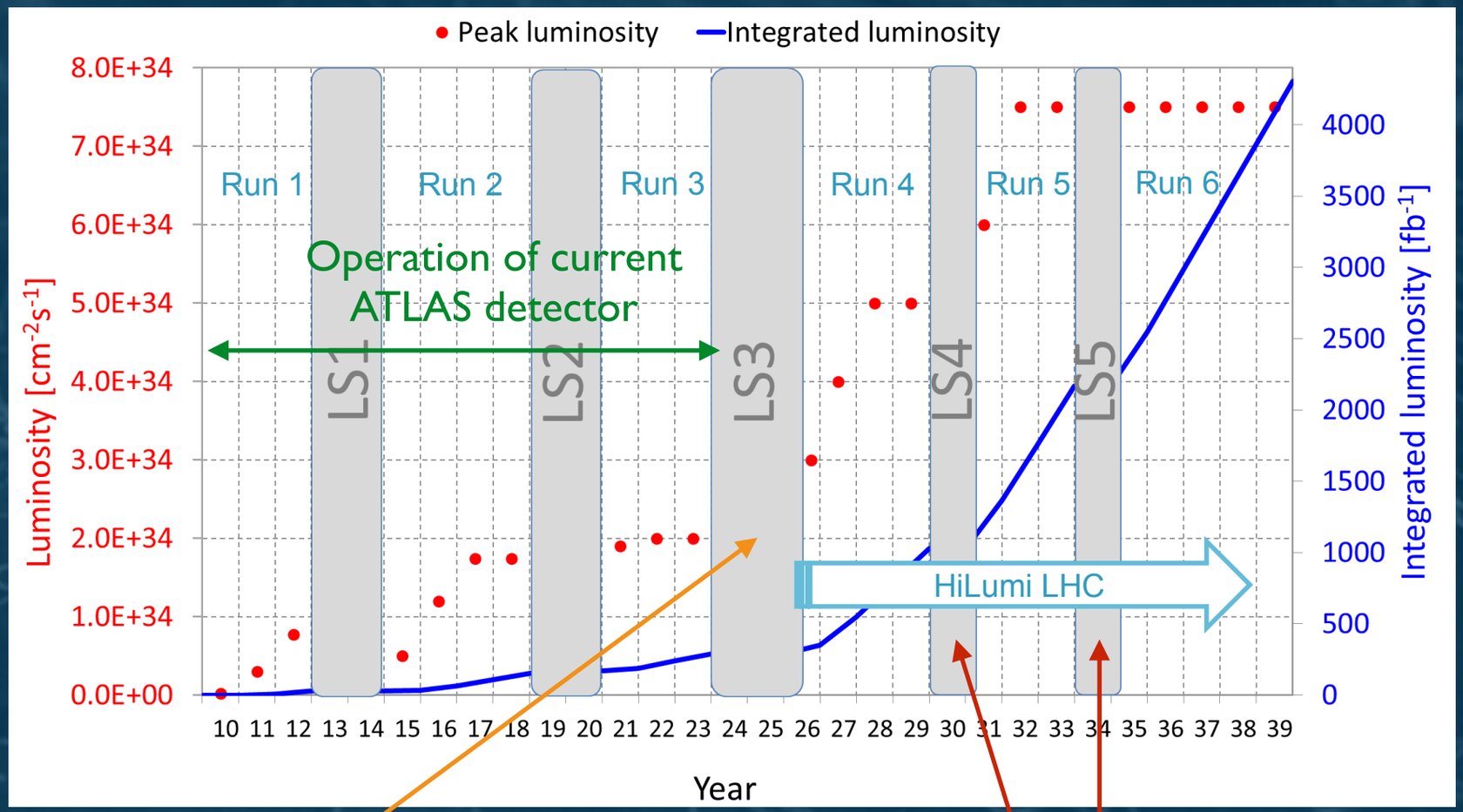
- Assume same spacial resolution (50x50μm²) as ITkPixV1 and reasonably achievable timing resolution of 100ps (for the innermost two layers)
  - Have existing sensor technology for 100ps precision (proven rad-hard)
- Can include timing requirement in track reconstruction (time should be consistent for hits coming from the same vertex)
- Use timing information to reduce number of potential track seeds and reject fakes in high pile-up environments
  - Preliminary studies of having timing information from just 2 layers with 100ps timing indicate around 30% reduction in combinatorics
- Gives interesting synergies with High Granularity Timing Detector (HGTD)





Backup

Introduction



Phase 2 upgrade of ATLAS detector, full replacement of current inner detector with all-silicon Inner Tracker (ITk)

Planned replacement of ITk Pixel Inner System (baseline LS5)

- Two Innermost layers of ITk Pixel detector (Inner System) will need to be replaced in ~2030/2034 → Need to start looking into possible new technologies to improve detector performance beyond current ITk Pixel design