ASIC Block projects to:
provide future SoC chips with example designs & synergistically help maintain and renew a highly skilled HEP aware ASIC workforce

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Background & Motivations

- Over the past 30 years ASIC designs have evolved significantly in sophistication and complexity enabling high precision calorimetry, high rate, high resolution tracking, improving the physics reach of detectors by orders of magnitude per decade.

The technical expertise required for successful designs has grown from

- Primarily physicists and technicians designing circuits with a few transistors at the front end and relatively simple triggering requirements and data conversion off detector.

To the present day where it is not unusual to think of:

- A complete system on a chip (SoC) with analog signals at the input and sparsified data at the output with each ASIC reading out hundreds to thousands of channels. This already Requires design teams with specialists in analog, digital and chip assembly.

Extreme Environments - Our designs go well beyond typical commercially guaranteed environments. Requiring operation for extended periods in: High Radiation, Very cold temperatures etc. Rendering many "off the shelf" commercial solutions useless.

Design Teams for Next Generation Detectors

- Instrumentation design teams need to sit at the table with physicists as the next gen detector systems are being developed to help inspire the possibilities while keeping costs and feasibility in line with what is manufacturable within budget.
- To do this they need to have up-to-date design / verification / version control and testing experience and ways (motivations) to train and maintain engineers and interested physicist staff.
- There is huge motivation to maintain “hands on”
  Design / Development / Testing experience in our institutions
  - Experience improves Submission success rates and Vision of what is possible to do.
    - Design Specification is more successful with experienced personel as participatants.
    - Cost & Schedule predictability improved through experience of design teams.

Handling Decadal design cycles without losing Institutional Memory

LHC Experience

The challenges of LHC fostered a huge number of creative design ideas that were tested in silicon and many were successful.

One problem was that almost everything was new to the community as people turned to deep sub micron designs: High channel counts, High rates but very low power, high levels of rad tolerance integrated D/A's, A/D's, PLL's, Regulators, Power conversion, I/O, Monitoring, input protection, etc. Some things worked well, some things were dropped, some things worked marginally but were accepted "as is" as work able but high maintence.

With LHC upgrade designs behind us and much of the Large scale Neutrino detector designs near final the community needs to evolve a way to maintain the current level of expertise in our design teams and provide training and experience in the state of the art ASIC processes.

Proposal

Development of Basic Building Blocks for ASIC based Front End readout designs in new and existing technologies intended for extreme environments can begin NOW.

We can easily predict the need for BASIC (SoC) blocks

Low power, fast A/D's D/A's PLL's

Monitoring, Power conversion etc.

Designs can start well in advance of final detector specifications and importantly institutions can be encouraged to work together if we have an appropriate funding technique. This may be in the form of suggested topics for DOE sponsored constortia along the lines of the CERN work packages that produced ASICs for LHC , but focused on block designs compatible with next generation SoC ASICs.

Establishing design examples in MPW fabrications so that design & testing techniques are vetted, engineering staff have relevant hands on experience and possibly IP made available for the target design.

Example Blocks

- DCDC conversion on chip - 5V input to 1V core voltages could reduce material & cabling requirements.
- Bluetooth (like) - Wireless Slow control.
- Combination Logic Techniques (Data driven logic) for track clustering & data abstraction
- Clock gating Schemes for power reduction

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With these blocks in hand already experienced Design teams could focus efforts primarily on front end and data processing innovations that address Novel and New functionality as the specifications for Next Generation Detector systems are established.