

# Future Directions in high-speed, transient waveform digitization



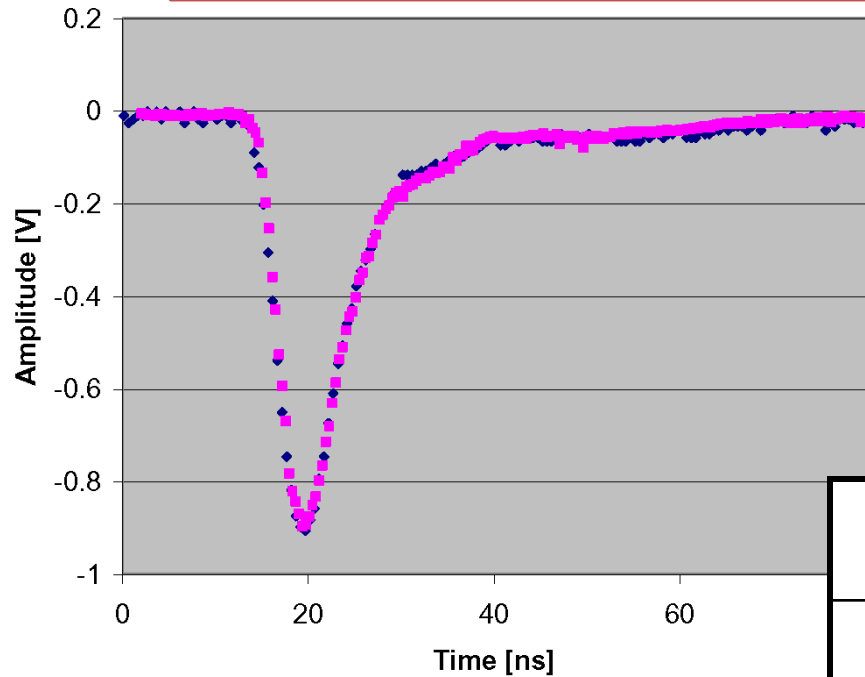
**Gary Varner**  
**University of Hawaii**



**Input to the Snowmass process**

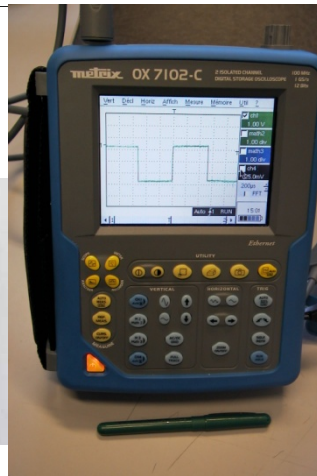
# Switched Capacitor Array technology

Belle TOF FM PMT signal



- 2 GSa/s, 1GHz ABW
- Tektronics Scope
- 2.56 GSa/s LAB

“oscilloscope on a chip”



	WFS ASIC	Commercial
Sampling speed	0.1-6 GSa/s	2 GSa/s
Bits/ENOBs	16/9-13+	8/7.4
Power/Chan.	$\leq 0.05W$	Few W
Cost/Ch.	$< \$10$ (vol)	$> 100\$$





# Belle II Detector

# ent

BEAST (Background commissioning detector)

EM Calorimeter:  
CsI(Tl), waveform sampling (barrel+ endcap)

electrons (7 GeV)

Beryllium beam pipe  
2cm diameter

Vertex Detector  
2 layers DEPFET + 4 layers DSSD

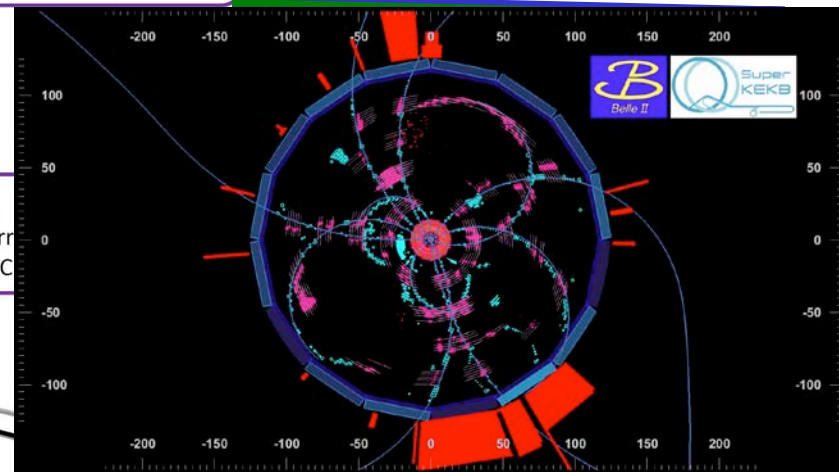
Central Drift Chamber  
He(50%):C<sub>2</sub>H<sub>6</sub>(50%), small cells, long lever arm, fast electronics (Core element)

KLong and muon detector:

Resistive Plate Chambers (barrel outer layers)  
Scintillator + WLSF + SiPM's (end-caps , inner 2 barrel layers)

Particle Identification

TOP detector system (barrel)  
Prox. focusing Aerogel RICH



positrons (4 GeV)



Belle II now has grown to ~947 researchers from 26 countries

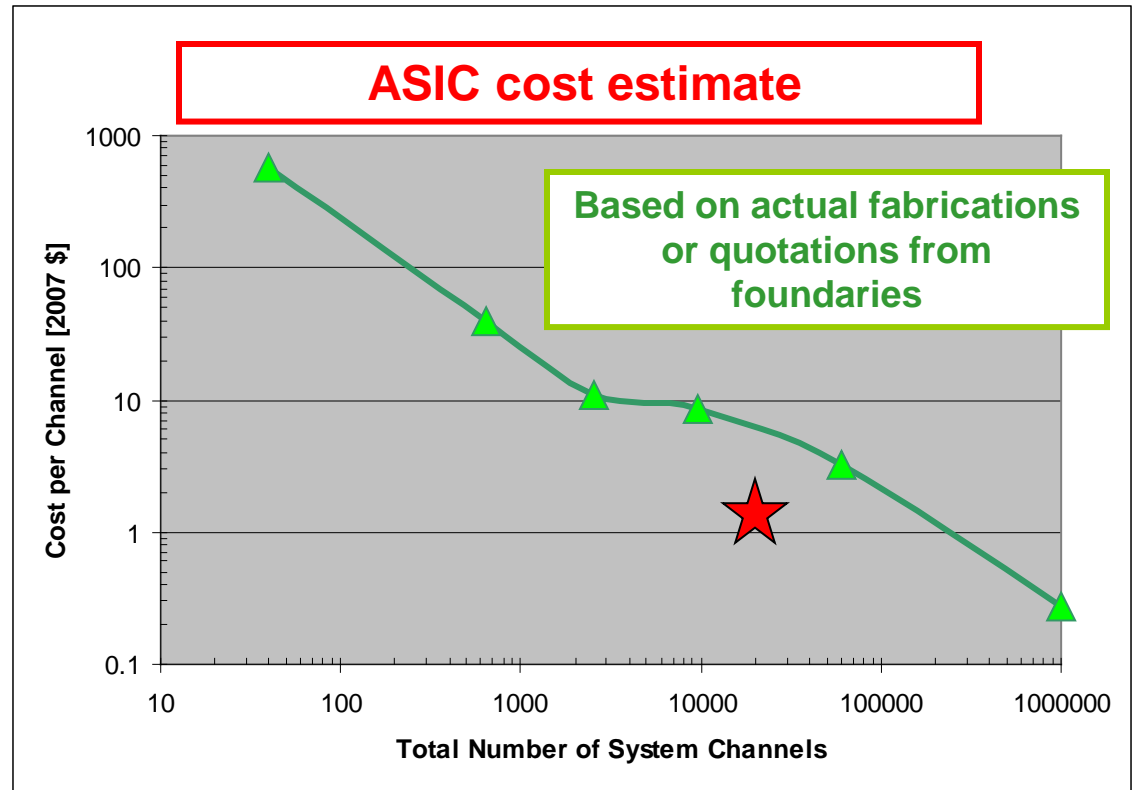
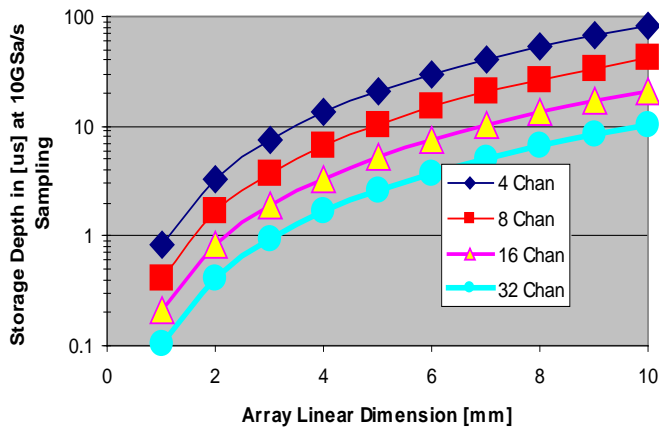
for the future: Snowmass prelude – July 2020

# What can learn from these developments

- ASIC costing well understood, very competitive!

**NIM A591 (2008) 534-345.**

Storage Depth Capacity





# Cherenkov Telescope Array

Chile



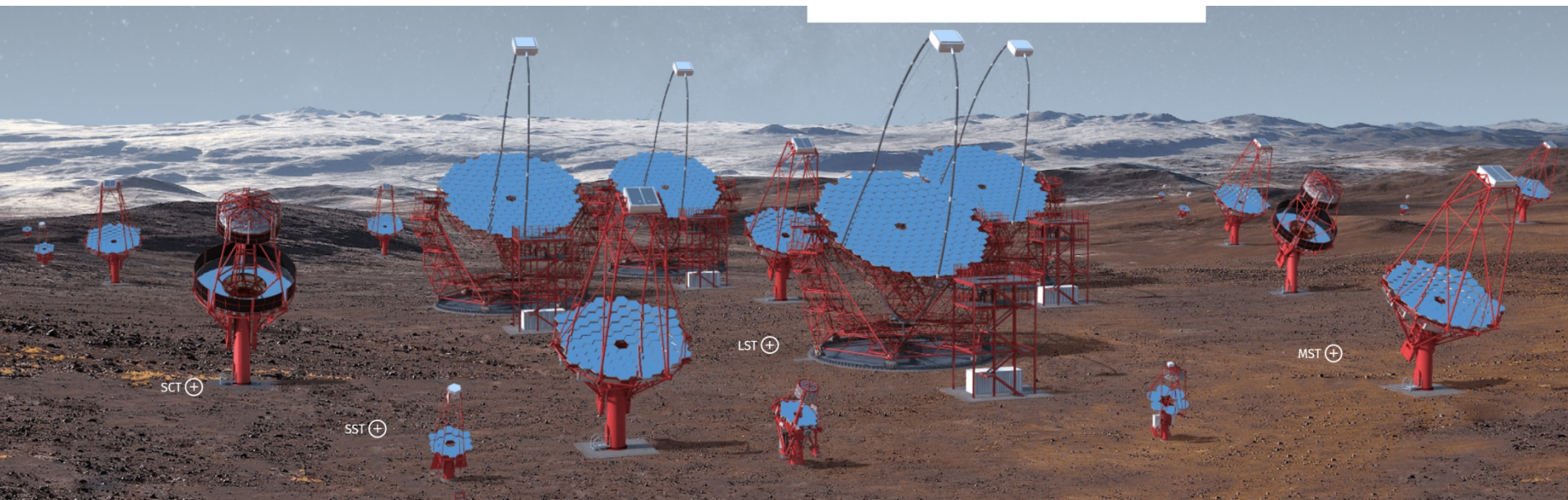
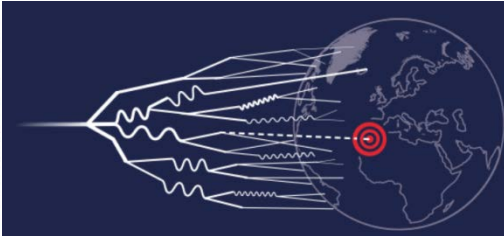
La Palma



## About

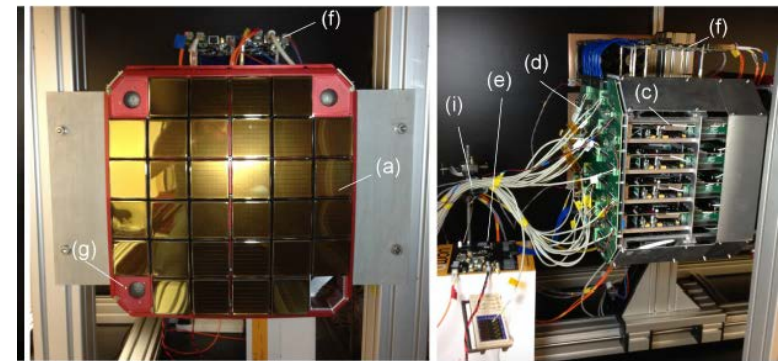
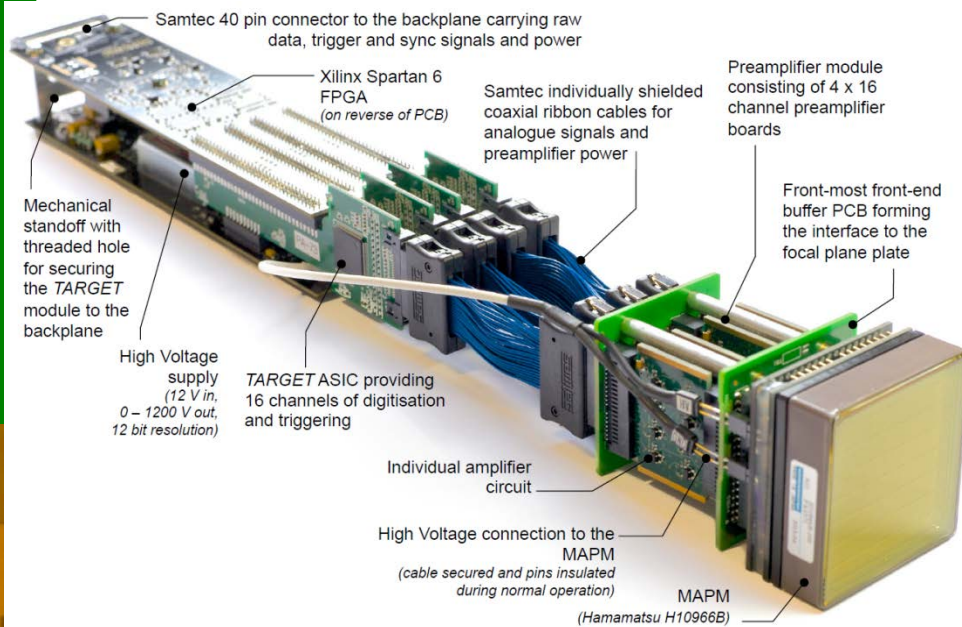
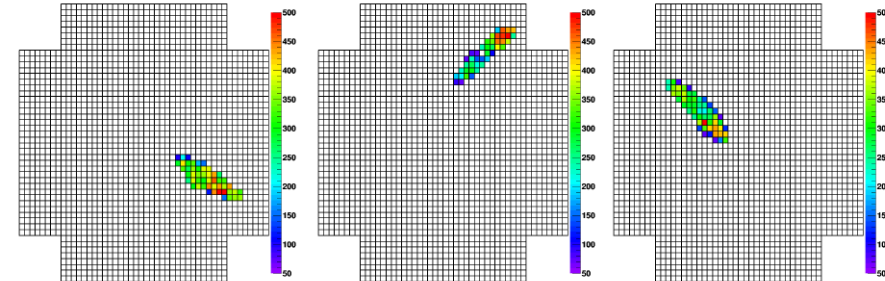
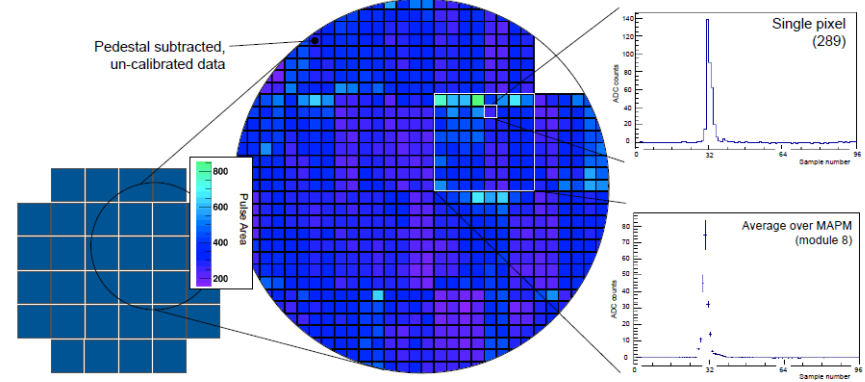
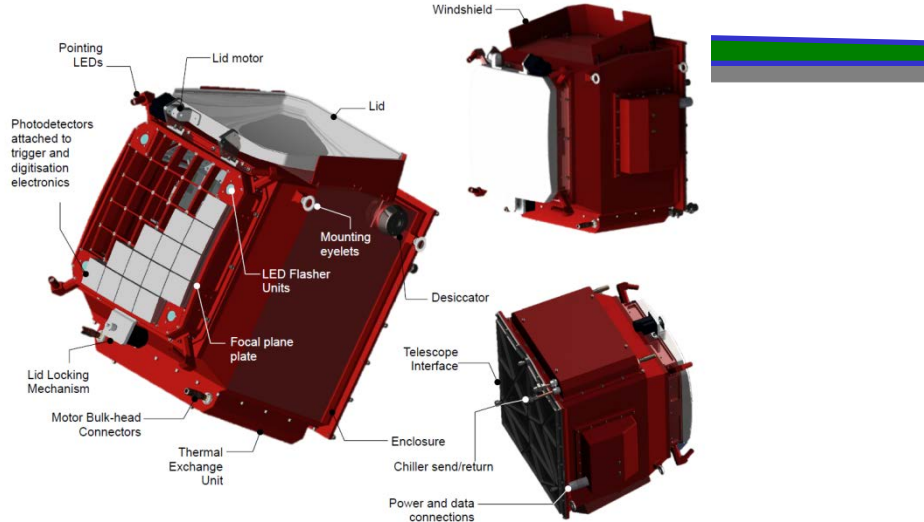


The Cherenkov Telescope Array (CTA) is the next generation ground-based observatory for gamma-ray astronomy at very-high energies. With more than 100 telescopes located in the northern and southern hemispheres, CTA will be the world's largest and most sensitive high-energy gamma-ray observatory.





# GCT Camera (CTA) – Gearing for prod.

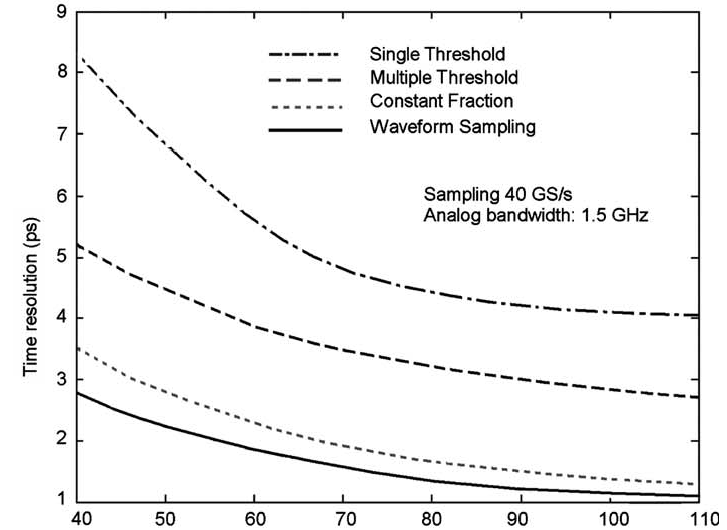
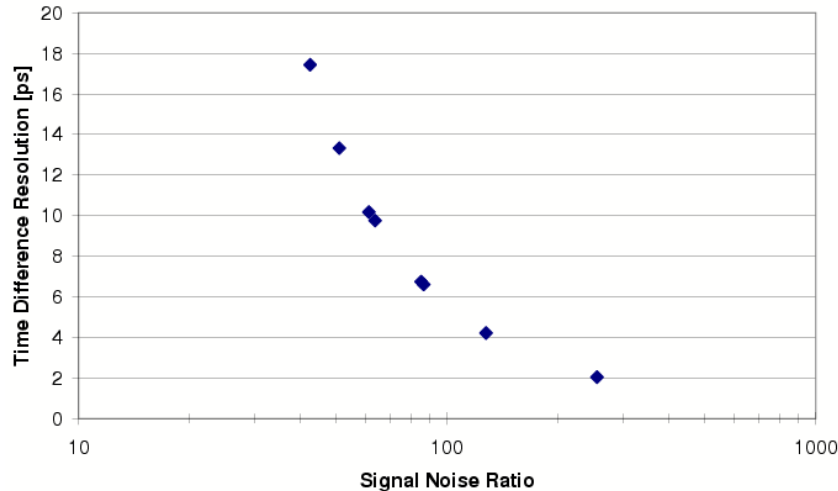


# Technology has room to improve

1GHz analog bandwidth, 5GSa/s

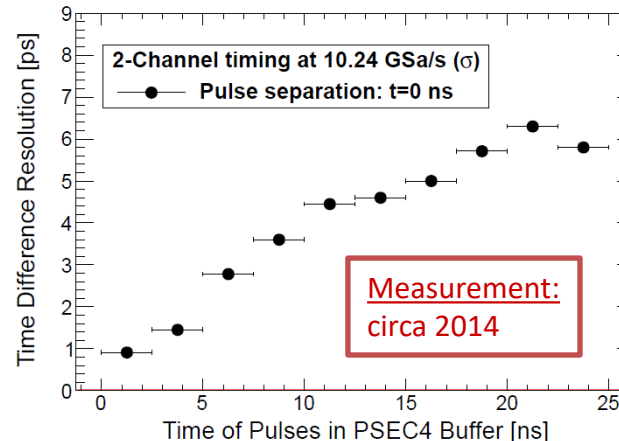
Simulation includes detector response

Time Difference Dependence on Signal-Noise Ratio (SNR)



G. Varner and L. Ruckman  
**NIM A602 (2009) 438-445.**

J-F Genat, G. Varner, F. Tang, H. Frisch  
**NIM A607 (2009) 387-393.**



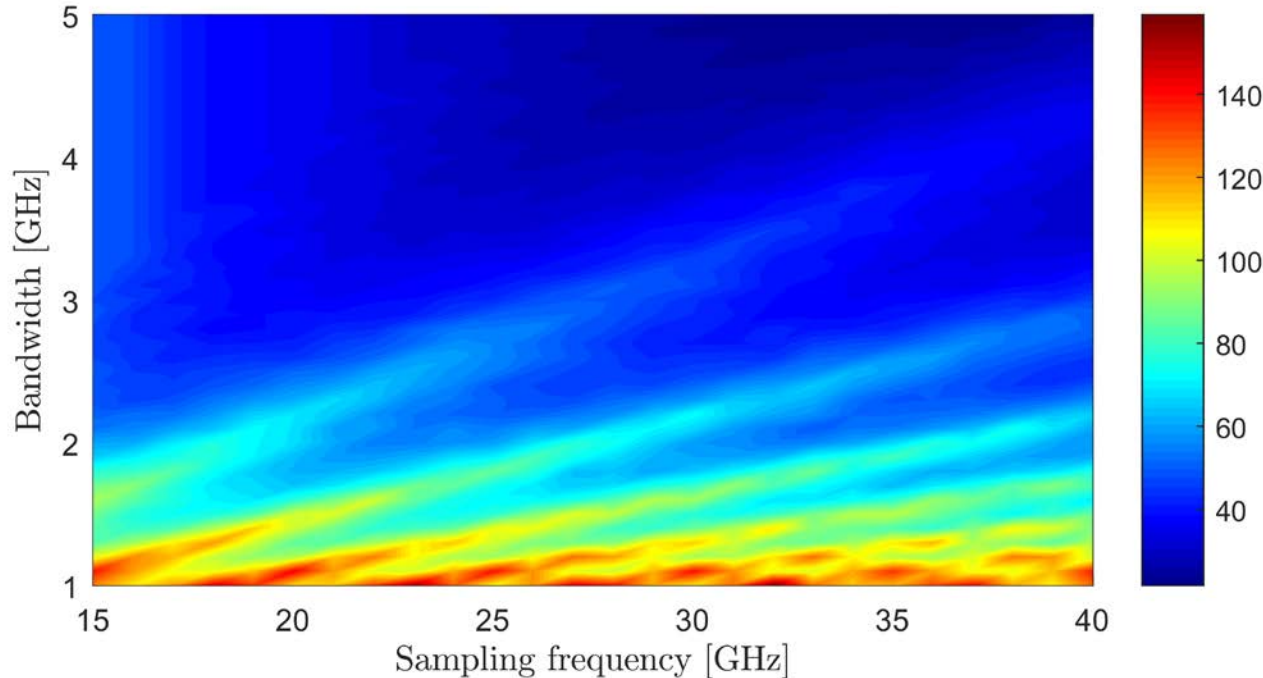
Extending to 1ps and lower, with advanced calibration techniques

E. Oberla, J-F Genat,  
 H. Grabas, H. Frisch,  
 K. Nishimura, G. Varner  
**NIM A735 (2014) 452-461.**

Measurement:  
 circa 2014

# Now pushing to the femtosecond regime

Pushing sampling speed and analog bandwidth



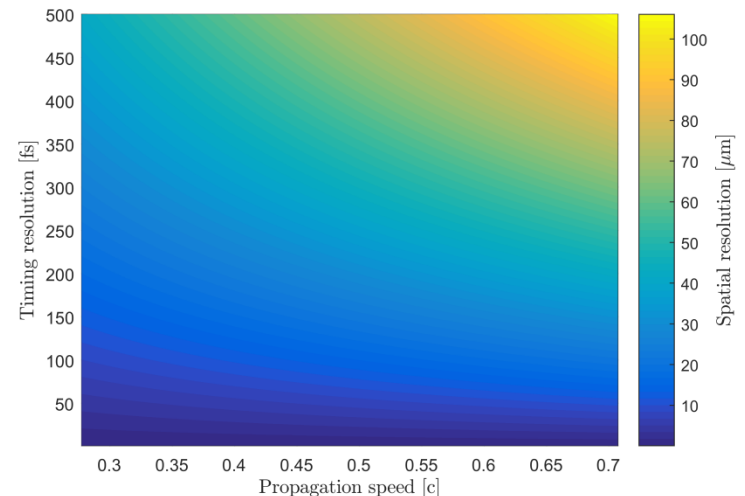
P. Orel, G. Varner  
and P. Niknejadi  
NIM A857 (2017) 31-41.

**Femtosecond timing:  
exchange timing for  
micron spatial  
dimension (channel  
count reduction)**

And pushing the **space-time limit**  
(new type of PID or DIRC devices?)

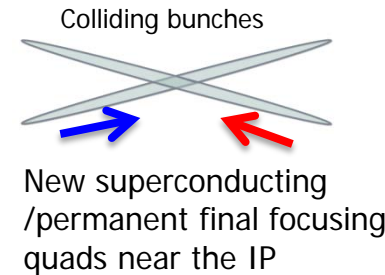
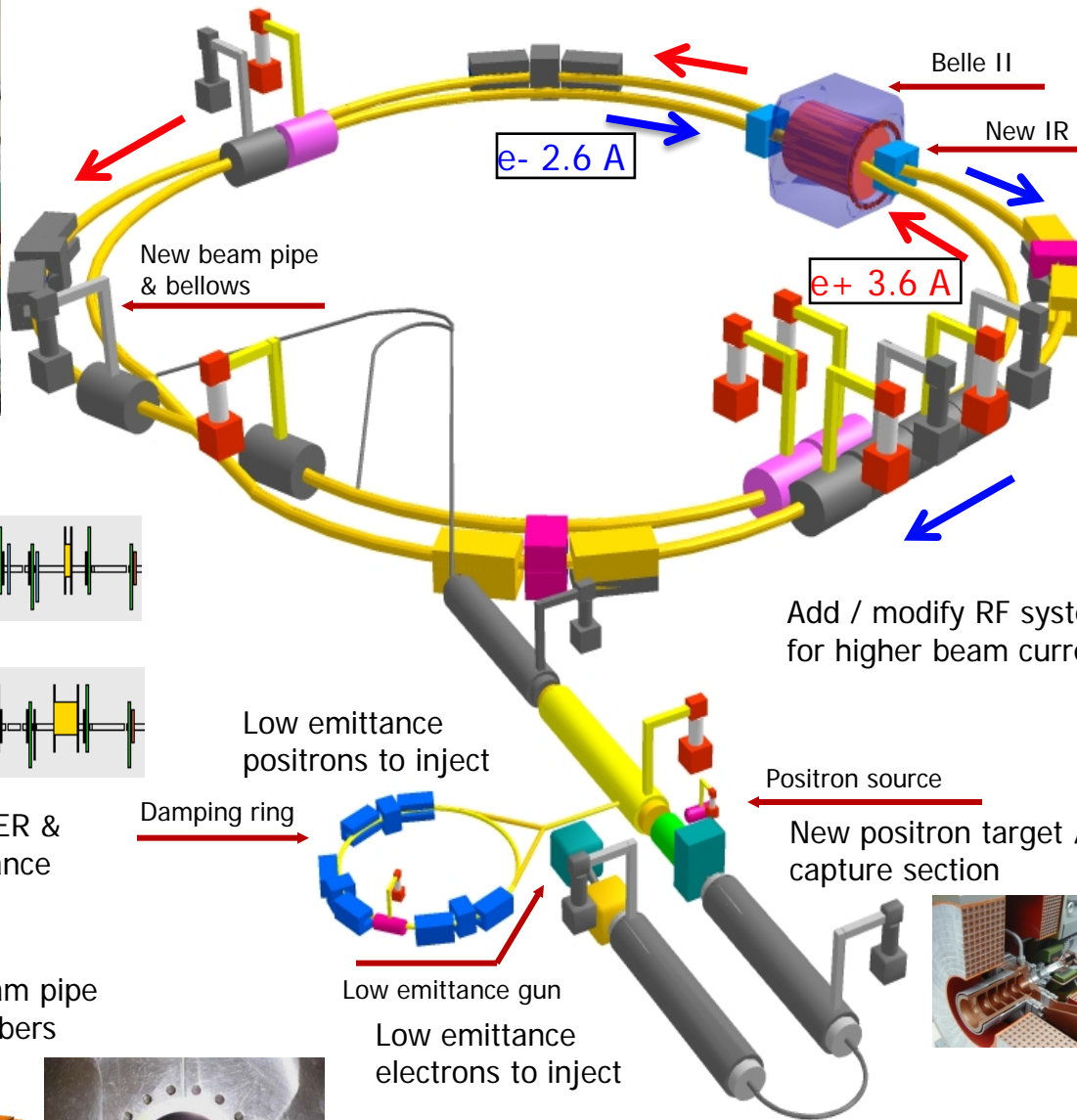
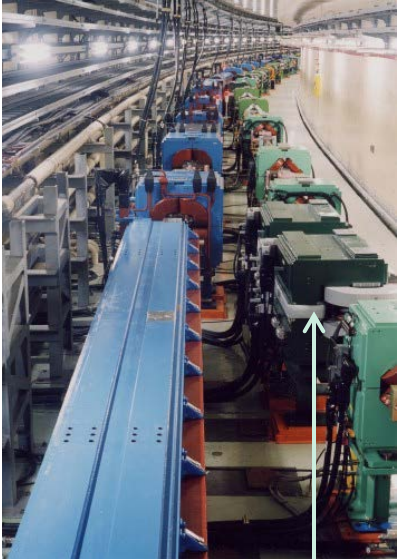
P. Orel and G. Varner

IEEE Trans. Nucl. Sci. **64 (2017) 1950-1962.**

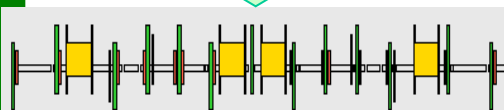
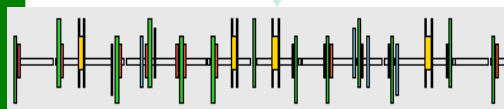




# KEKB to SuperKEKB



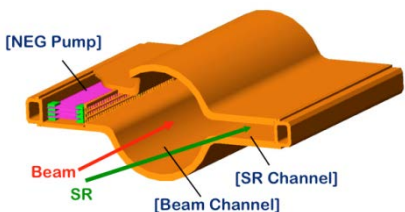
Replace short dipoles with longer ones (LER)



Redesign the lattices of HER & LER to squeeze the emittance

**Nano-beams!**

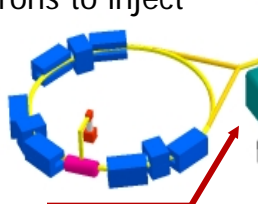
TiN-coated beam pipe with antechambers



Add / modify RF systems for higher beam current

Low emittance positrons to inject

Damping ring

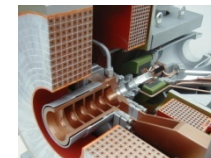


Low emittance gun

Low emittance electrons to inject

Positron source

New positron target / capture section

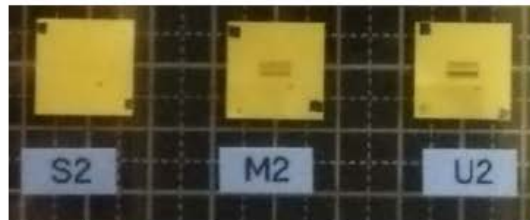


*To get x40 higher luminosity*

# Huge data challenge: online reduction (many TB/s)



X-ray beam line under construction at LER



Masks:  $\sim 20 \mu\text{m}$  Au on  $600 \mu\text{m}$  CVD diamond substrate



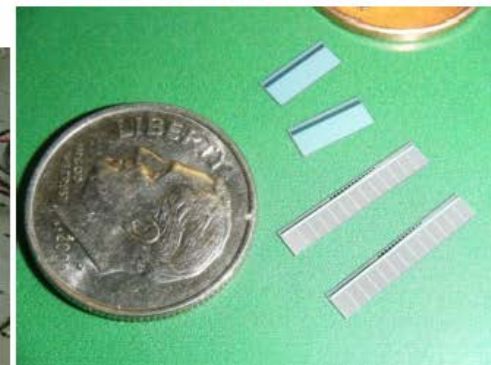
Water-cooled mask holder

US-Japan Collaboration (U. Hawaii, SLAC, Cornell U.)

High-speed readout electronics for the X-ray monitor, being developed by U of Hawaii.

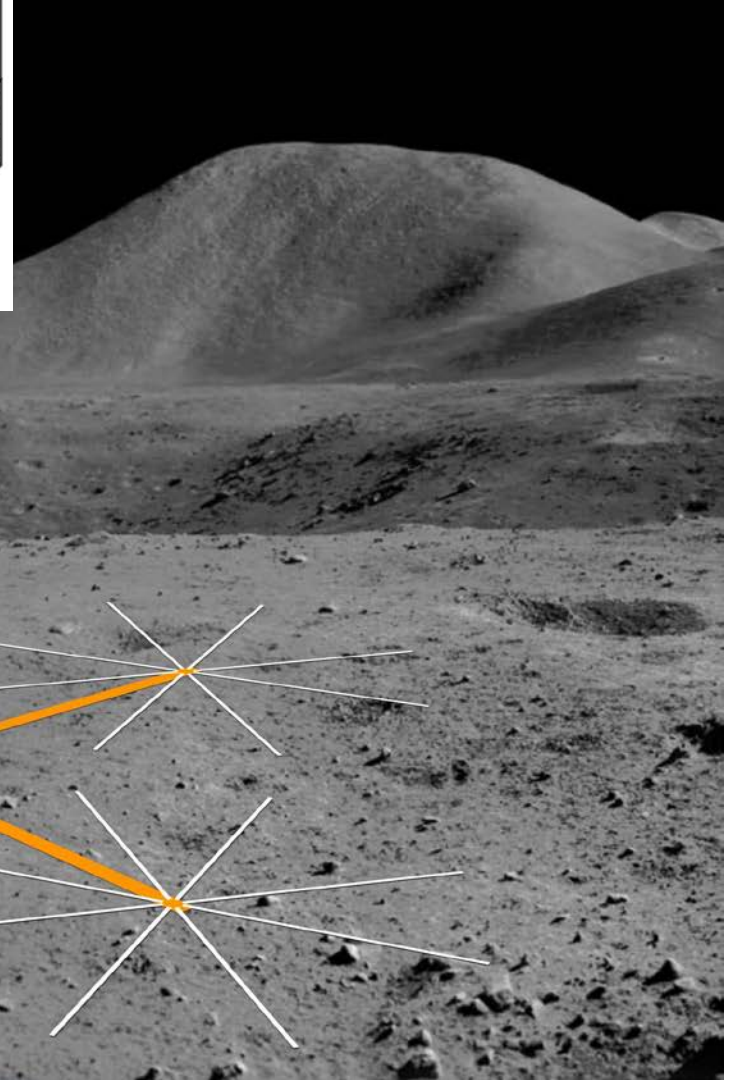
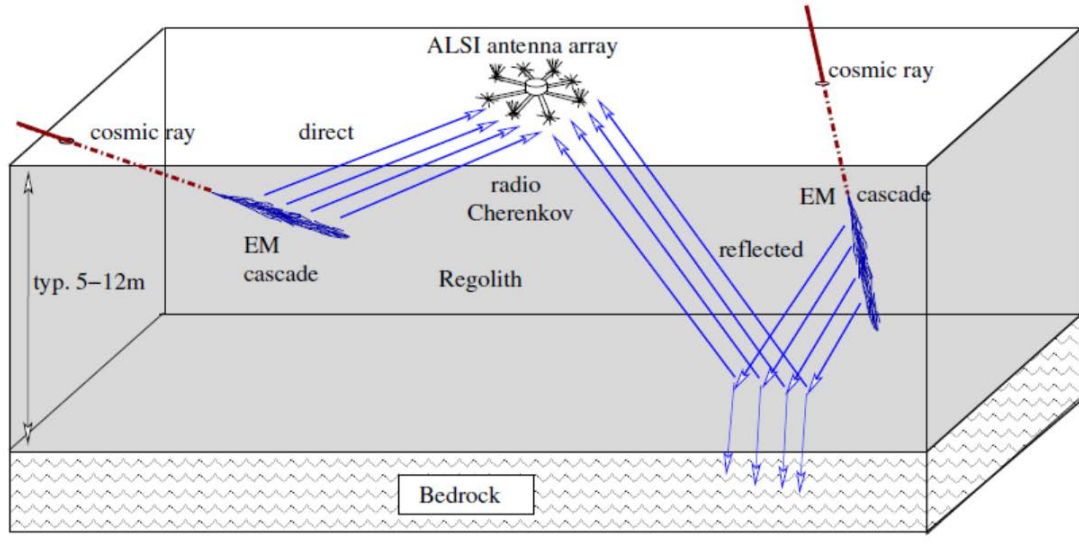


Deep Si pixel detector and spectrometer chips for the X-ray monitor, being developed at SLAC.





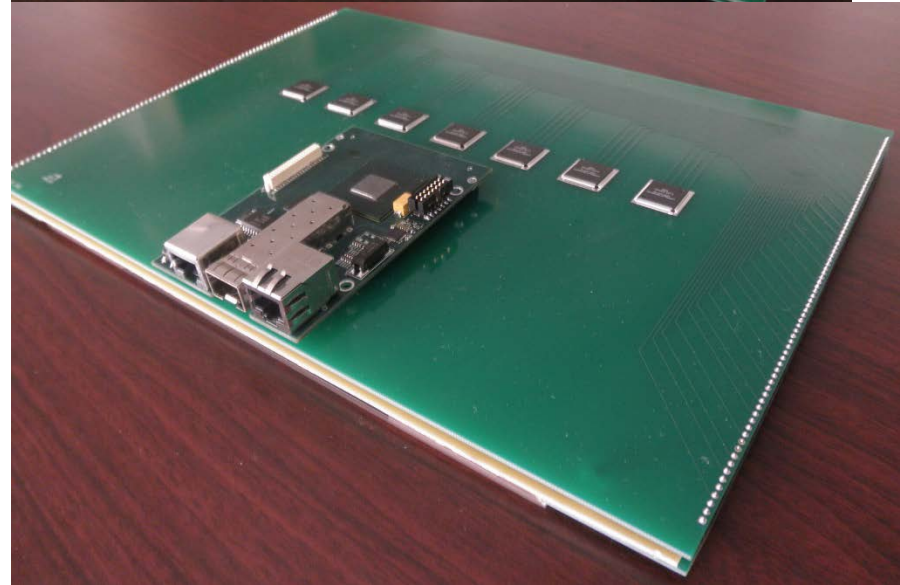
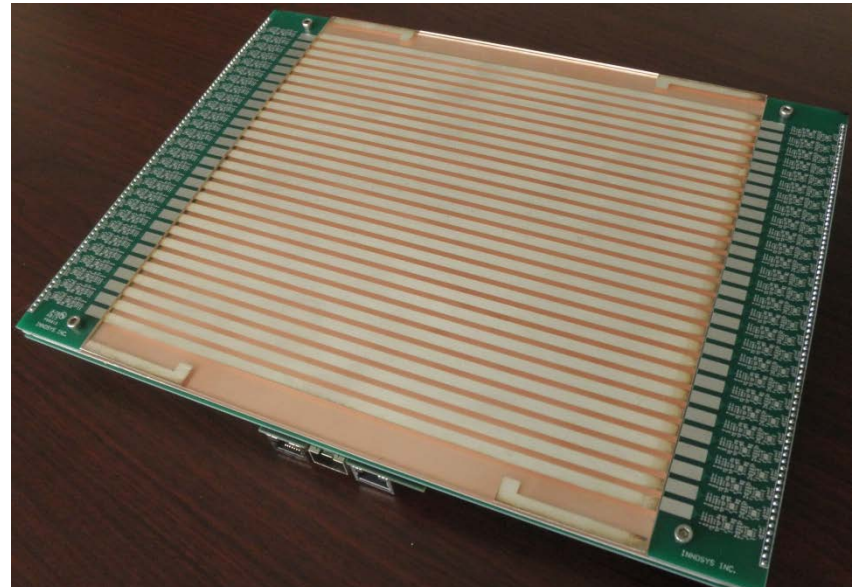
# Low power: Lunar cosmic-ray radio geology





# Strategy for Extreme Low Power operation

- Only power what actually need
- CMOS intrinsically zero power when idle
- Strategy works for either strip or pixel geometry
- Places to reduce power:
  - Remove FPGA
  - Low-power processing
  - **Single ASIC**



# Future directions (summary)

1. Femtosecond timing to provide
  - a. Reduction of spatial granularity (8M -> 4k ch.)
  - b. “streak camera” diagnostics
2. Feature extraction (marry more digital processing with power of SCA) for ‘up front’ data reduction
3. As scale to large experimental systems, cost and POWER are huge (existential) issues

