Workforce Development – Kurtis Nishimura

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What?

Develop tools, organizational structures, codebases, schools & courses, ..., that can help to efficiently train the next generation of those working on electronics* for HEP.

*My personal view was mainly toward FPGA and ASIC synthesis flows, but could imagine those to be parts of a broader effort in general electronics or ASIC design.

**Also recognizing that this could be a better match for “IF4: Trigger and DAQ,” but FPGA development targeted at testing and supporting ASICs can require unique expertise.

Why?

Local experience from our own university group and collaborations we're involved in:

- It's quite hard to find expertise in electronics, but especially so for digital logic development (both FPGA and ASIC), and particularly in "smaller" collaborations.

Can always train locally, but…

- Graduate student / postdoc physicsts often starting from low level in modern electronics.
- Graduate student / postdoc EE often starting from low level in physics.

- Often things are learned "the hard way" - by taking (often bad) examples and trying to make them work, throwing up one's hands, then starting a new (often differently bad) example that someone else uses later.

How?

Some starting ideas for addressing these issues:

- Common training efforts (course curricula [academic or shorter ‘boot-camp’], schools, workshops, reading lists…).
- Access to well vetted blocks – often turns what seems like an insurmountable problem into putting together lego pieces.
    - May not need to be truly open source to all, but open to the community at least.
    - e.g., SLAC surf has many HDL blocks available open source with an extremely permissive license.
    - I would guess that other labs and groups have their own libraries, maybe even available open source already.
    - For ASIC-oriented design, provide a list of what technologies, libraries, temperatures(?) blocks have been vetted in (guessing this part cannot be open source).
- For ASIC, open access tools and PDKs? e.g., Skywater 130 nm w/ standard cells
    - Early days, but seems worth keeping an eye on, and maybe enabling for those without access to pricey tools.

Synergies?

Obvious synergies from the talks today:

- “Blocks for SOC” (Mitch Newcomer)
- “Internships” (Jim Hoff)
- “HEPIC” (Jim Hoff)
    - Perhaps improved coordination via HEPIC could make it easier to form a cohesive effort on workforce development?

Some specific technical efforts:

- Q-Pix Consortium (see “Kiloton Scale LArTPC Pixel Based readout” (Jonathan Asaadi) – aiming to keep underlying HDL open source and available to community.
- Working to keep local codebases open source when possible (see here for an example of how our group locally is starting to standardize GbE interfaces), also encouraging local developers to use existing libraries when it’s a good fit (e.g., SLAC surf).

Conclusion

Just some ideas to get discussion started…

At very least, I'm sure as a community we can do a better job of training in these specialties more efficiently, so I hope we can adopt some changes in that direction!