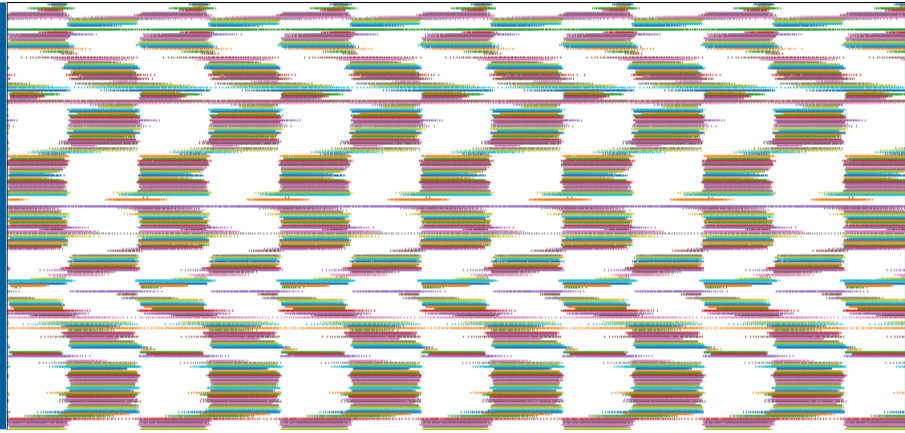
Smart Detectors Using Neuromorphic Computing

THE INTELLIGENT PATH TO LOW MASS



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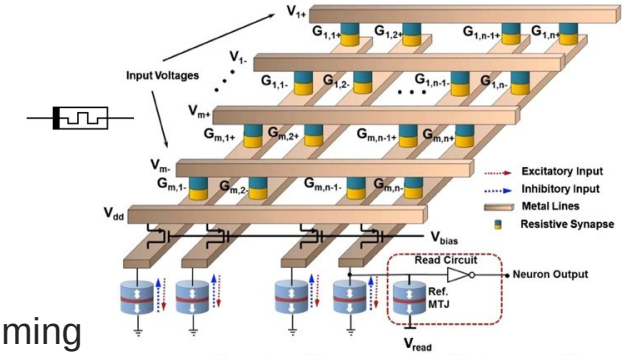
Using Neuromorphic Computing

- Technology from neuromorphic computing used for extremely low power calculation
  - Based on memristors (ReRAM)
    - Resistive value is a weight that is learned or set
      - In neuromorphic computing proportional to signal timing
    - ReRAM avoids look-up tables or storing and reading values from memories and has small on chip area
      - A CMOS ReRAM CAM uses **45% less area** and **96% less power**
  - ReRAM can be fabricated using CMOS technology
  - ReRAM can be used for neuromorphic learning
- Considerable R&D is necessary to include non-Von Neumann elements into HEP Readout ICs
  - And to develop intelligent detectors and algorithms to take advantage of the potential
  - Snowmass LoI IF7/IF4 180

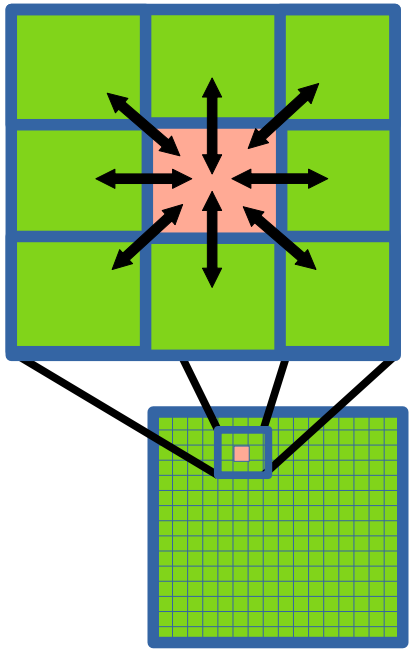


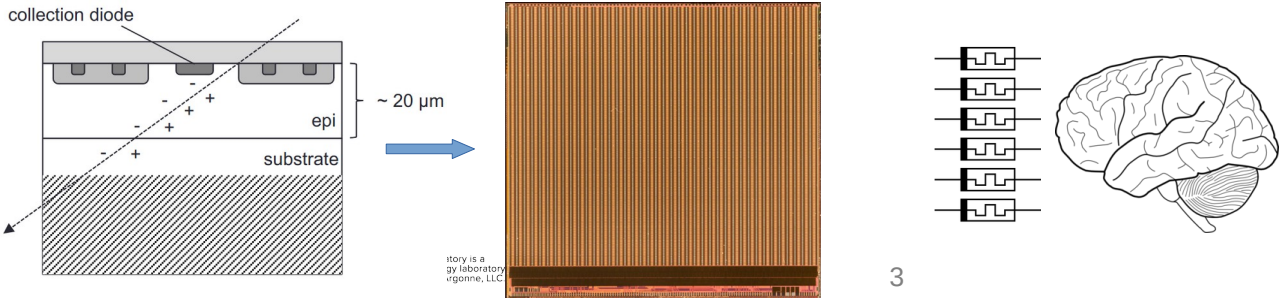
$$G_x = \begin{bmatrix} -1 & 0 & +1 \\ -2 & 0 & +2 \\ -1 & 0 & +1 \end{bmatrix} \qquad G_y = \begin{bmatrix} +1 & +2 & +1 \\ 0 & 0 & 0 \\ -1 & -2 & -1 \end{bmatrix}$$

$$G = \sqrt{G_x^2 + G_y^2}$$

Target Application: Silicon Pixel Detector

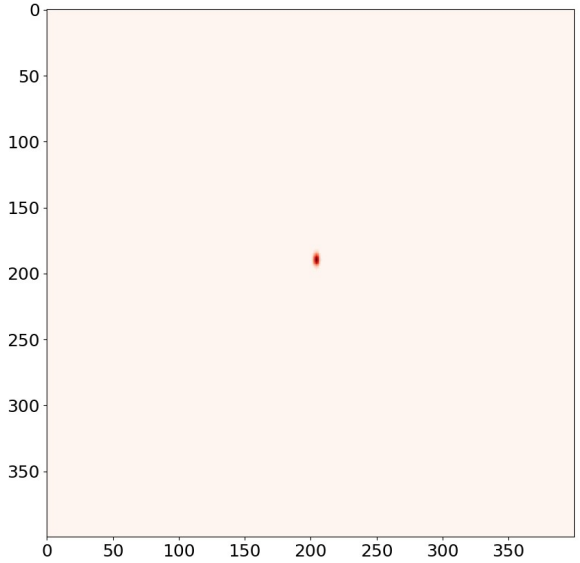
- Apply to a Silicon Pixel Detector Read out Integrated Circuit (RoIC)
  - A silicon pixel module gives natural scale for simulation – using 400x400 pixels
    - Corresponds to one HL-LHC ATLAS ITk Pixel front end chip
  - Pixel cluster finding for non-trivial computation
    - Use only nearest neighbor hits for purely local calculation
  - Ability to identify hit clusters provides a worthwhile goal
    - Data unpacking and hit clustering dominates the ATLAS trigger's track reconstruction processing time
- Algorithm uses ReRAM to do analog matrix multiplication
  - Distributed coincidence filter
  - Local Sobel Filter for image edge detection
  - **No learning** in current implementation
    - Each time step processed independently



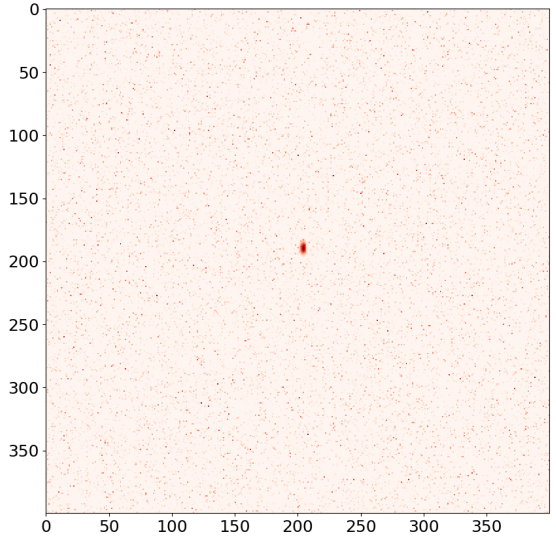


Example Hit

- Total number of signal pixels is 54 channels – 0.03% (ITk-like occupancy)
  - Total charge of 17.9 peak-value normalized units
    - Signal charge follows Gaussian distribution
- Total number of noisy pixels is 15,245 channels – 9.5%
  - Total charge of 2,291.3 signal peak-value normalized units
    - Noise charge sampled from exponential

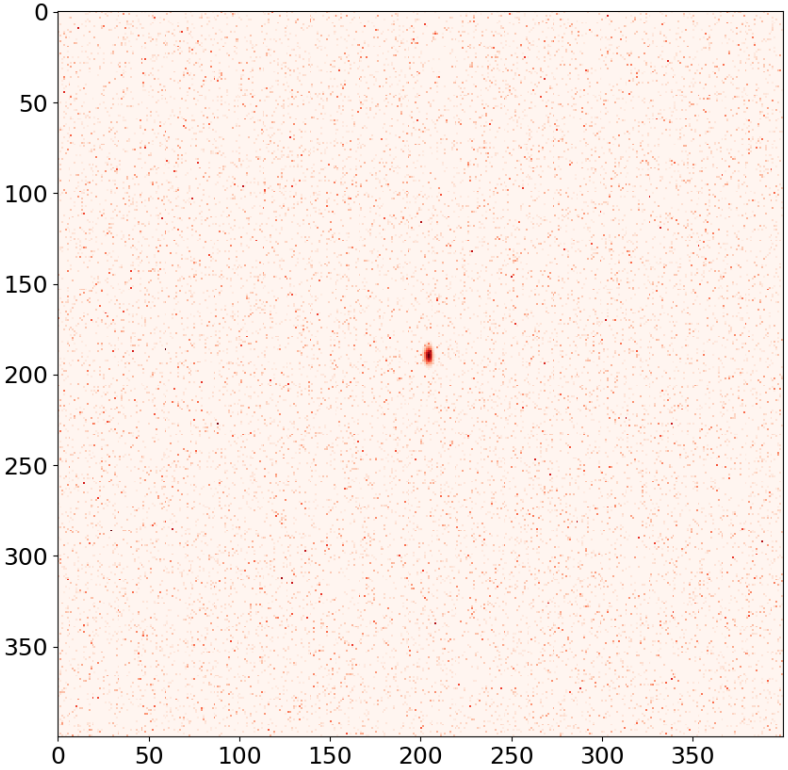


Signal

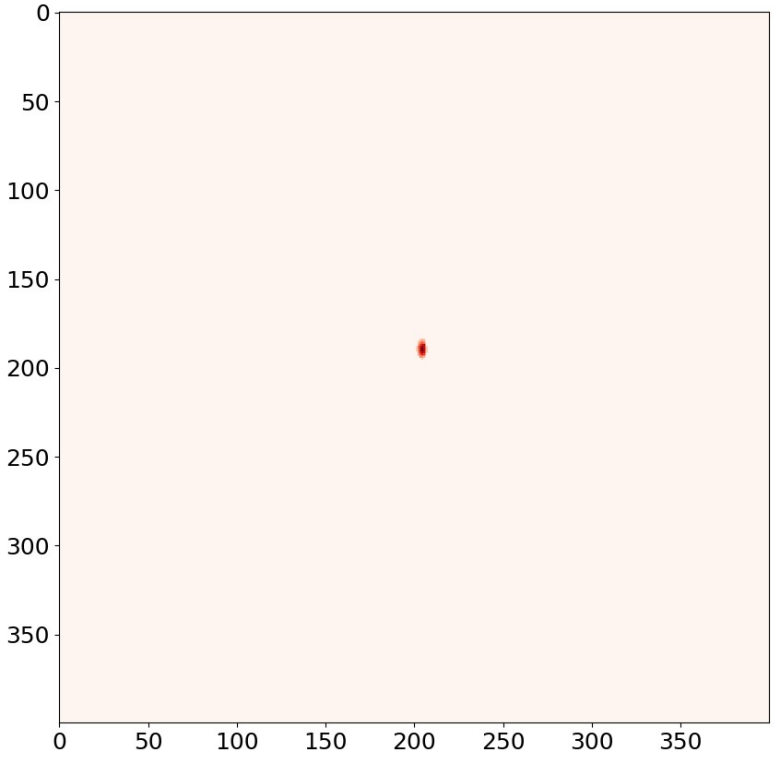


Signal+Noise

Clean Up Noise

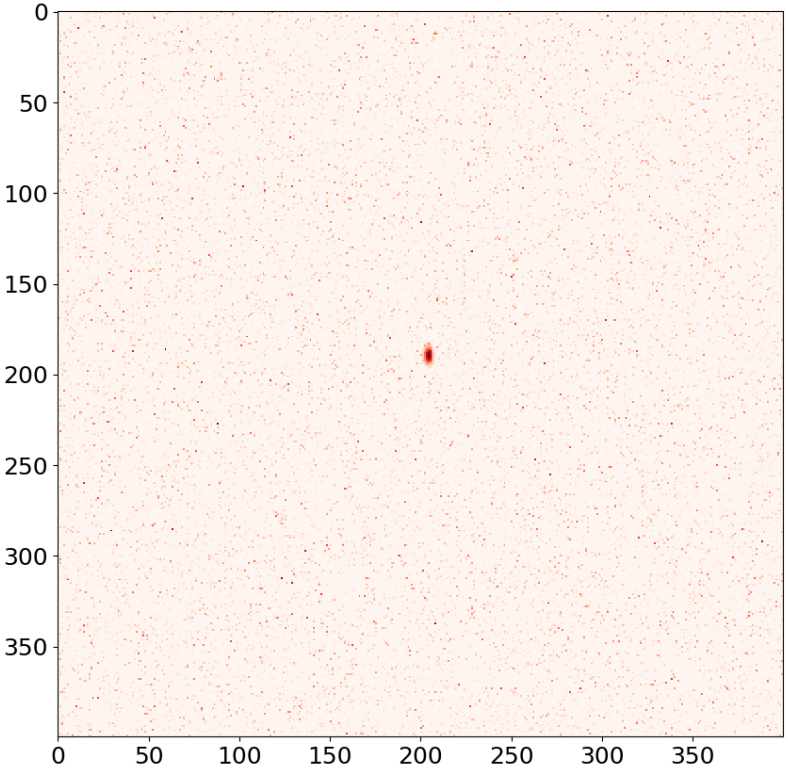


Input Data

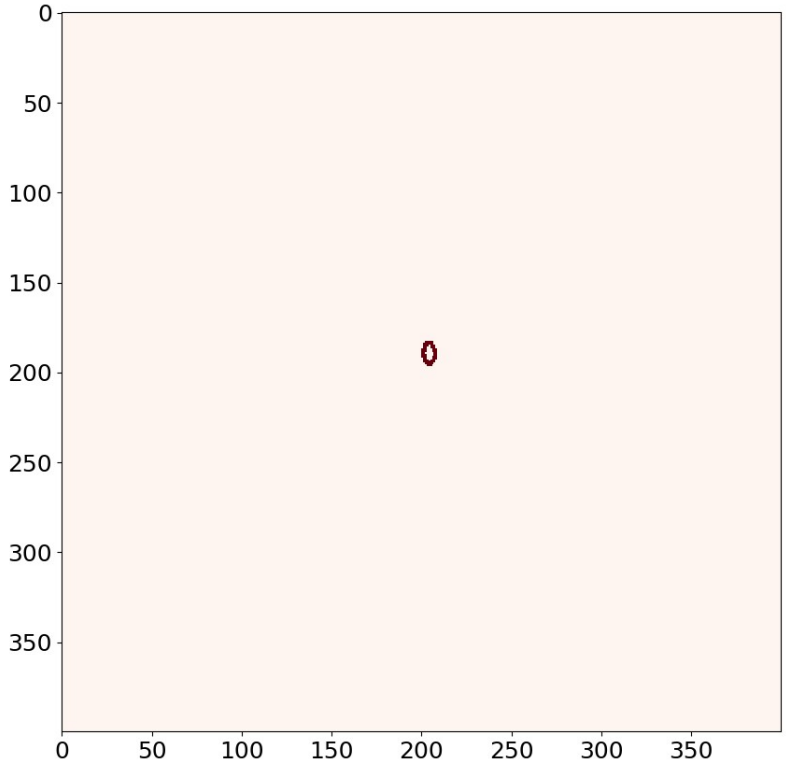


After Noise Filtering

Cluster Finding



Input Data



Filtering + Edge Detection

Potential Impact

- This example algorithm based on theoretically usable IC components reduces readout bandwidth by 92% and requires ~2 μW per pixel
- ITk Pixel will require 100kW of cooling power
  - This algorithm would increase the power required by **~200W** or ***0.3%***
- The noise rate in ITk Pixel FE is $<10^{-6}$ not 0.1
  - Benefit of noise filtering is negligible
- On average reading out only cluster edges reduces bandwidth by **50%**
  - Potentially reduce ITk Pixel services by 50% and decrease needed support structure
  - The mass of services and support structures represents **~80%** of the ITk Pixel x^0 at $|\eta| \sim 2$
    - Regardless of readout technology this would reduce mass
- Potential impact on design of fully integrated CMOS pixel detectors
  - Could enable fully CMOS detectors with a pixel pitch down to the order of the CMOS process feature size