

ECON ASICs

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ECON-T status

- **Submission goal:** September has been plan since ~June, and **October is drop dead date.**
- **Verilog** (Ralph) is ~100% complete including major iteration with top-level place-and-route (Chinar) in July
- **Block level synthesis / place-and-route** (Alpana) is more streamlined
 - working to catch up with final verilog changes in late July.
- **Top-level synthesis / place-and-route** (Chinar) is progressing well
 - major effort to converge (iteratively) with Ralph on chip hierarchy in July
 - converging on floor plan, placement of I/O, power ring (with Davide)
- **Verification (Hoff, Gingu)**
 - ~finished incorporating July verilog changes into top-level UVM framework
 - **Need additional Hoff effort in August to get i2c and eRx data flowing**
 - major contributions from Danny Noonan (Florida Tech) are saving significant effort
- **PLL (Xiaoran)**
 - realized technical challenge in transferring 6-layer lpGBT design to 9-layer ECON-T
 - Because of 50% time in July, still requires ~5 weeks @ 100% effort to complete → **threatening October submission**

July/Aug: Received 50–60% both

Future : **Need 100% of Xiaoran**

	<i>June</i>	<i>Jun 29 - Jul 6</i>	<i>July 06-12</i>	<i>July 13-19</i>	<i>July 20-26</i>	<i>July 27 - Aug 02</i>	<i>Aug 03 - Aug 09</i>	<i>Aug 10-16</i>	<i>Aug 17-23</i>	<i>Aug 24-30</i>
<i>Hoff</i>	<i>~60% FTE</i>	<i>19 hrs</i>	<i>17 hrs</i>	<i>25 hrs</i>	<i>26 hrs</i>	<i>31 hrs</i>	<i>~50% FTE</i>	<i>25%</i>		
<i>Xiaoran</i>	<i>~75% FTE</i>	<i>28 hrs</i>	<i>32 hrs</i>	<i>26 hrs</i>	<i>20 hrs</i>	<i>20 hrs</i>	<i>~50% FTE</i>	<i>100%</i>		

ECON-T status

	<i>Mar</i>	<i>Apr</i>	<i>May</i>	<i>June</i>
<i>Xiaoran</i>	32	36	34	34

Xiaoran averaged 75–85% FTE on ECON since starting at Fermilab in March – I can't see total, so I don't know denominator.