Considerations for future Trackers

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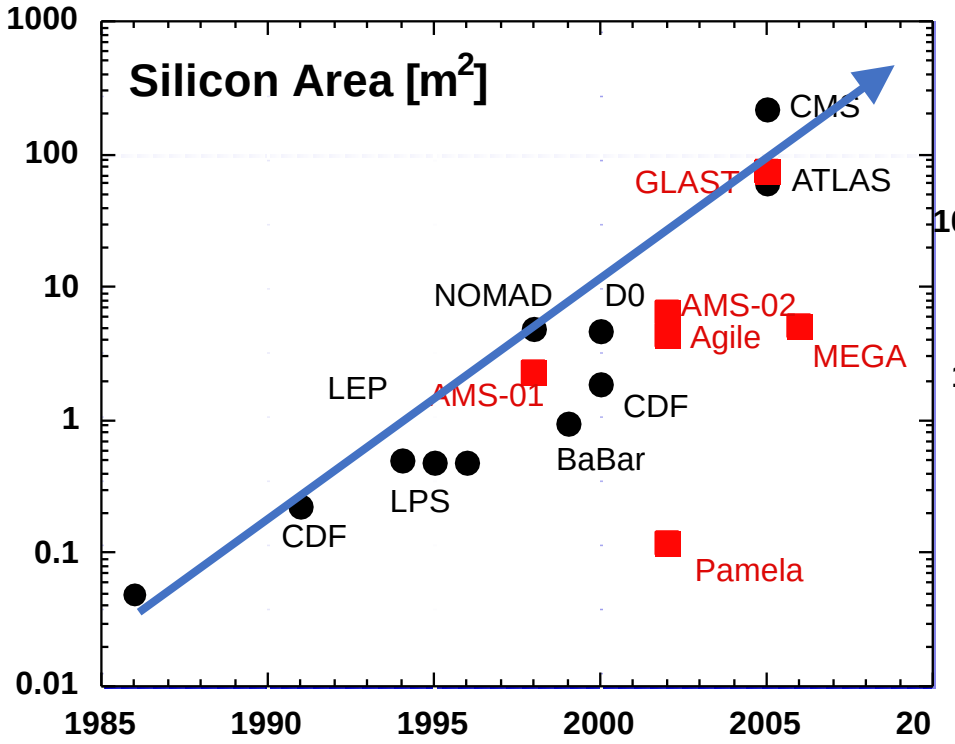
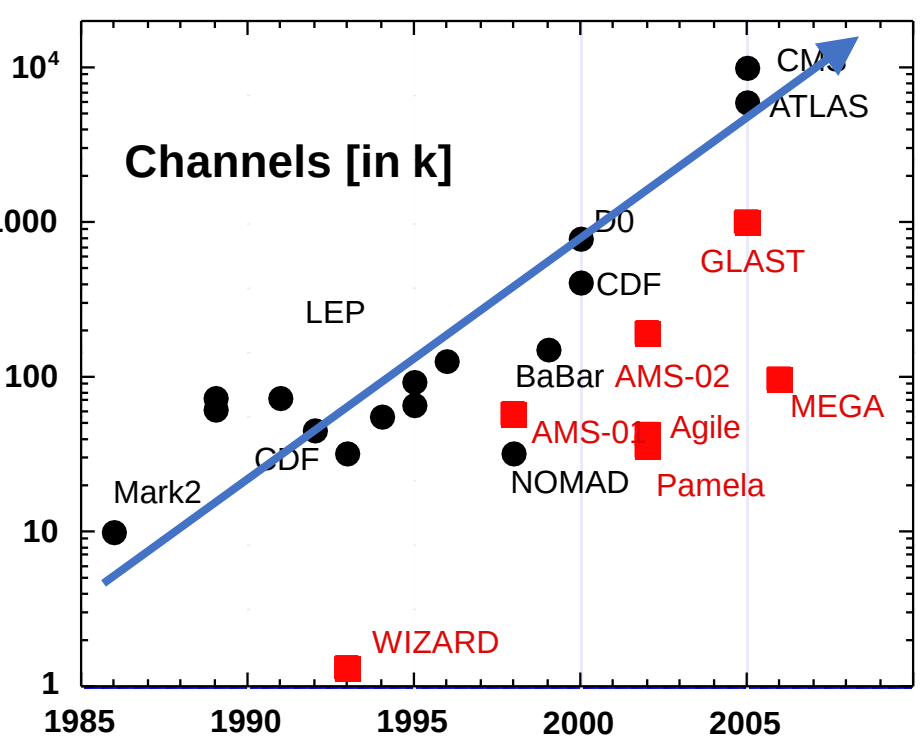
Trends

- Have had a version of "Moore's Law" with "silicon in trackers"
  - Plots curtesy Hartmut Sadrozinski (circa 2001)
  - Silicon area grows by **x2.4** every 2 years
  - Number of channels grows by **x2.1** every 2 years

The original:
"Number of transistors on a microchip doubles about every 2 years, though the cost of computers is halved"



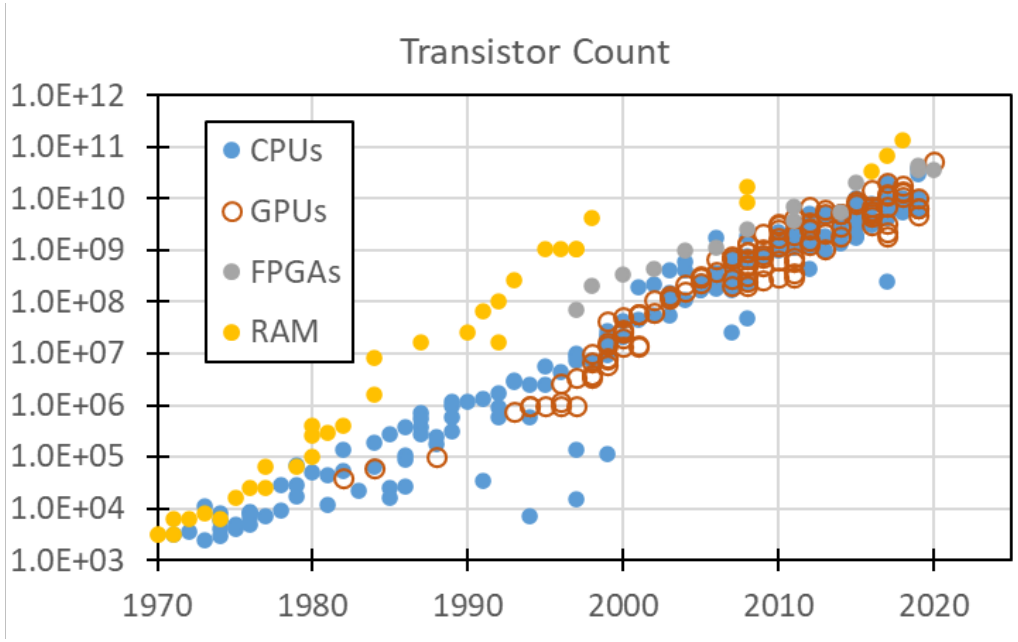


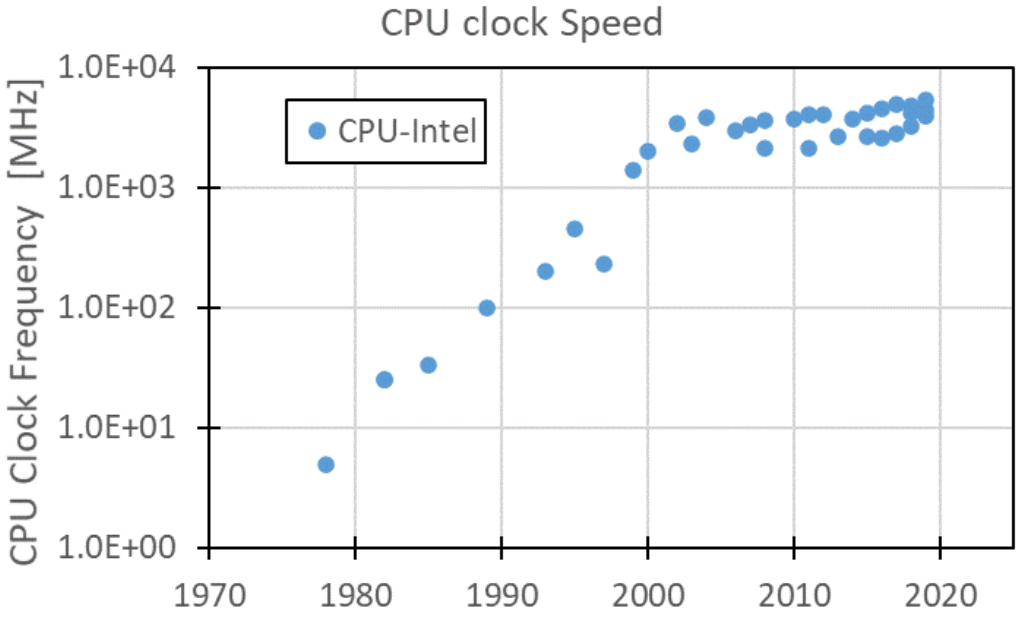
From H. F.-W. Sadrozinski, "Applications of Silicon Detectors", IEEE Trans. Nucl. Sci., Vol. 48, No. 4, (2001), 933

Industrial trends

- Transistor count (and many other parameters) have been pushed very hard for a long time. This required special technologies, e.g. multi-core and multi-chip combinations.
- The Moore's Law, predicted to be dead many times, appears to be still alive

This does not mean that "everything is exponential". The clock speed has been nearly flat for last ~20 years.



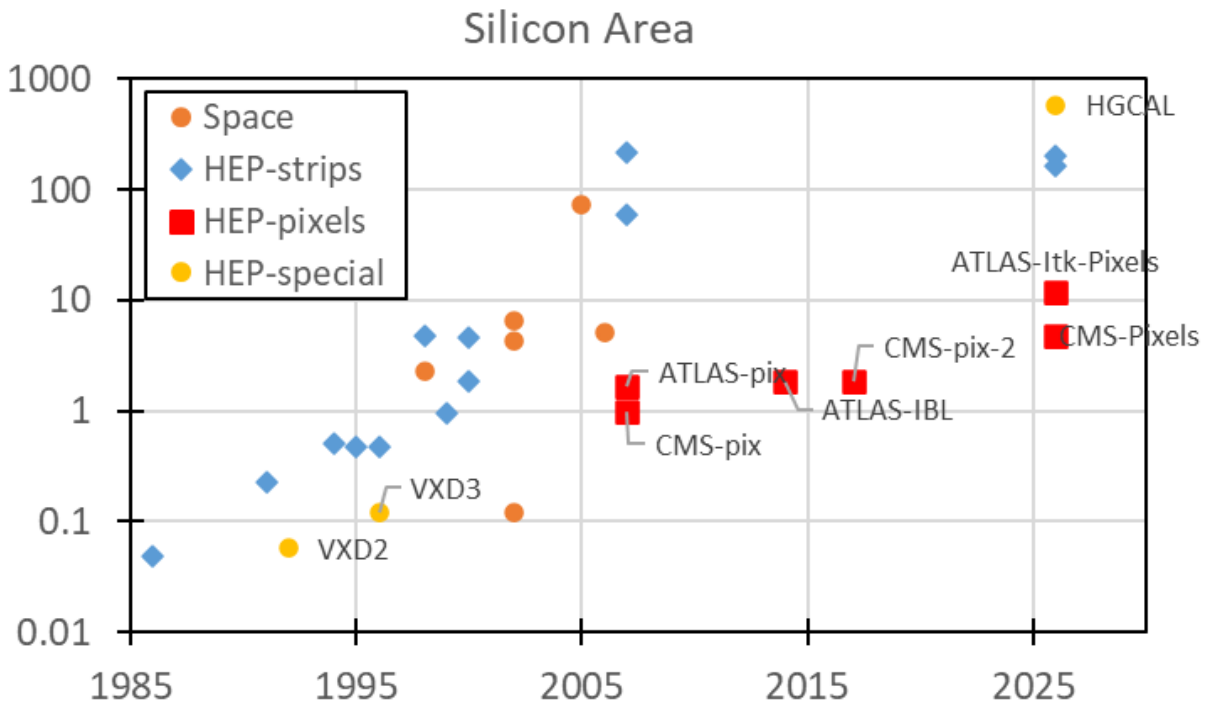


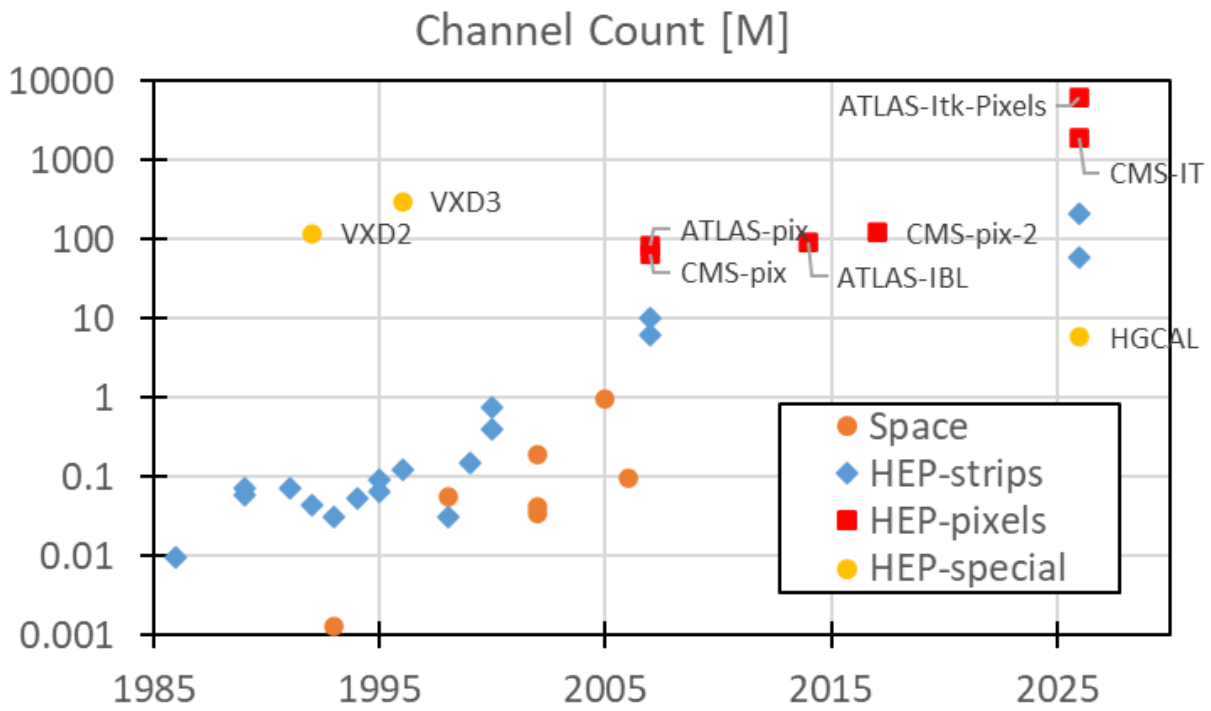
Consequences of Industrial trends

- Do the modern processing nodes directly benefit the technology we use?
  - The cutting edge is ~7 nm. For LHC upgrades 65 nm and 130 nm nodes are used.
    - The smaller feature sizes become expensive quickly (at least now).
    - The analog performance is near-optimal for the current nodes.
  - The miniaturization of the transistor size is helpful for the digital part… if more local intelligence is needed.
- Chip packaging and integration:
  - Multi-chip integration techniques might be useful.
- Importantly, the industrial priorities have been changing. Instead of raw "CPU power" the trends now are power efficiency, multi-core designs, specialized functions (video, image processing, neuromorphic computing)

Updated Trends

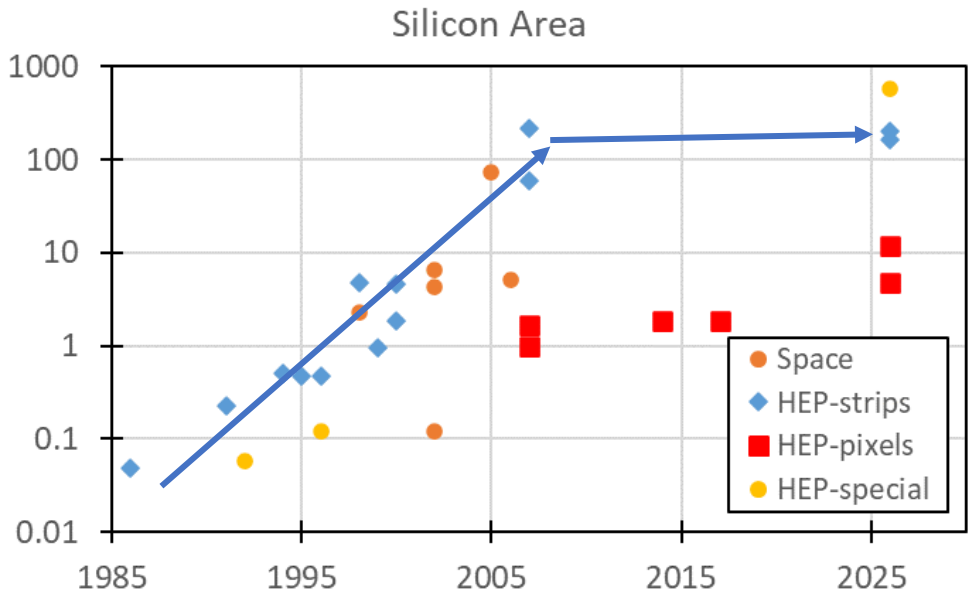
- A (partial) update of the trends
  - Could/should improve the plots, but think the tendencies are clear.
  - Added pixels and “special cases” (CCD, pads)

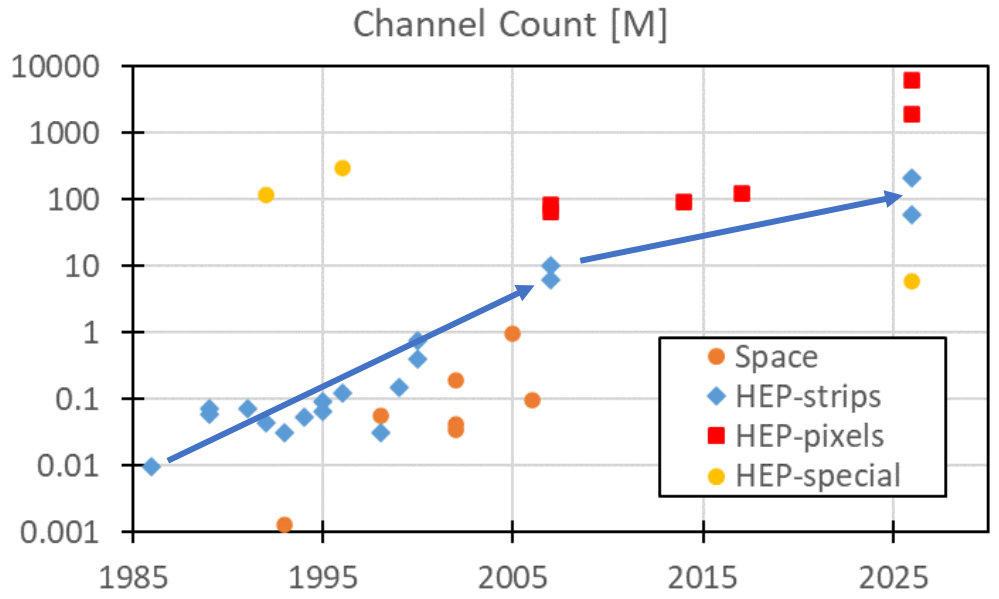




Features: Strips

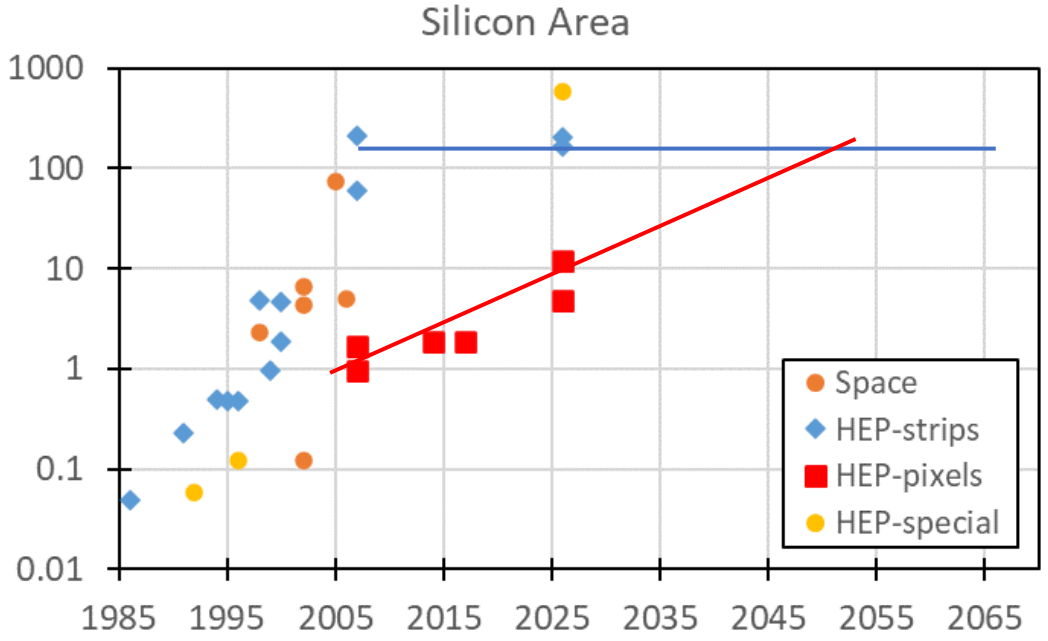
- Strip system features:
  - Had a rapid rise of strip area and channel count, as the Si vertex detectors increased in scope and displaced the gaseous trackers.
  - Tracker area plateau'ed (currently dominated by strips). Expect this to continue:
    - We are probably not going to make "trackorimeters" with O(1000) layers and O(10,000) m2, although this could have some benefits.
  - Number of channels continues to rise, but slower (better segmentation)

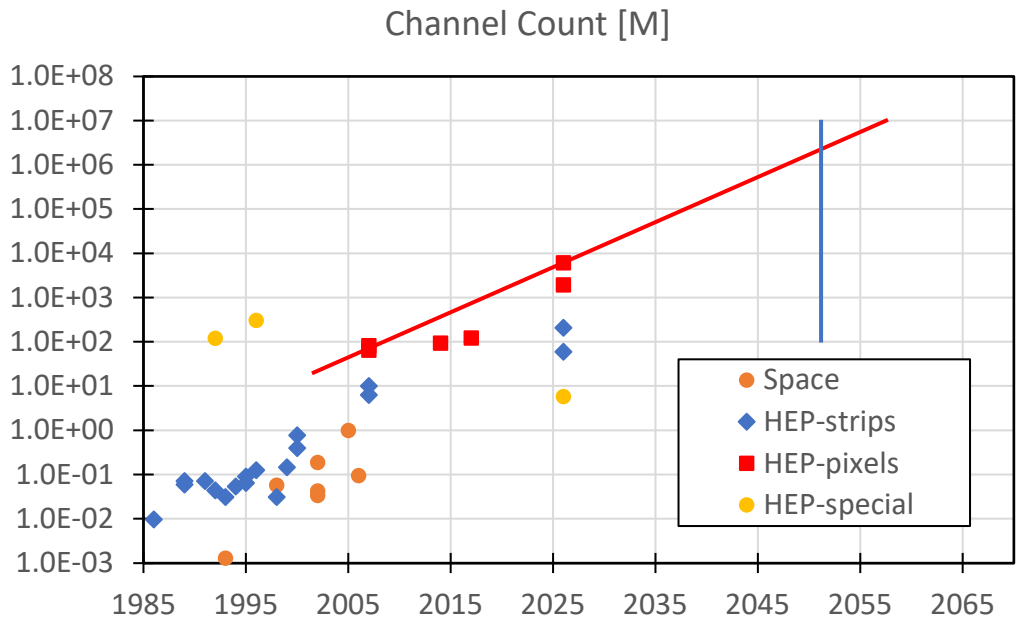




Features: Pixels

- In some sense, pixels are where the vertex detectors used to be at the beginning of ~~time~~ silicon:
  - Continued increase in area and channel counts.
  - Somewhat muted, probably due to hadron collider constraints: power, material budget.
  - The rise has been ~**x1.2** per 2 years and ~**x1.6** channels in 2 years.
- There is an opinion that the next tracker (post-HL-LHC) will be pixel-only.
  - At nominal trends this may happen in ~2050, with a few Tera-channel system.



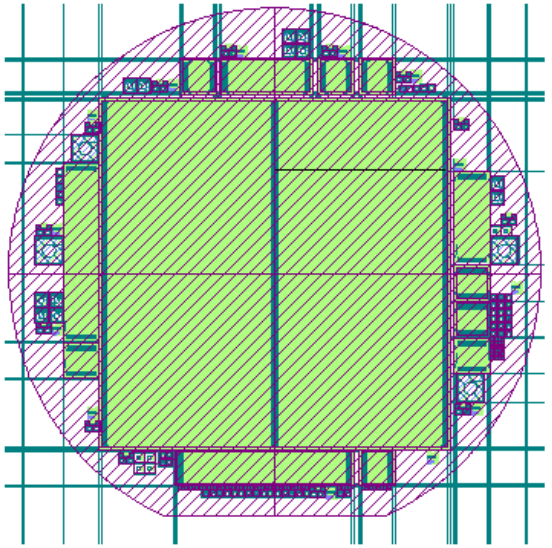


Replaceability

- It seems the upgrades/replaceability were easier in early days.
- Was difficult in LHC era, however the updates have happened and are being planned for:
  - ATLAS-IBL added an innermost pixel layer
  - CMS replaced entire pixel system
  - Both upgraded pixel systems are planned for replaceable inner layers during HL-LHC operations
- Believe the upgrades will be a part and parcel of the future, to either copy with radiation effects or take advantage of a better technology.
- A “continuous replacement” can take care of a lot of issues.

Example with Infineon

- A massive effort over many years: 1st publication in 2013 [1], and still publishing [2]
- A strong participant in CERN-lead market survey for tracking sensors, due to the early R&D jointly with CMS Vienna group.
- Cancelled participation in HEP projects in 2018, during on-going ATLAS submission.
- Thought to come **very** far. Were likely 1 submission away from commencing production.
- The long time scale is driven by **design → layout → fabrication → testing → irradiation → testing** cycle. Takes at least 1.5 years (longer during R&D), and one needs several iterations.



[1] M. Dragicevic, *et al*, "Qualification of a new supplier for silicon particle detectors", NIM A 732 (2013) 74–78

[2] J.Fernández-Tejero *et al*, "Microelectronic test structures for the development of a strip sensor technology for high energy physics experiments", NIM A, in print, https://doi.org/10.1016/j.nima.2020.163971 .

Timescales

- Think that FE ASIC development cycles are similar to sensors (Different aspects of design and layout are stressed: usage of CAD tools to address complexity, instead of design rule development based on device physics understanding and testing)
- “Services” may need a significant time as well if they are “pushing the envelope”, e.g. “microscoping X0”, high readout BW, new heat dissipation technologies.

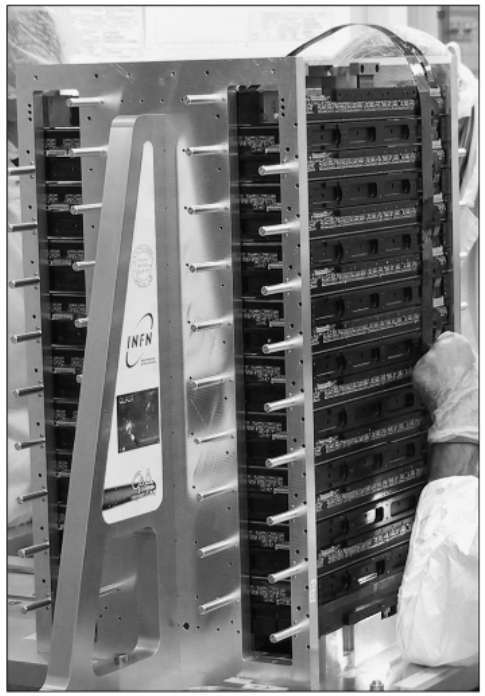
Conclusions from the development:

1. Even for “traditional” trackers most components are niche items, tailored to the experiment’s requirements. They often come with a single-source solution.
2. The development cycles are long.
   - The only way to shrink them is by sacrificing either complexity or quality/performance. Seems a no-go.

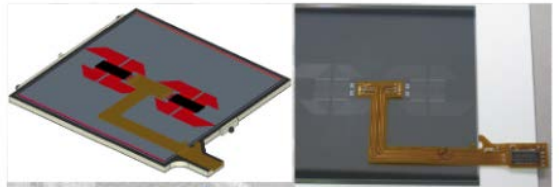
Future colliders

- European strategy decision to priorities the e+e- collider has a huge impact on the future trackers.
- Hadron (“discovery”) machine would imply:
  - Even higher radiation hardness (e.g. further 3D-pixel development)
  - Hence more cooling
  - Likely further segmentation (pixelization), data rates
- Electron machine implies precision studies:
  - Somewhat relaxed interaction rate
  - Extreme radiation length optimization
    - Can be a competition b/w silicon and gaseous tracking
    - Would have to reduce power a lot, to avoid active cooling

Low-power examples



- GLAST/Fermi LAT “Tracker-converter” [1]:
  - Had to be designed for space, hence low-power: 160 W, 3 orders of magnitude less than for LHC experiments.
  - Exploited long shaping time and “only” 880,000 channels. And 10 kHz trigger rate.
  - Still, had 74 m^2 area!
- Linear collider trackers contemplated some similar schemes, e.g.:
  - Long ladders (~1m) readout at the end with long shaping time (2ms) readout [2]
  - But also “system on a chip” with reading out strip sensor via pixel FE chip to reduce X0 [3]
  - In both cases the idea was to exploit ~1% duty cycle to achieve passive cooling
- The trick with FCC-ee style experiments would be to achieve the low-power, low-X0 instrumentation *without* power cycling.
  - Perhaps may involve special materials to achieve passive cooling
  - Will certainly involve ASIC power optimization
  - Might require replaceability of the trackers if radiation damage becomes an issue?



[1] W.B. Atwood et al, “Design and initial tests of the Tracker-converter of the Gamma-ray Large Area Space Telescope”, Astroparticle Physics 28 (2007) 422-434

[2] K. Collier et al, “Microstrip electrode readout noise for load-dominated long shaping-time systems”, NIM A 729 (2013) 127-132

[3] J. Brau et al, “KPiX - A 1,024 Channel Readout ASIC for the ILC”, NSS/MIC 2012 / RTSD 2012, 1857-1860

HV/HR-CMOS

- Anticipate this was covered elsewhere, hence only brief overview:
  - Example of monolithic sensors with embedded readout
  - Taking advantage of either electronics on top of epi layer, or HV process with higher-resistance structure to create a thin depletion layer.
  - The signal is “small” compared to heterogeneous systems, but the so is the noise when pixelized.
  - Nascent technology, developed a lot for ATLAS pixel (almost got there).
  - Used for mu3e experiment, ALICE.
- Can be implemented as a very thin, *O(50 um),* layer, hence *O(0.05%)* X0 without support.
  - Suspect will have to be used for the FCC-ee pixel/vertex part. Unclear about the rest of the tracker.
- May also be helpful for calorimetry (if implemented as a *uniform* (XY) radiation length).

HV/HR-CMOS references

- A compilation done for BRN:

current projects	status	Area [m^2]	Rad hardness [neq/cm^2]
ATLAS strips	not for installation	large	2.0E+15
ATLAS pixels	not for installation	3	1.0E+15
Mu3e	to be installed in the experiment	2	
STAR	Installed	0.16	1.0E+12
ALICE	being installed?	10	1.7E+13
CERN RD50	on-going generic R&D	N/A	Varying
CLIC vertex	on-going R&D		small

- References:

1 T. Hemperek, "Overview and perspectives of HR&HV CMOS", Pixel-2016
2 Signal vs resistivity and fluence: B. Hiti et al, "Charge collection in irradiated HV-CMOS detectors", NIM A 924 (2019) 214
3 CLIC study: N. A. Tehrani et al, "Tracking performance and simulation of capacitively coupled ...", NIM A 931 (2019) 214
4 ATLAS pixels, AMS: I. Peric et al, "A high-voltage pixel sensor for the ATLAS upgrade", NIM A 924 (2019) 99
5 ATLAS pixels, TJ: M. Dindal et al, "Mini-MALTA: Radiation hard pixel designs...",
6 Mu3e: H. Augustin et al, "MuPix8 — Large area monolithic HVCMOS pixel detector...", NIM A 936 (2019) 681
7 STAR, Mimosa28: G. Contin et al, "The STAR MAPS-based PiXeL detector", NIM A 907 (2018) 60
8 ALICE, TJ: M. Mager et al, "ALPIDE, the Monolithic Active Pixel Sensor for the ALICE ITS upgrade" NIM A 824 (2016) 434
9 G. Iacobucci, CERN seminar, Oct 04, 2019

The echo-system

- The current arrangement of (almost) only-huge experiments is unhealthy:
  - Social factors with training the next wave of experts, especially with long timescales.
  - A big impediment for the introduction of the new technology:
    - Large-system construction is focused on risk mitigation (rightfully so, when building some of the most complex systems on Earth!)
    - But this means less room for experimentation.
    - Ideally have a mix with interchange of ideas. (Or SBIR-style process specifically for investigating new ideas at the level of commissioning and exporing in realistic settings.)
    - (In my opinion) this was one of the main reason for HV-CMOS eventual omission from ATLAS tracker, in spite of very promising results and existent chips – long-term experience was not there.

Conclusions

- Have our own (empirical) “Moore-like” laws, but not directly tied to the leading edge of the industrial developments for the consumer marked
  - Too many unique requirements
- The scope/area of the trackers may be at the limit, but anticipate a qualitative changes – increase in pixel scope, emphasis on power efficiency
- Certainly a significant development time is required, given the complexity, (likely different) optimization than the current generation, and technology advancement.
- The preference for electron collider(s) in the future stresses low-mass precision trackers, hence passive cooling options
  - No-active-cooling pixelated system would be ideal, if feasible.
    - Note can “trade” pixelization for timing resolution, at least for some layers (idea from Linear Collider developments)
  - Anticipate monolithic technology to play an important role
- Ideally would prefer to see a healthy balance of large and small experiments, both for training and technology-proofing purposes.