

Sep. 14th, 2020

Overview of Triggering at CMS

Mu-2e TDAQ System Workshop

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Princeton University

Overview of Triggering

CMS

Physics Overview

Multi-level Data Processing

Triggering Architectures

Detectors and Algorithms

Hardware in Run 2

Towards the HL-LHC

Algorithms

Hardware

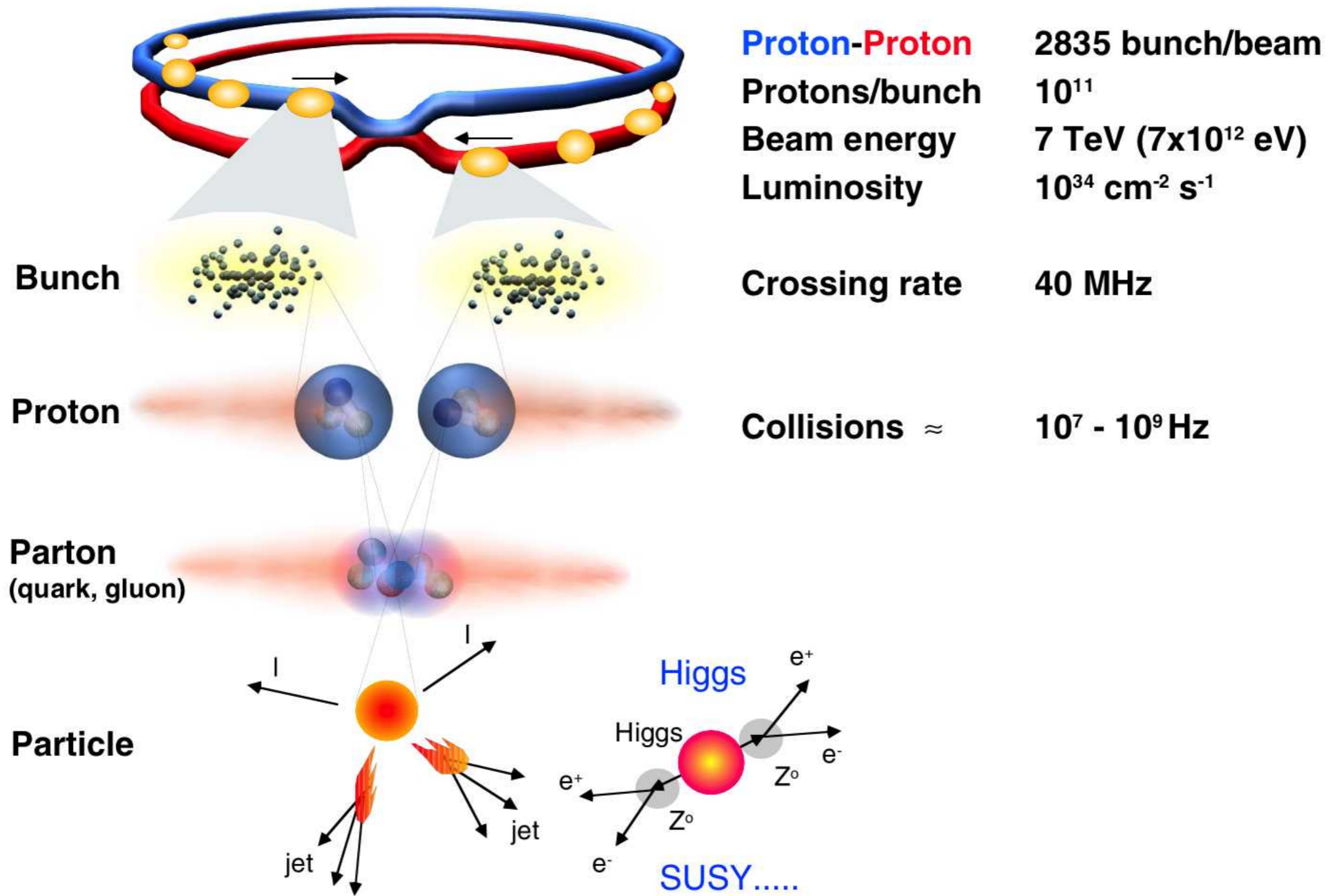
Technology and Development

Sep 14, 2020

Overview of Triggering@CMS

I.Ojalvo





Proton-proton Collisions at the LHC



At $L = 1-2 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$

- 25-50 events/crossing
 - ~ 1 GHz pp collision rate
 - Events contain 25-50 pileup events
- **EWK rate:** 1 kHz W&Z
- **Top Rate:** 10 Hz
- **Higgs:** ~0.1 Hz, H4l: 0.1 mHz

~Output 1 MB/event -> it would also be impossible to store all events

Process and Select Events in Stages

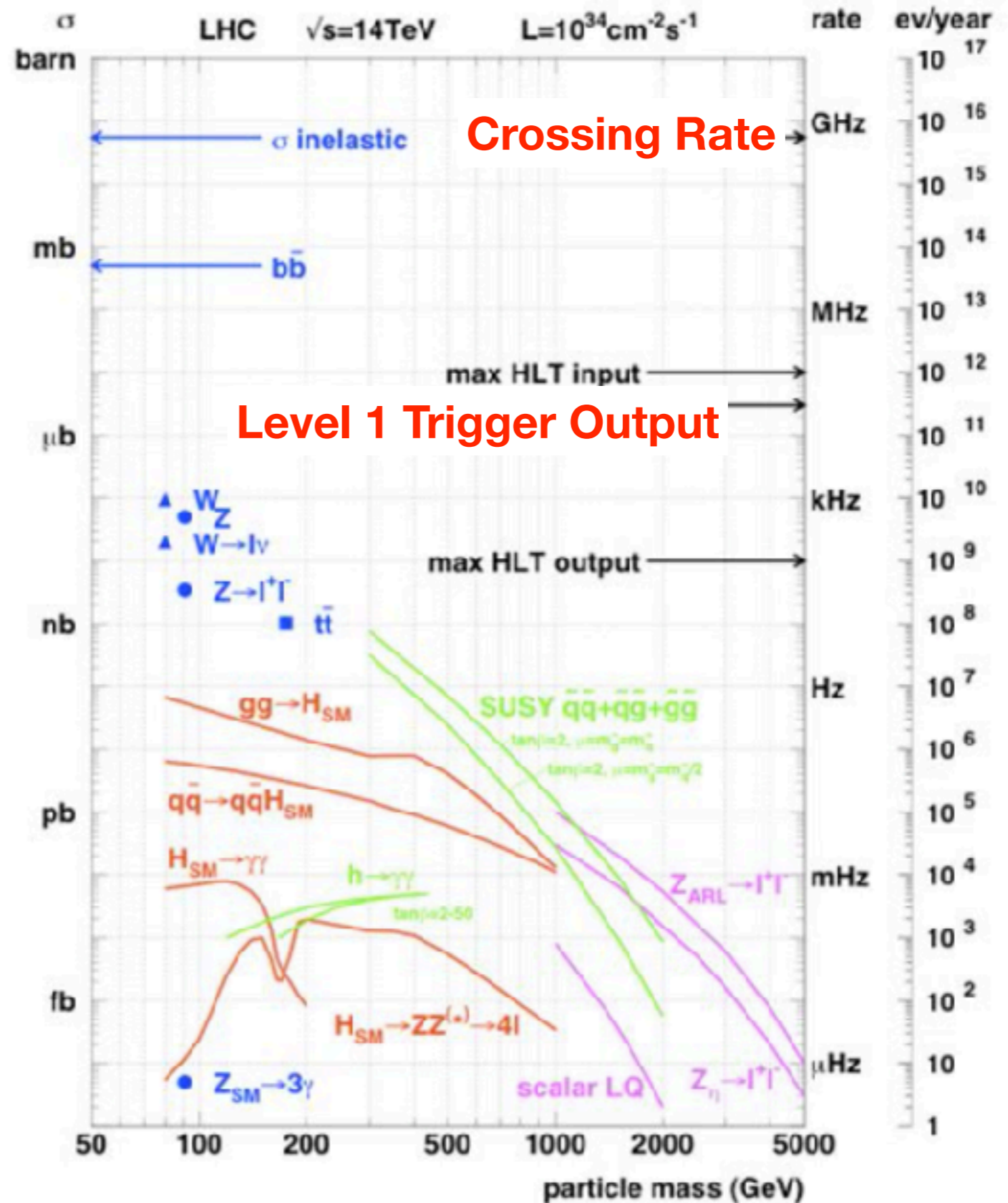
Level-1 Triggers

- reduce 1 GHz to 100kHz

High Level Triggers

- reduce 100kHz to 100's Hz

- Run I/II CMS detector buffers hold each event for ~120BX while the decision to trigger is being made using the Level 1 Trigger System



What Physics Signatures?

Electroweak Symmetry Breaking Scale

Higgs discovery and higgs sector characterization
Quark, Lepton Yukawa couplings to higgs

~40 GeV γ , e, μ



Low P_T b-jets, τ



New physics at TeV scale to stabilize higgs sector

Spectroscopy of new resonances (SUSY or otherwise)
Dark Matter candidate

Multiple low P_T objects



ME_T



Multi-TeV scale physics (loop effects)

Indirect effects on flavor physics (mixing, FCNC, etc.)
Bs mixing and rare B decays
Lepton flavor violation
Rare Z and higgs decays

Dedicated Triggers



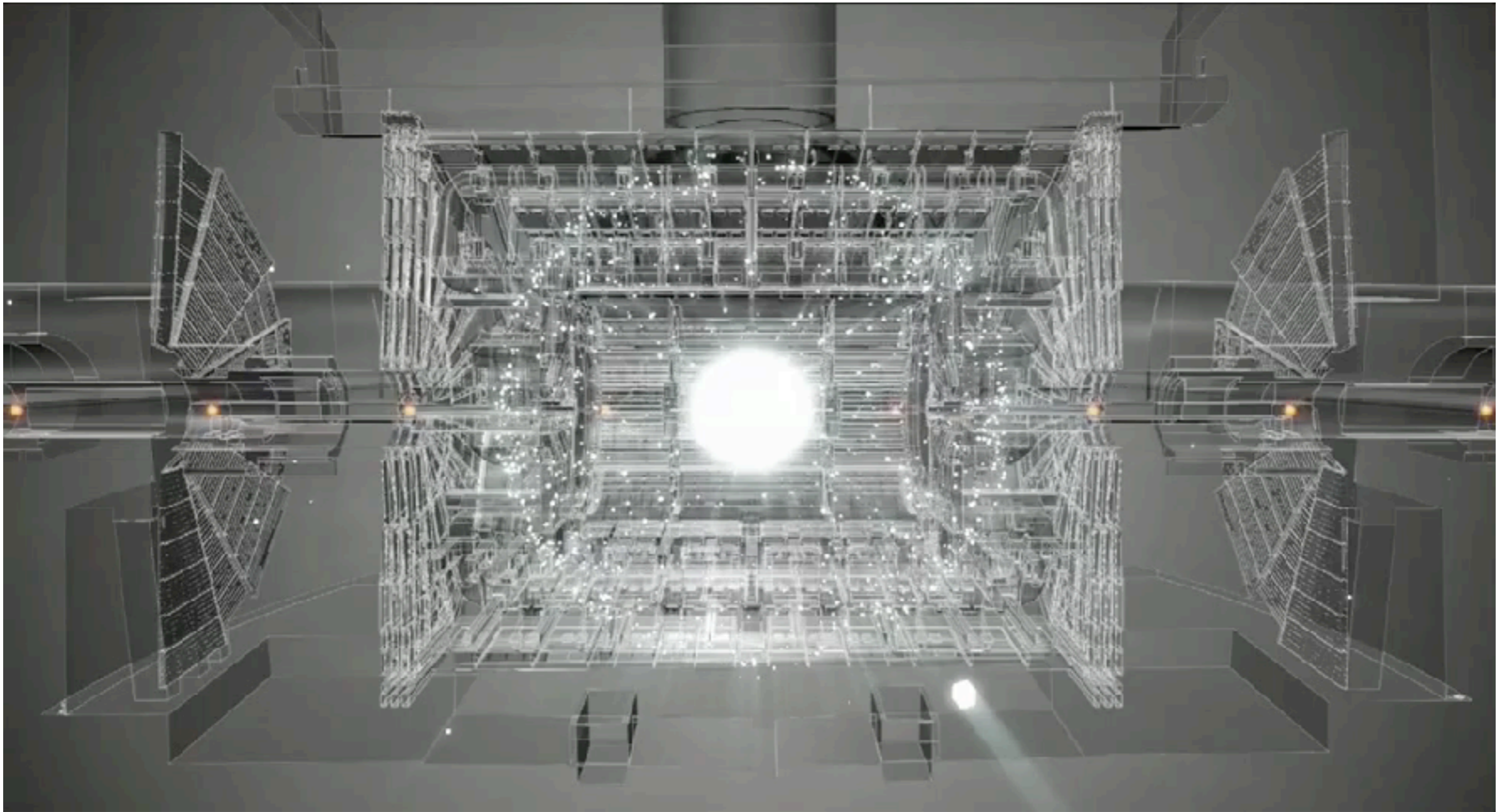
Planck scale physics

Large extra dimensions to bring it closer to experiment
New heavy bosons
Blackhole production

High P_T leptons and photons
Multi particle and jet events



$c = 30 \text{ cm/ns} \rightarrow \text{in } 25 \text{ ns, } s = 7.5 \text{ m}$

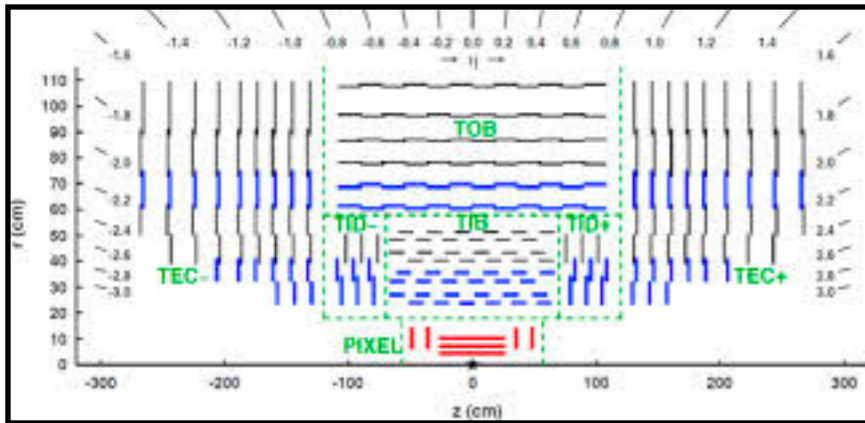


- New Event arrives **every 25ns**
- **Many channels, high occupancy**, searching for only a few **special events**, with a **limited latency**
- ▶ Develop systems which suit both the computing and latency requirements

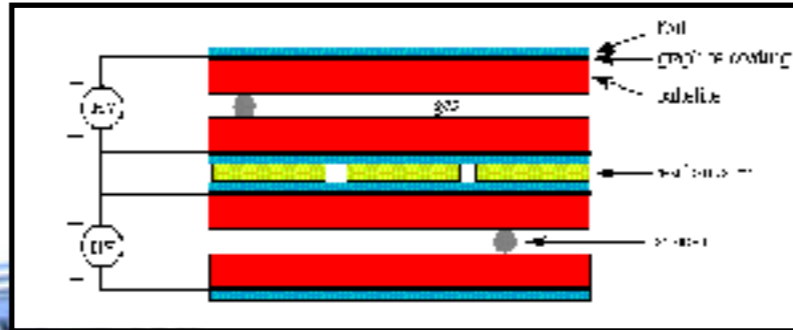


CMS Detector

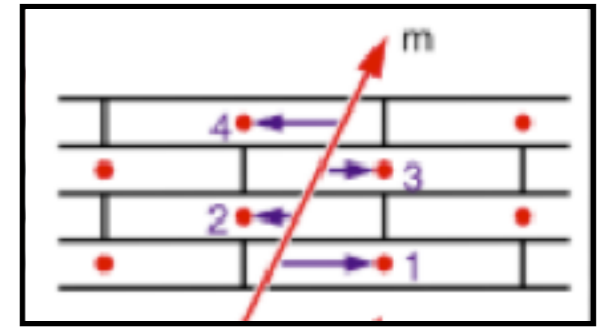
Tracker



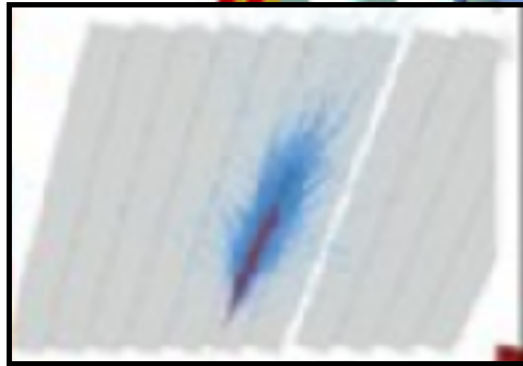
RPC



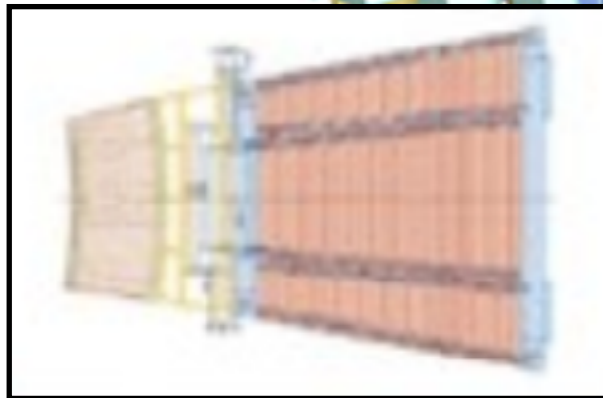
DT



ECAL

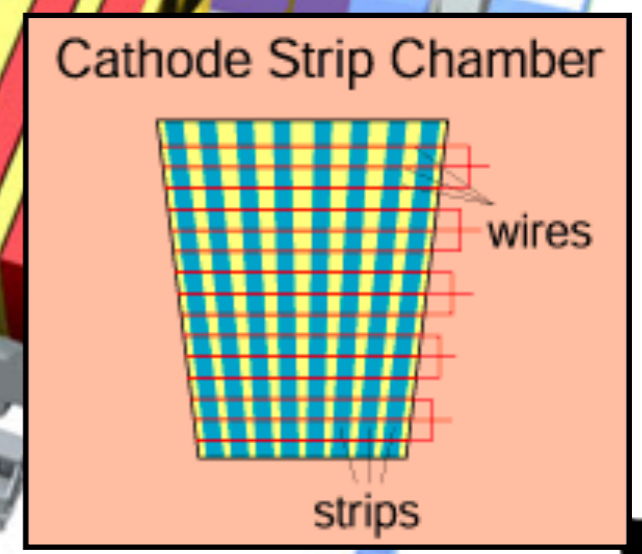


HCAL



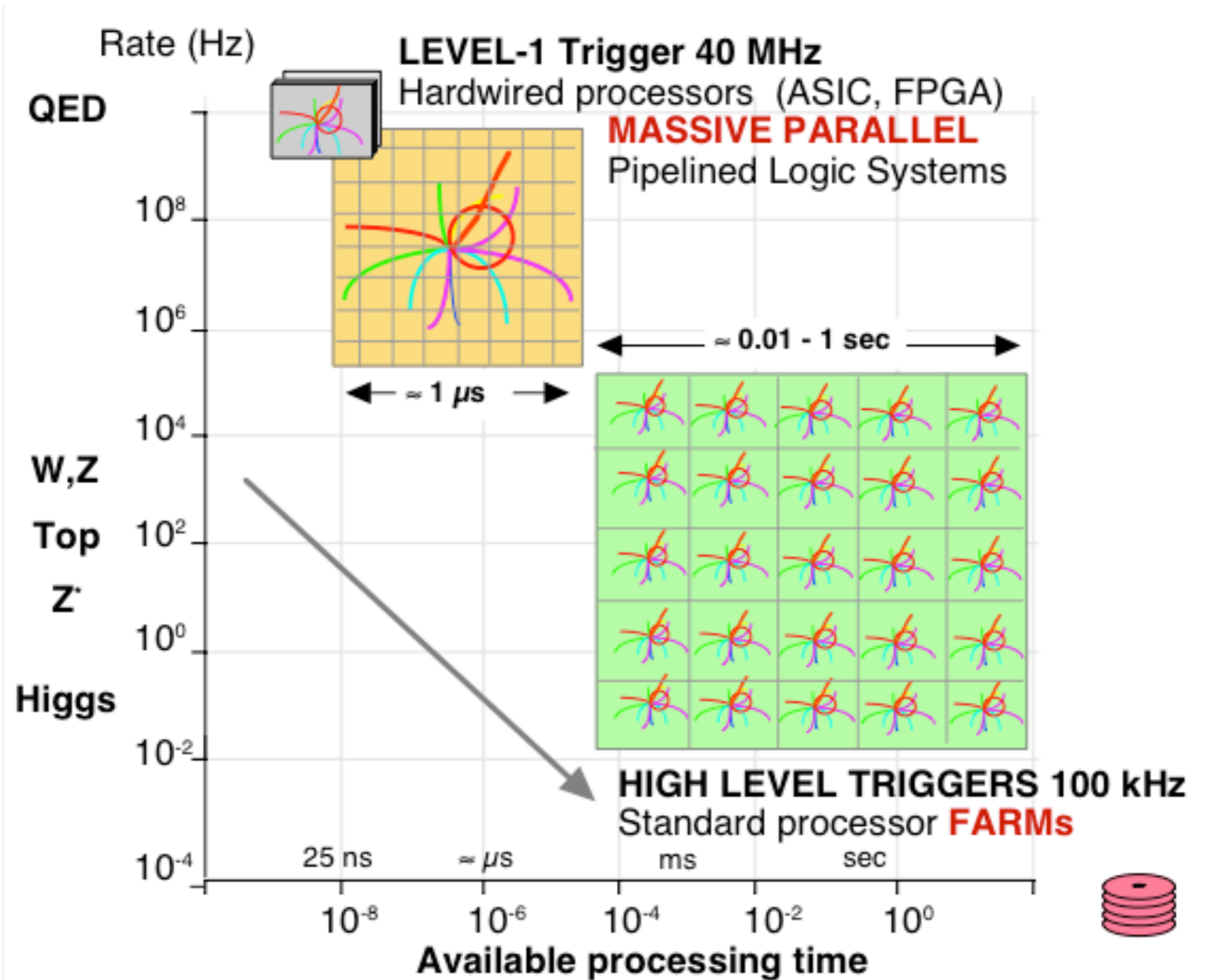
**Super
Conducting
Solenoid**

Total weight : 12,500 t
Overall diameter : 15 m
Overall length : 21.6 m
Magnetic field : 4 Tesla

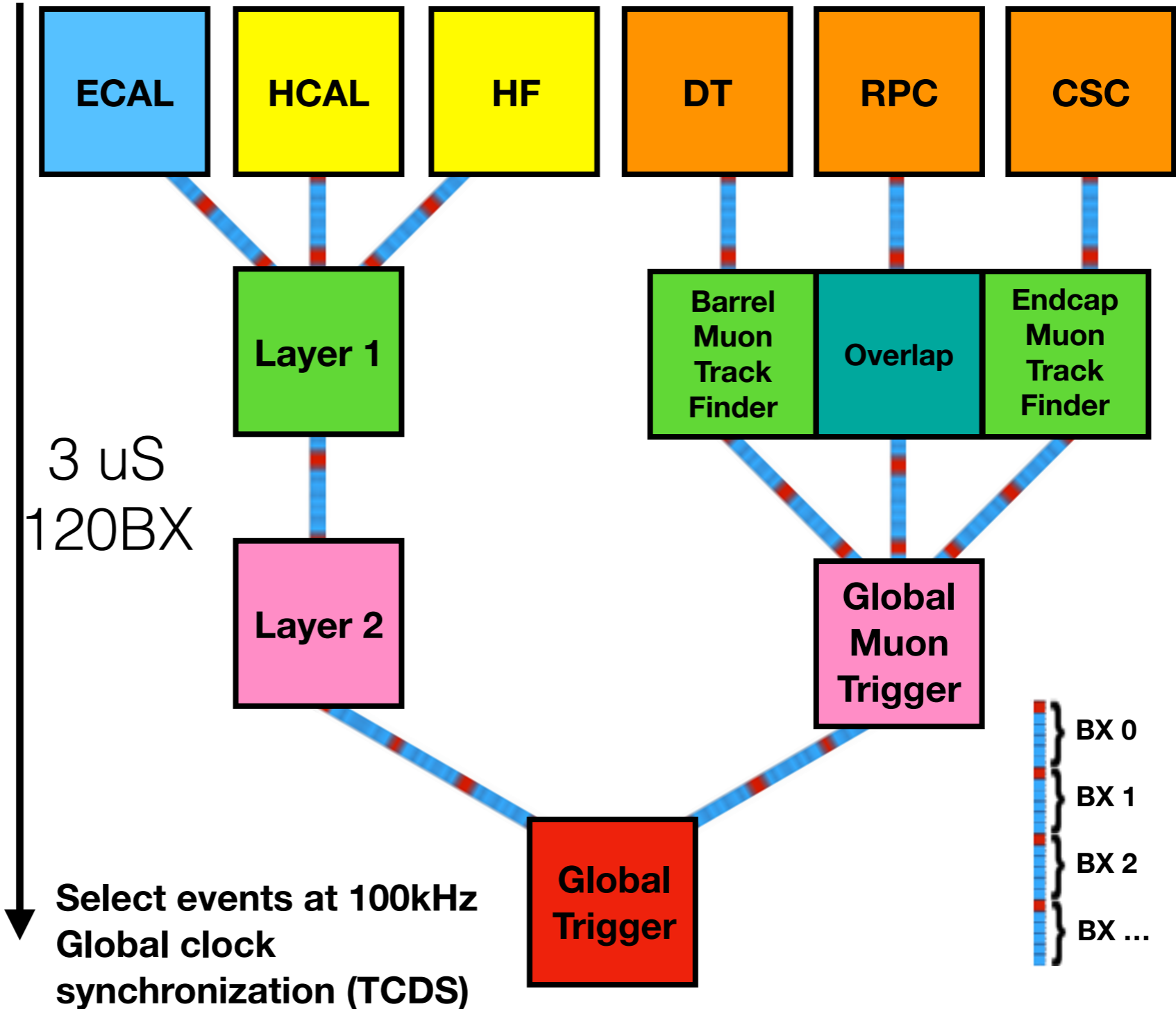
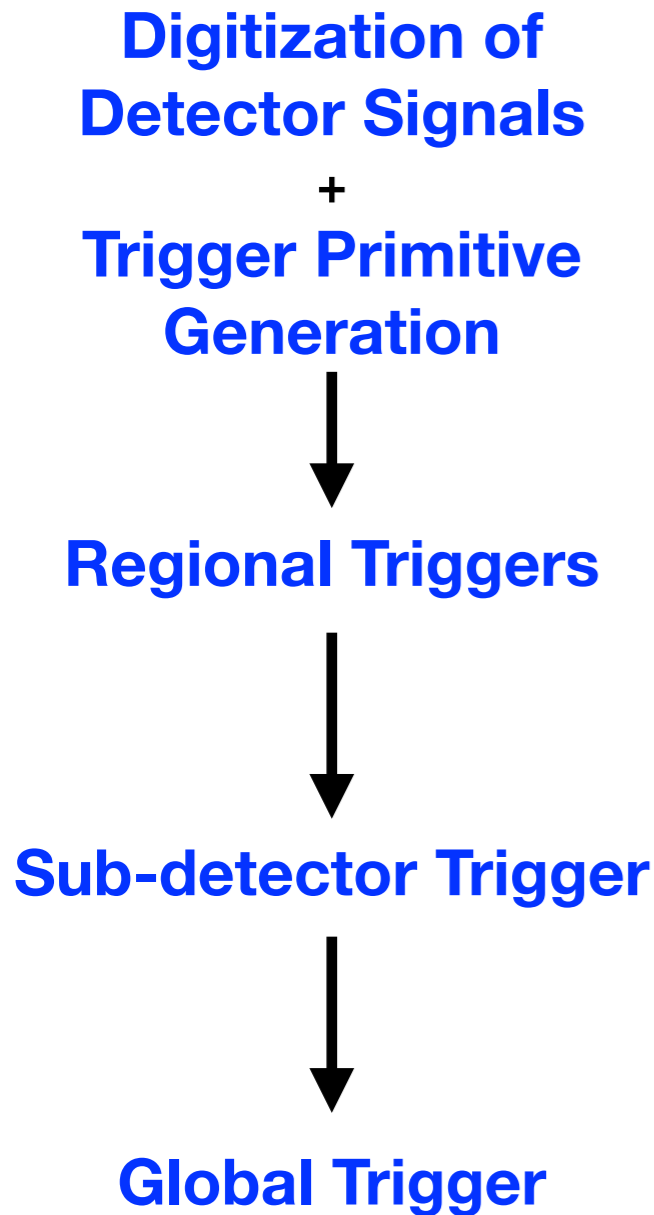


CSC





CMS Level 1 Trigger Data Flow



Pipeline System
Frequency 40MHz
Feed-Forward Algorithms
 - (no backwards loops)
Highly Distributed
Full Event Processed at the GT

Designed on custom built electronics employing high speed links (I/O) and (ASICs +) FPGAs



Data Processing in the High Level Trigger



- Implemented using generic processors
- Muon Systems, Calorimeters and Tracker
- Increase in number of Trigger, algorithms, selections and complexity
- Event Filtering, **Selections are made sequentially: When an event fails a given selection criteria then the processing stops** in order to allow the node to be used by a **new event**

HLT Reconstruction for Taus

Level 2

Narrow CaloJets are formed around “**Level 1 Seeds**”

Level 2.5

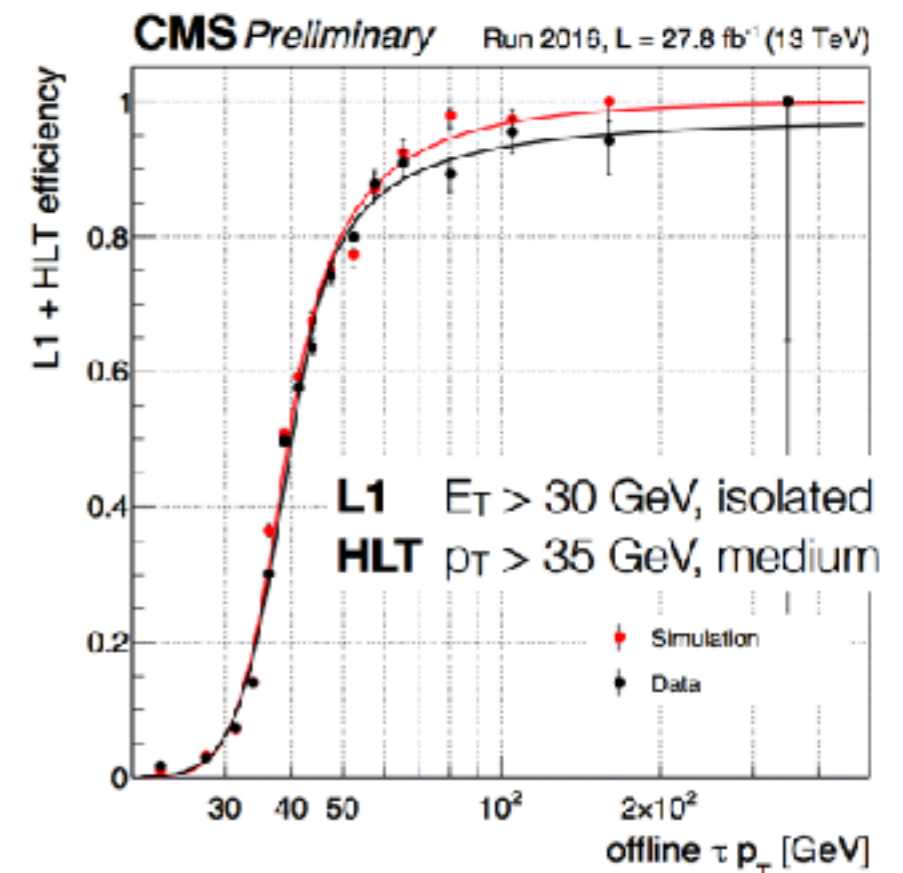
Pixel based Isolation is required around the CaloJet

Level 3

Offline-like **Tau** Reconstruction proceeds with HLT Particle Flow

- ▶ Less stringent than Offline Reco
- ▶ For each step if a minimum requirement (typically p_T or isolation) is not met then processing is **Halted**
- ▶ If all of the **requirements are met** then the **event is saved** for **offline analysis**

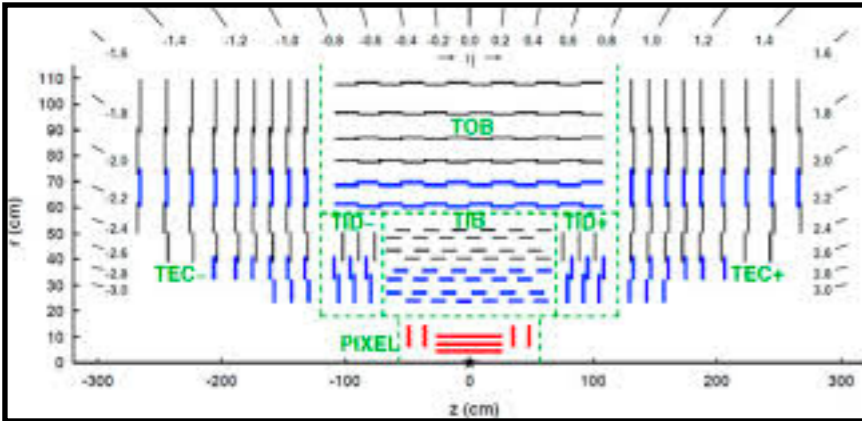
“**Trigger Bit**” Stored Per Event₁₀



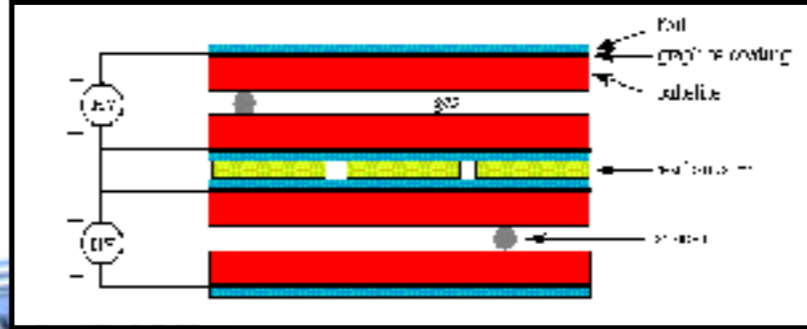
Algorithms

CMS Detector

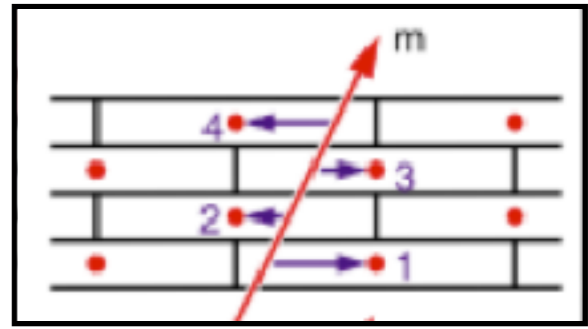
Tracker



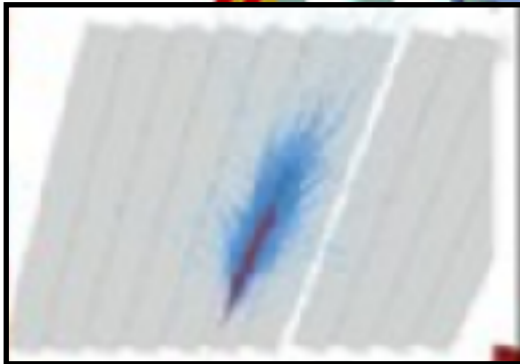
RPC



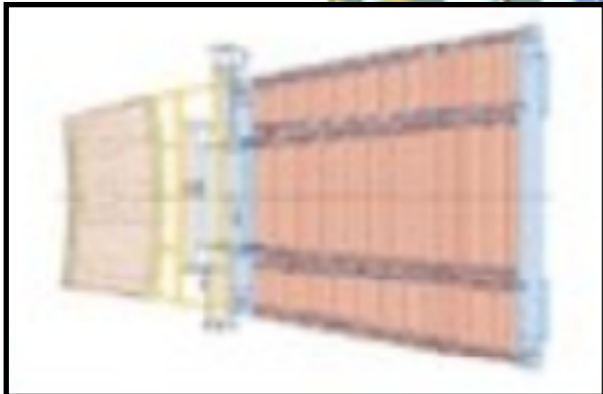
DT



ECAL

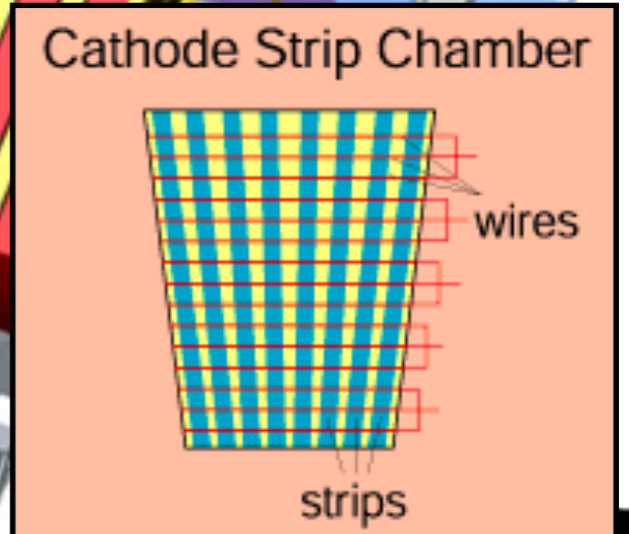


HCAL



Total weight : 12,500 t
 Overall diameter : 15 m
 Overall length : 21.6 m
 Magnetic field : 4 Tesla

**Super
 Conducting
 Solenoid**



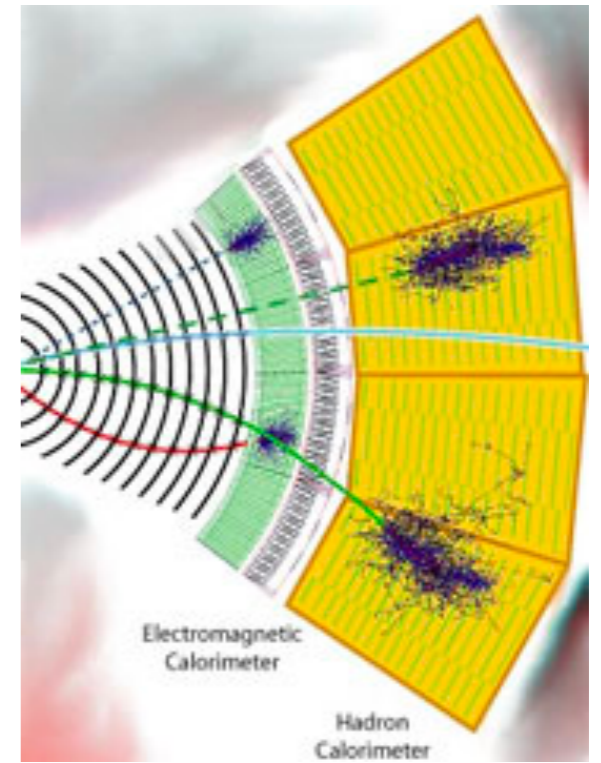
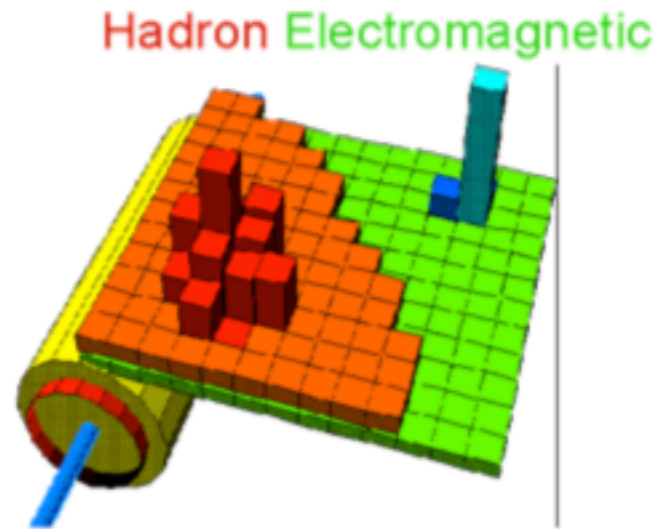
CSC



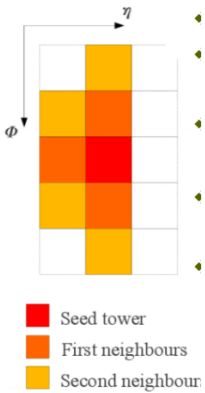
Level 1 Trigger Object Identification: E/gamma Taus



Calorimeter Data input to Level 1 as spatially fixed "Trigger Towers"

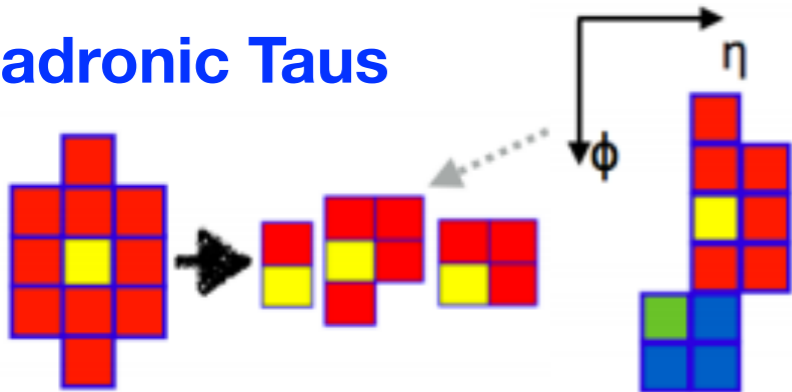


Electrons/Photons

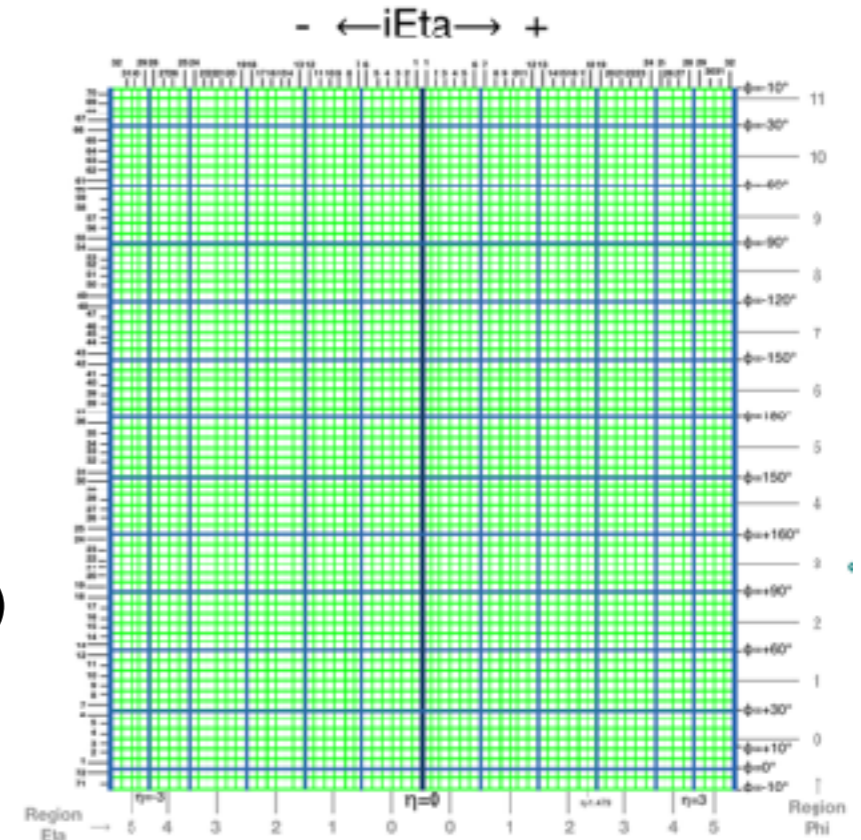


- Clustering around seed tower with local energy maximum (> 2 GeV)
- Neighboring energy deposits clustered (>1 GeV)
- E/H and Isolation

Hadronic Taus



- Clustering same as E/G
- Shape finding (Decay Modes)
- E+H and Isolation

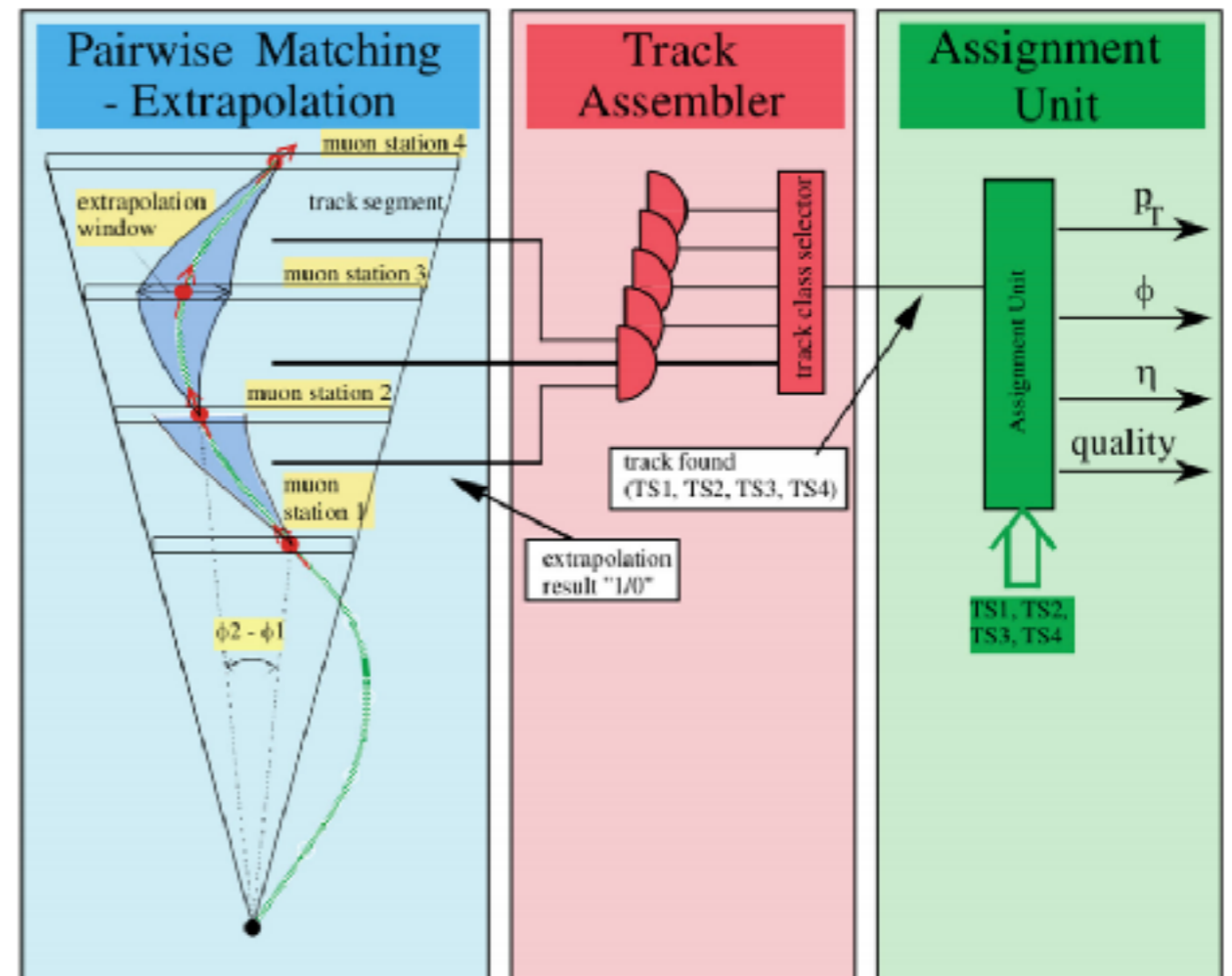
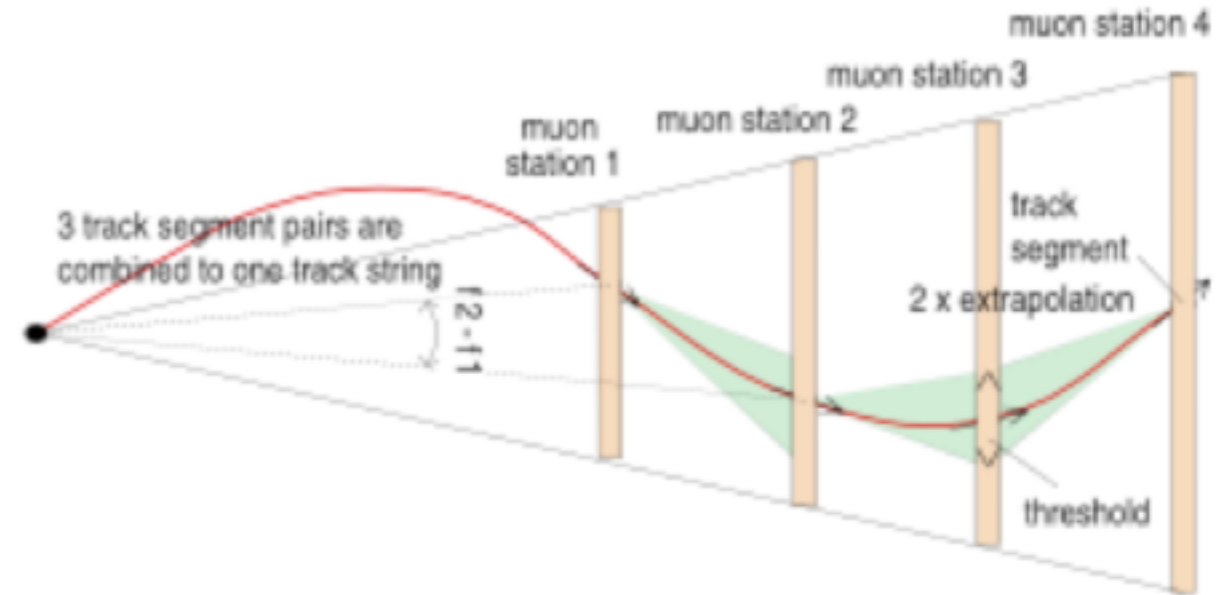


Level 1 Trigger Object Identification: Muons

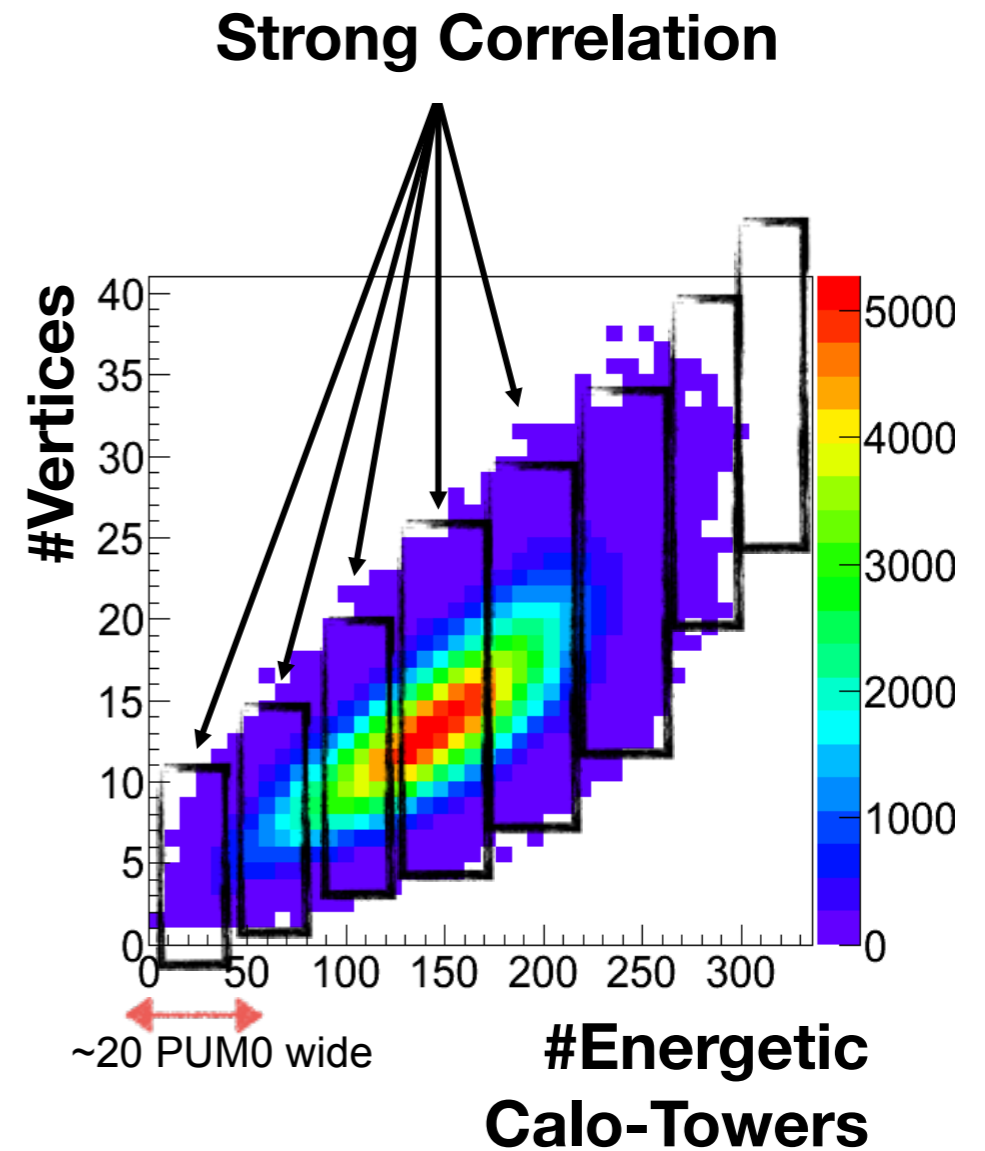
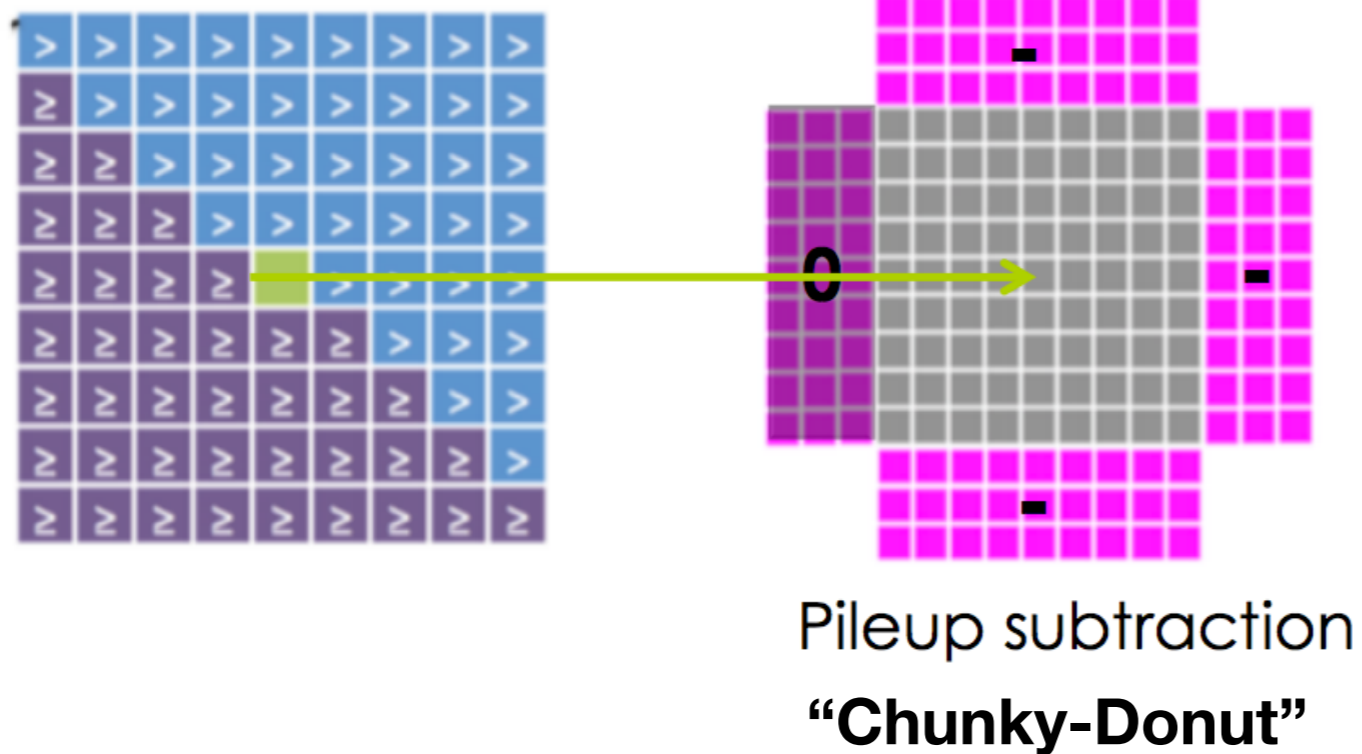
Muon Hits must be matched station by station and is dependent upon Muon Momentum

- **Input segments from Muon Chambers** forwarded to Barrel, Endcap, Overlap Muon track finders
- **Search** for track segments in adjacent modules
- **Track is assembled**
- **Kinematic assignment** based on Look Up Tables

Requires Memory to Store Patterns
Fast Logic for Matching Segments
- **FPGAs are Ideal**



Jets and Sums Require Regional Information



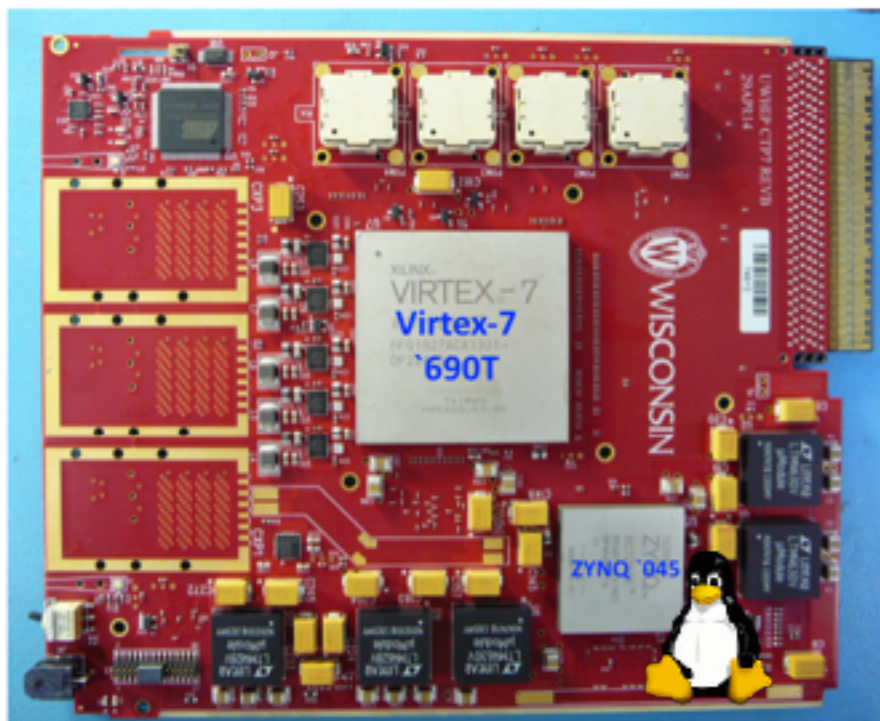
- Pileup Algorithms attempt to identify the number of p-p collisions per event and correct for the extra “noise”
- MET/Sums constructed from Summed Jets/Calo-Towers

Trigger Hardware

Trigger Hardware Run II



31 Rx and 12 Tx Frontpanel Optical 10G links on MiniPODs

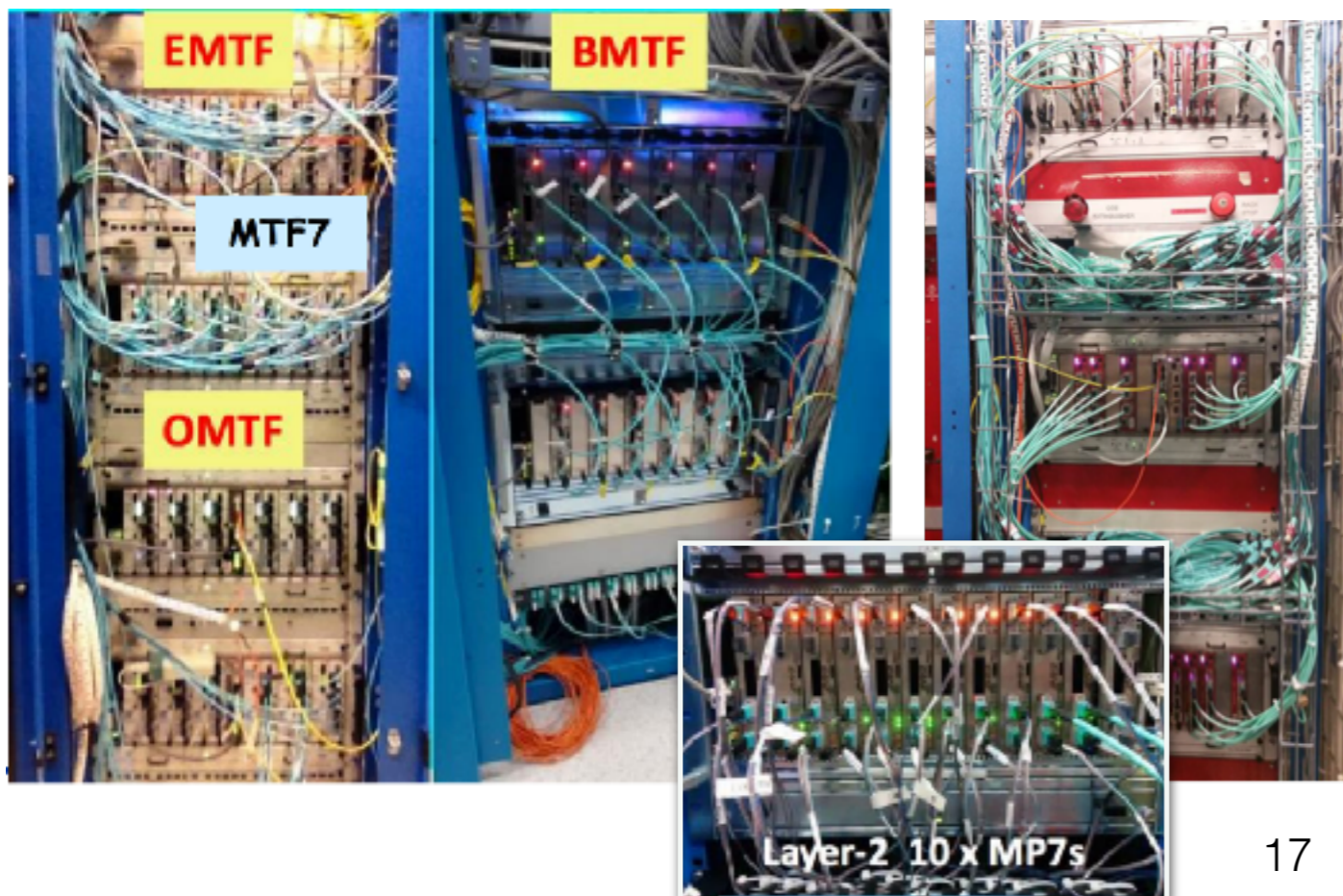


CTP7

13 GTH
Back-plane
Tx/Rx links



MP7



- ▶ Virtex 7 FPGAs used as main processor
 - ▶ Half a Million Logic Cells, Up to 500MHz Clock Frequency, MultiGigabit transceivers
 - ▶ Up to 10Gbps optical links
- ▶ uTCA Form Factor and infrastructure
- ▶ DAQ, Slow Control, Monitoring



Reprogrammable Hardware

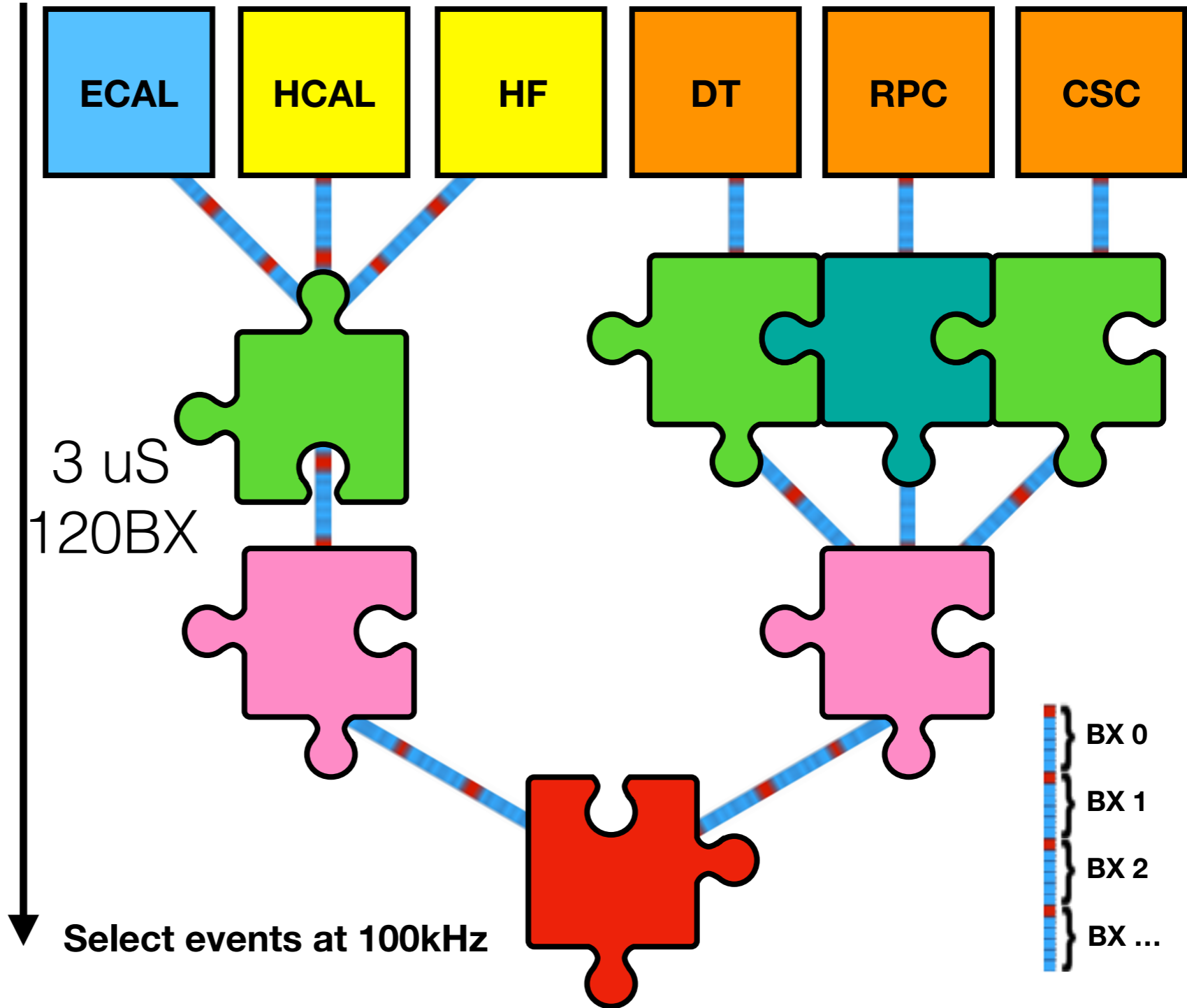
Digitization of
Detector Signals
+
Trigger Primitive
Generation

????

????

Global Trigger

Flexible Design
Standardized Technology
Reprogrammable Logic
Space for New Algorithms



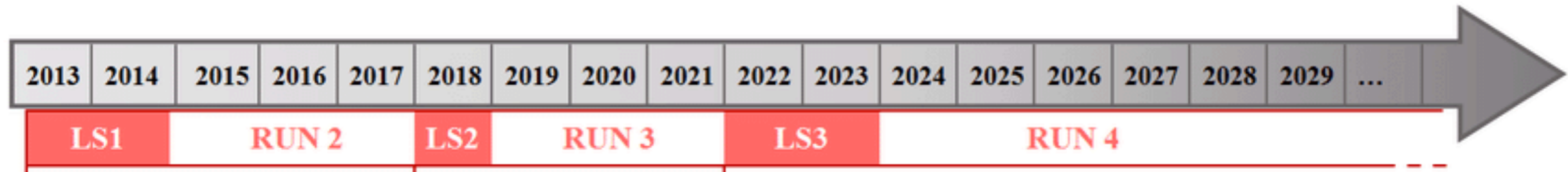
Trigger System for HL-LHC



Motivations for an High Luminosity-LHC

The LHC plans a program of Increased Luminosity over the next 10 years in order to increase collected data rate

- ➔ More data will lead to more precise measurements and searches with finer sensitivity

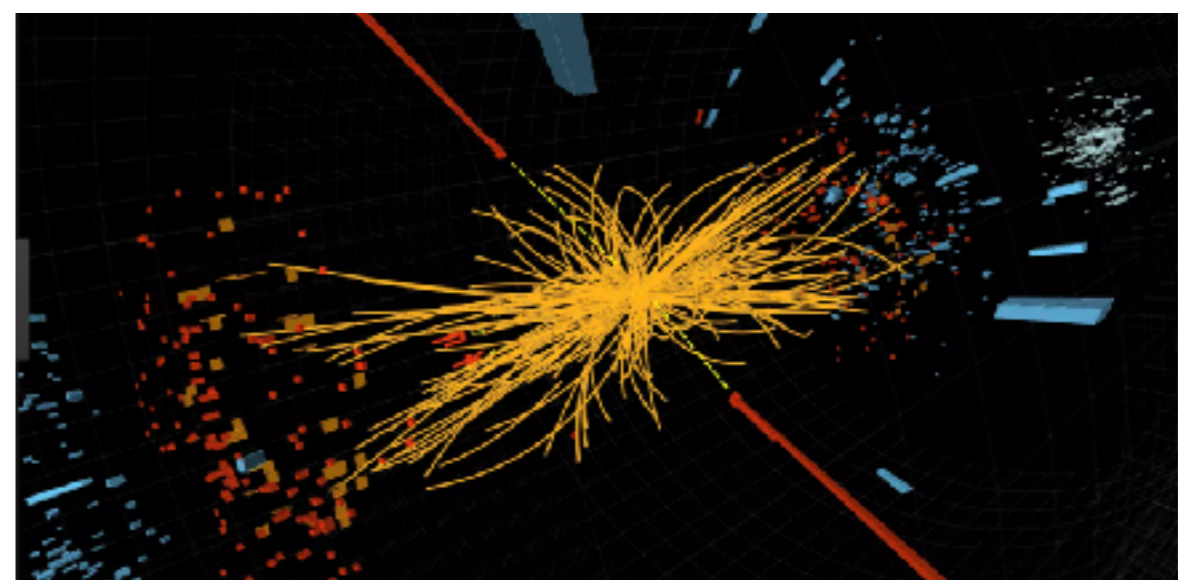
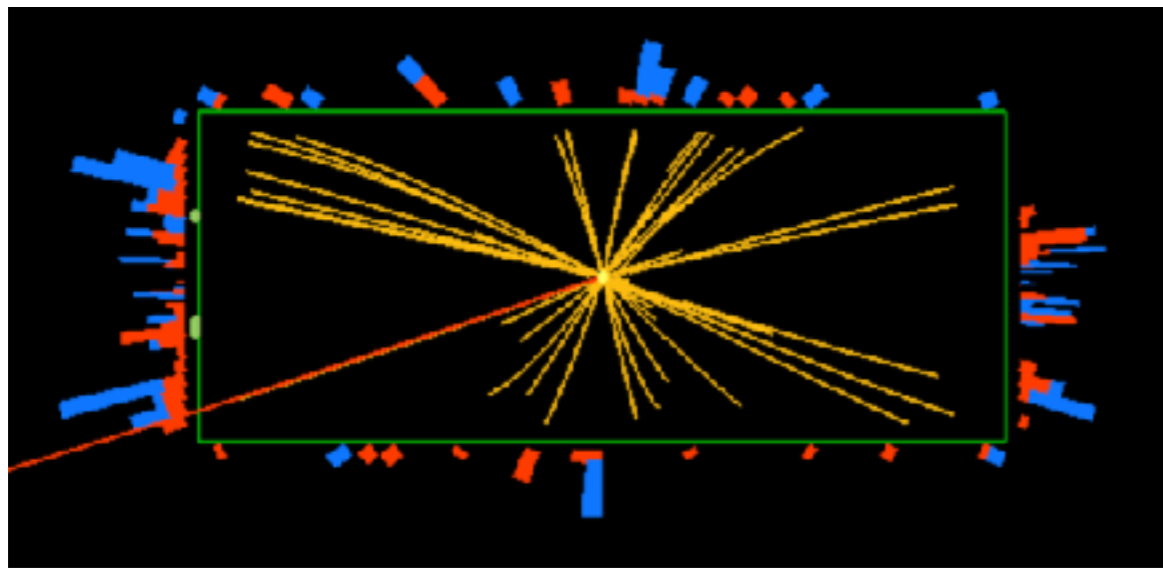


2011

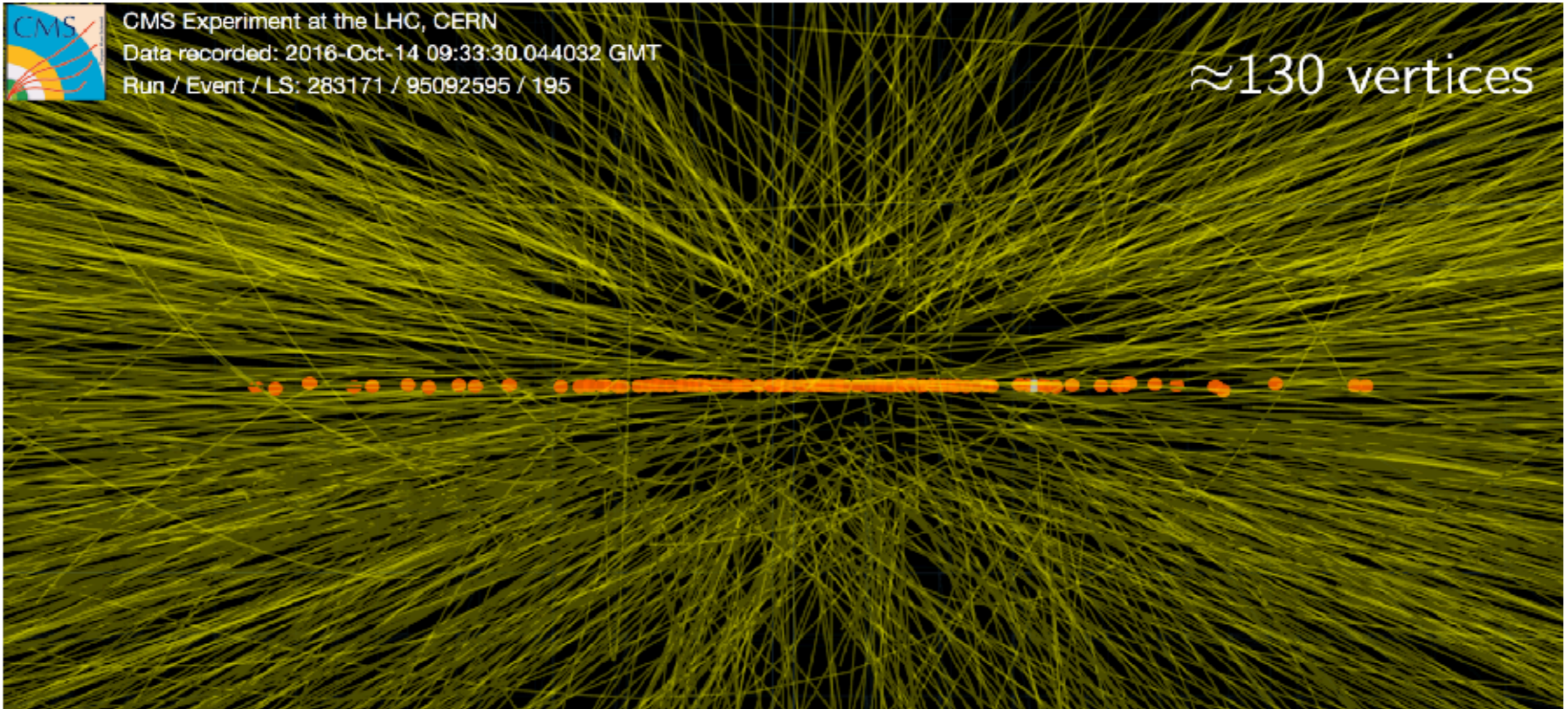
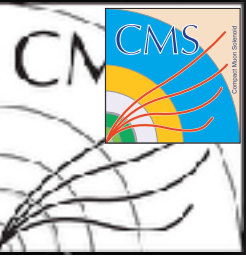
$\sim 0.5 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$

2016

$2 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$



Challenges of the High Luminosity LHC (HL-LHC)



Event from Special Run in 2016, HL-LHC 150-200 vertices

- ▶ Due to the **increased instantaneous luminosity**, the HL-LHC represents a significant challenge for **Event Reconstruction** and **Primary Vertex** identification
- ▶ Improvements to the CMS detector are planned to replace portions of the detector which will have **degraded due to radiation damage** and to **upgrade the detector** in order to **maintain a strong physics program**



CMS Phase 2 Upgrade

New Tracker

- Coverage up to $|\eta| < 3.5$
- Tracks available at Level 1 Trigger
- Radiation tolerant - high granularity
- - less material

Muons

- Replace DT FE Electronics
- Complete RPC coverage in forward region (new GEM/RPC technology)
- CSC replace FE electronics for inner rings

Barrel ECAL

- Replace FE Electronics
- Crystal-level information at L1

New Endcap Calorimeters

- High granularity (HGCal)
- Segmented depths

Barrel HCAL

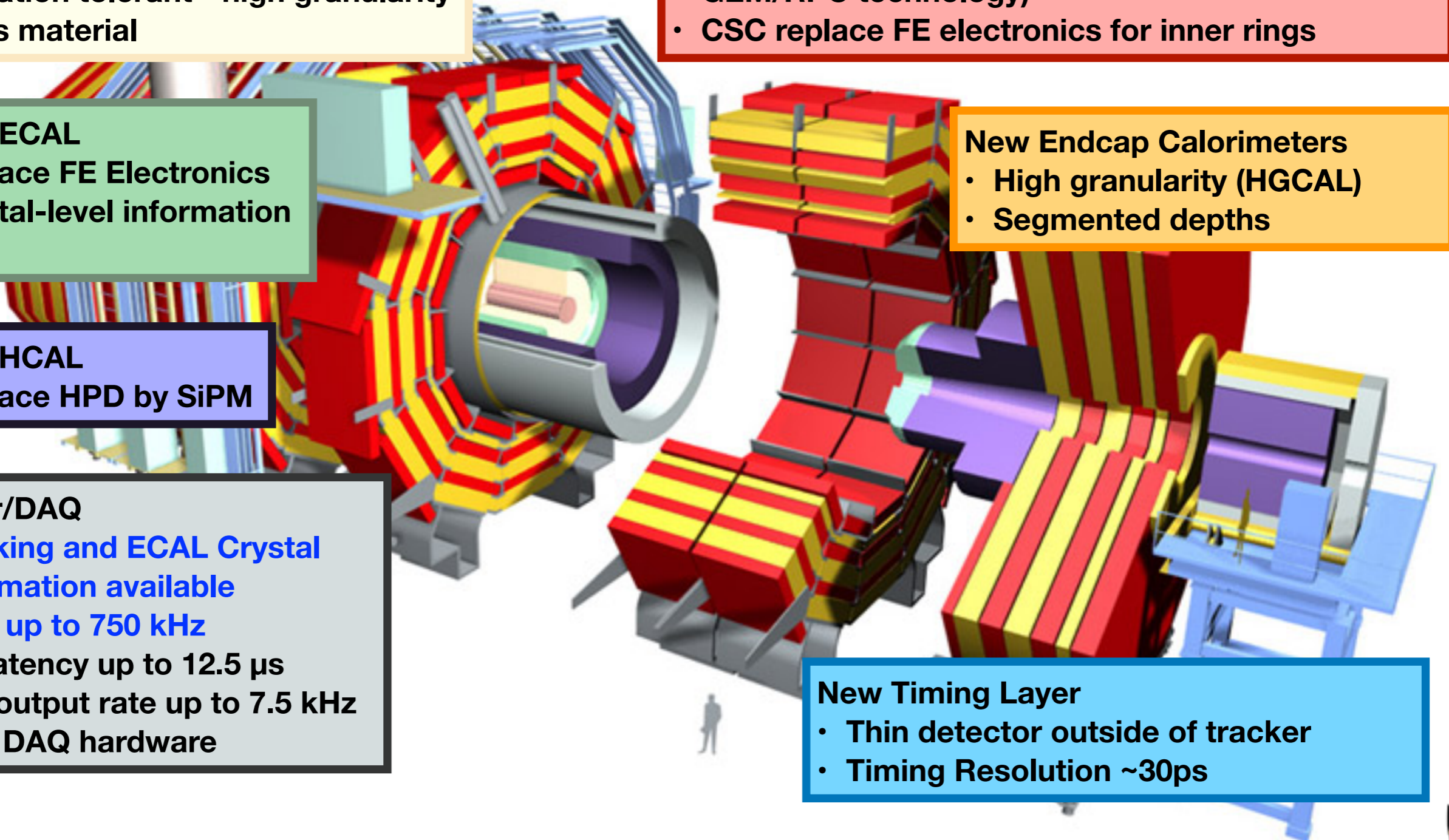
- Replace HPD by SiPM

Trigger/DAQ

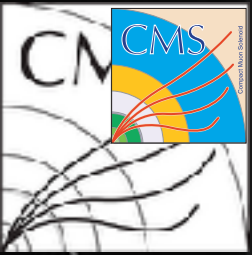
- Tracking and ECAL Crystal information available
- Rate up to 750 kHz
- L1 Latency up to 12.5 μ s
- HLT output rate up to 7.5 kHz
- New DAQ hardware

New Timing Layer

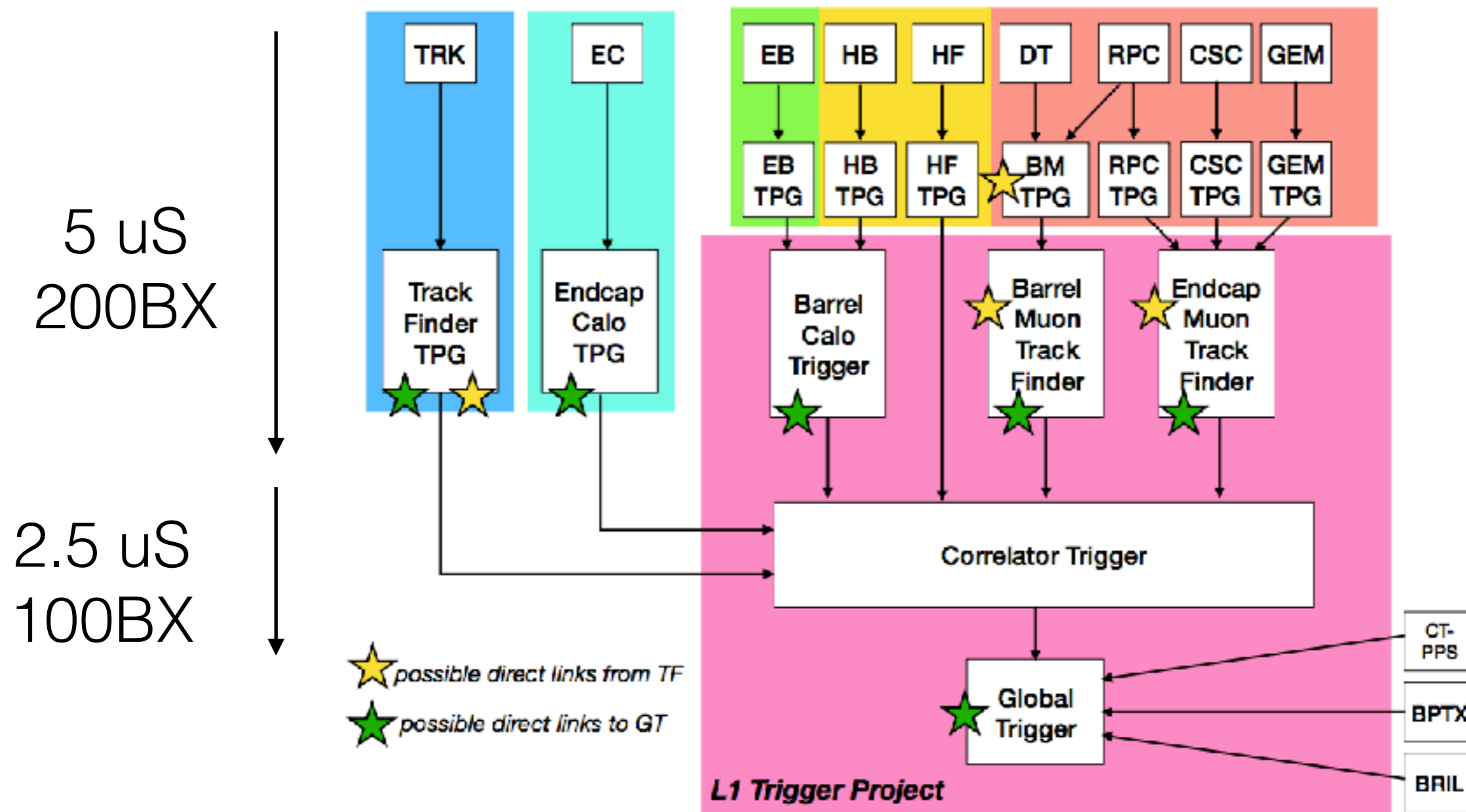
- Thin detector outside of tracker
- Timing Resolution ~ 30 ps



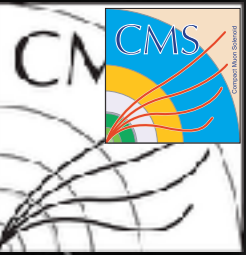
Trigger Design Phase-II (HL-LHC) Upgrade System



- ▶ Tracking system for input, improved ECAL granularity, HGCAL
- ▶ Generate a trigger within 12.5 μ S at a max rate of 750kHz

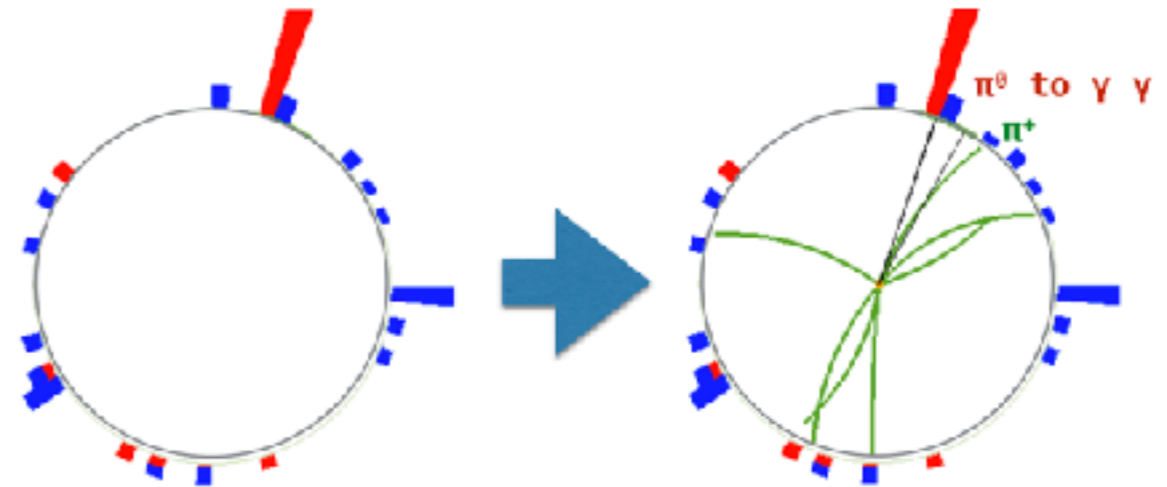


Track Trigger for HL-LHC

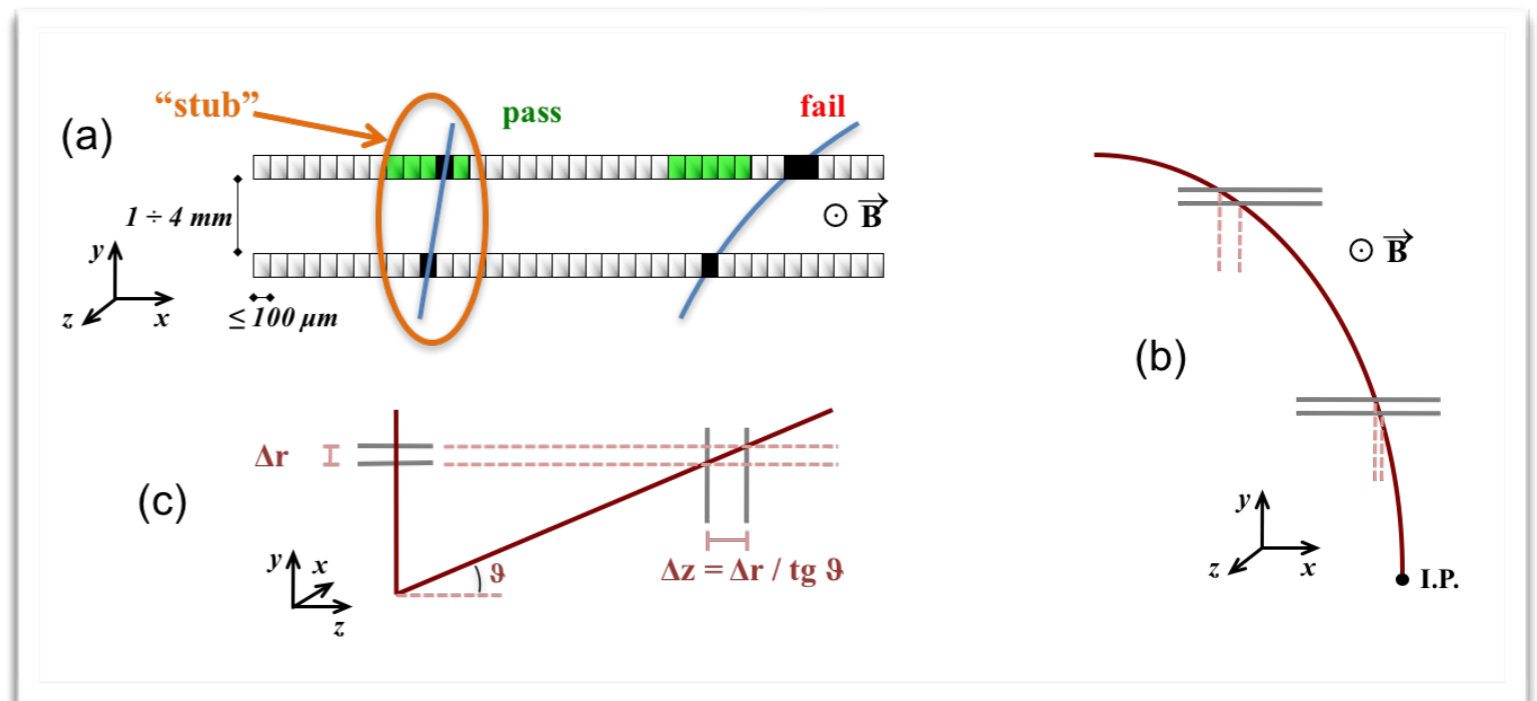
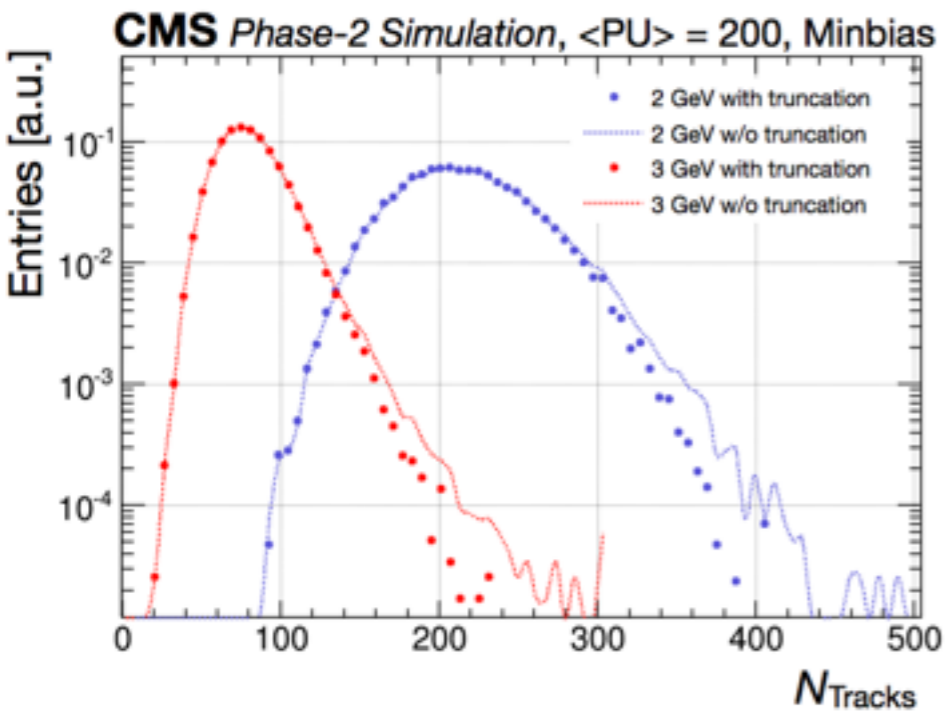


Data from the Outer Tracker included in the Level 1 Trigger

- **Stubs** created by matching layers in the Outer Tracker
- For each hit on an inner layer match to a hit on the outer layer
 - **Local P_T measurement to reduce data rate**



Multiple Technologies/ Architectures Explored

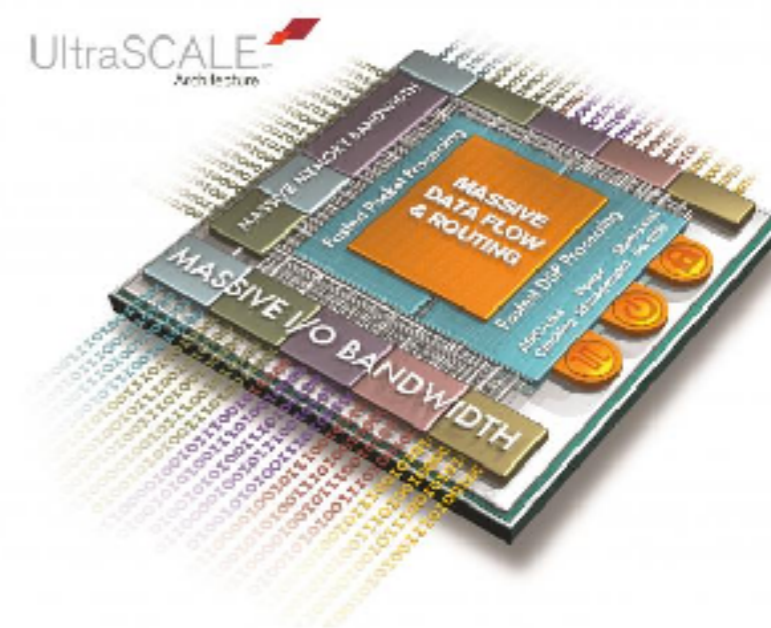


Phase II Trigger Upgrade will bring offline reconstruction to Level 1 while increasing flexibility

	KINTEX ⁷	KINTEX ⁷ UltraSCALE	VIRTEX ⁵	VIRTEX ⁵ UltraSCALE
Logic Cells (LC)	478	1,161	1,995	4,407
Block RAM (BRAM) (Mbits)	34	76	68	115
DSP-48	1,920	5,520	3,600	2,880
Peak DSP Performance (GMACs)	2,845	8,180	5,335	4,268
Transceiver Count	32	64	96	104
Peak Transceiver Line Rate (Gb/s)	12.5	16.3	28.05	32.75
Peak Transceiver Bandwidth (Gb/s)	800	2,086	2,784	5,101
PCI Express Blocks	1	4	4	6
100G Ethernet Blocks	-	2	-	7
150G Interlaken Blocks	-	1	-	9
Memory Interface Performance (Mb/s)	1,866	2,400	1,866	2,400
I/O Pins	500	832	1,200	1,456

What is needed?

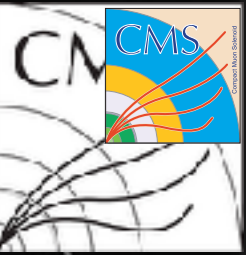
- ▶ Large, multi-purpose **Ultrascale+ class FPGAs**
 - ▶ Industry FPGA size appears to be more than doubling with each generation
 - ▶ Programmable Systems are excellent for improving algorithms over time!
- ▶ **Multi-Gigabit Transceiver Links 16 to 28 Gb/s**
- ▶ **Advanced Telecommunications Architecture (ATCA) Form Factor**
 - ▶ Better Form Factor for board routing
- ▶ **IPMI and Embedded Linux Solutions**



Algorithms + Implementation using High Level Synthesis



High Level Synthesis for Algorithm Development



- **HLS is an automated design process that interprets algorithm specification at a high abstraction level and creates digital hardware/RTL code that implements that behavior**
- **HLS significantly accelerates design time** while keeping full control over the choice of optimal architecture exploration, proper level of parallelism and implementation constraints
- Reduces overall verification effort
- **New Model for Phase 2 Trigger:** Core firmware for I/O, clock, ancillary functions **written by firmware engineers, trigger algorithms** written by **physicists**
- **Several HLS options in use: product / vendor:**
 - [Catapult-C](#) / [Calypto Design Systems](#)
 - [BlueSpec](#) / [BlueSpec Inc.](#)
 - [Symphony C](#) / [Synopsys](#)
 - [MaxCompiler](#) / [Maxeler](#)
 - [Cynthesizer](#) / [Cadence](#)
 - [HDL Coder](#) / [MathWorks \(Matlab\)](#)
 - [OpenCL](#) (Intel/Altera)
 - [Vivado HLS](#) / [Xilinx](#)

Becoming a Standard Tool at CMS!



HLS Usage: Kalman Filter Tracking

A **Kalman Filter Muon Track-Finder** has been written in **HLS firmware** for the barrel region **already for Run II**

Algorithm does **track propagation** and **parameter updating**

A large amount of matrix math

Solution: use DSP cores to reduce

FPGA resource utilization

- Programmable using HLS

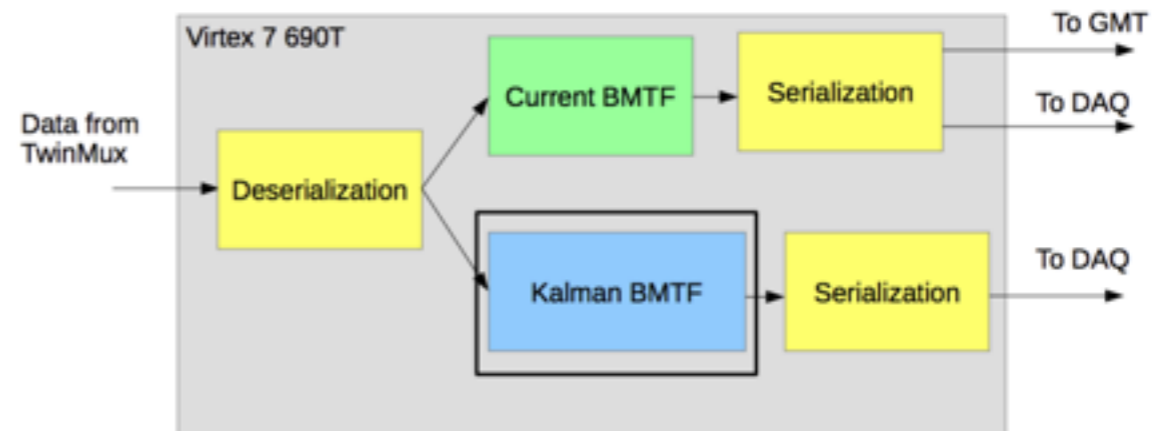
Latency ~200 ns

Data and emulator agreement is 99.7%

Parallel implementation in current

Phase-1 BMTF firmware

$$\begin{aligned}
 x_n = \begin{pmatrix} k \\ \phi \\ \phi_b \end{pmatrix}_n &= \begin{pmatrix} 1 & 0 & 0 \\ a & 1 & b \\ c & 0 & d \end{pmatrix} \begin{pmatrix} k \\ \phi \\ \phi_b \end{pmatrix}_{n-1} \\
 P_{n+1} &= F P_n F^T + Q \\
 z_k = \begin{pmatrix} \phi_s \\ \phi_{bs} \end{pmatrix} &= \begin{pmatrix} 0 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} k \\ \phi \\ \phi_b \end{pmatrix}
 \end{aligned}
 \left. \begin{array}{l} \\ \\ \\ \end{array} \right\} \begin{array}{l} y_n = z - H x_n \\ S = H P H^T + R \\ K = P H^T S^{-1} \\ x = x_n + K y_n \end{array}$$



HLS Usage: NN for Muon P_T Assignment

HLS4ML tool kit

Implementation of fast neural network inferences into FPGAs:

arXiv:[1804.06913v2](https://arxiv.org/abs/1804.06913v2)

Converts results of a trained NN into Vivado HLS firmware for modern FPGAs

Optimize use of DSPs for NN calculation

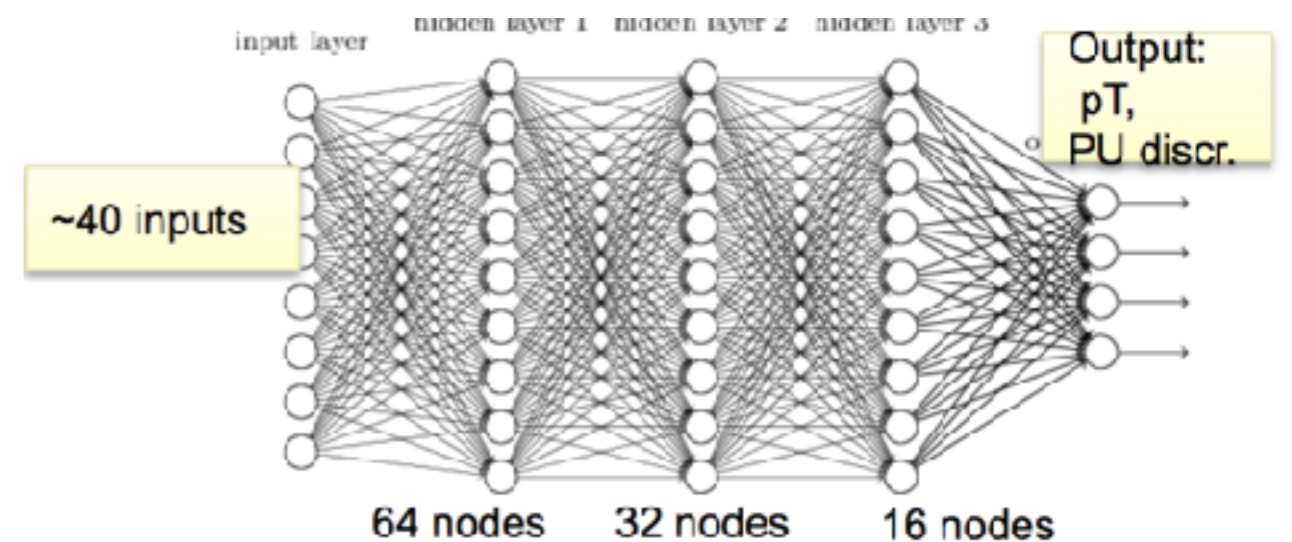
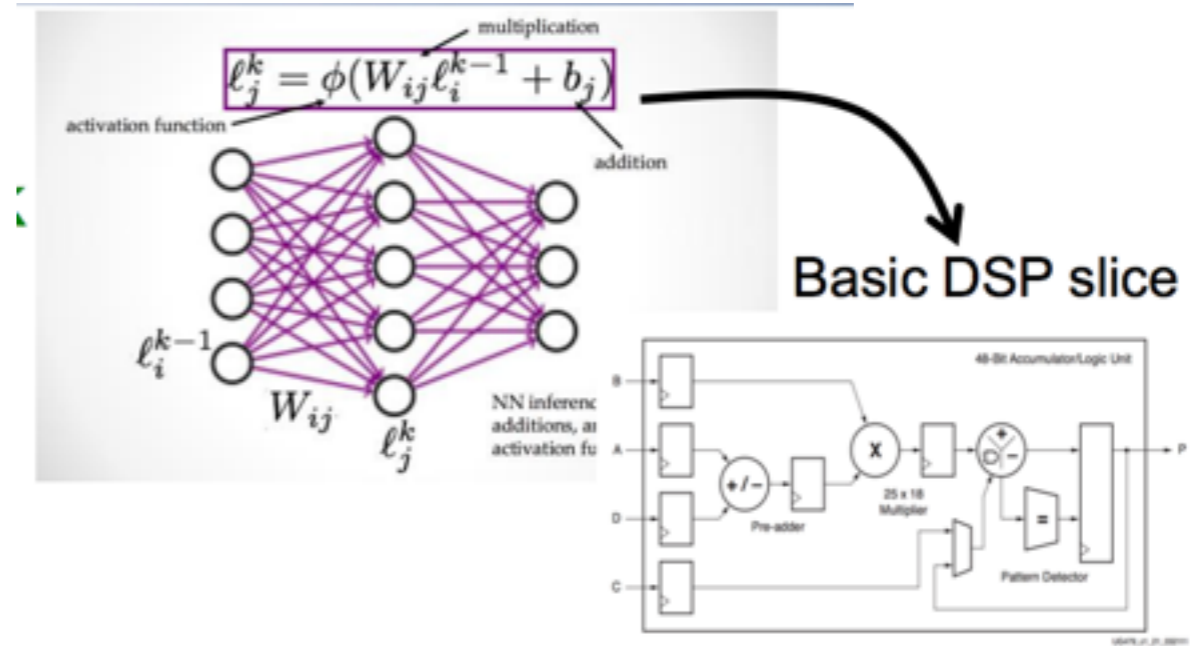
P_T regression for muon trigger

NN alternative to BDT LUT

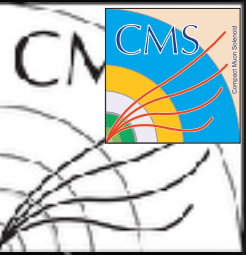
No loss of input variable precision

Development and testing ongoing for

Run-3 and Phase-2



Conclusion



Level 1 Trigger (Run-1, Run-2 and Run-3)

Select 100 kHz interactions from 1 GHz

Processing is synchronous & pipelined

Decision latency is 3 μ s

Algorithms run on local, coarse data (Calo + Muon)

Hardware is modular and “generic” possibility to modify algorithms

Higher Level Triggers

Depending on experiment, done in one or two steps

If two steps, first is hardware region of interest

Then run software/algorithms as close to offline as possible on dedicated farm of PCs

Phase-2 Level 1 Trigger

Bring tracking to L1T (new triggerable tracker is the key)

Migrate algorithms (not constraints) from HLT L1

Keep the processing parallel

Keep the pipeline, increased latency for track building



Any Questions?

Vivado HLS C/C++ libraries **contain functions and constructs** that are **optimized for implementation in an FPGA.**

Using these libraries helps to ensure high Quality of Results (QoR)

final output is a high-performance design that makes optimal use of the FPGA resources.

Vivado HLS also provides **additional libraries to extend the standard C/C++ languages:**

- Arbitrary precision data type (e.g. 5-bit unsigned integer: `ap_uint<5>`)
- Fixed-point data type (e.g 18-bit integer with 6 bits above binary point: `ap_fixed<18,6,AP_RND >`)
- Half-precision (16-bit) floating-point data types
- Math and video operations, Xilinx IP functions (FFT, FIR)

Radar Design (1024x64 floating-point QRD)	RTL Approach (VHDL)	Vivado Hls
Design Time (weeks)	12	1
Latency (ms)	37	21
Resources:		1
• BRAMS	273	38
• FFs	29,686	14,263
• LUTs	28,512	24,257

HLS QoR (* from Xilinx brochure)

HLS does require learning a new skill
it implies **change in the methodologies,**
in the design processes, and to some
extent, in the skills required.

Example Algorithm with HLS



Example: HLS algorithm to compute “Pile Up” Level as part of CMS Trigger Calorimeter Logic

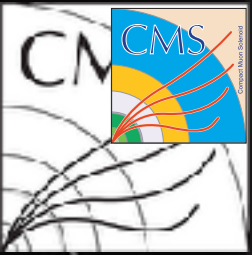
```
1 #include <stdio.h>
2 #include "ap_int.h"
3
4 #define NR_CALO_REG ( (6 + 7) * 2 * 18) // 468
5 #define PUM_LEVEL_BITSIZE (9)
6
7 // helper function to count number of bits set in "bitString"
8 ap_uint<PUM_LEVEL_BITSIZE> popcount(ap_uint<NR_CALO_REG> bitString)
9 {
10     ap_uint<PUM_LEVEL_BITSIZE> popcnt = 0;
11     loop_popcnt: for (int b = 0; b < NR_CALO_REG; b++)
12     {
13 #pragma HLS unroll
14         popcnt += ((bitString >> b) & 1);
15     }
16     return popcnt;
17 }
18
19 ap_uint<PUM_LEVEL_BITSIZE> UCT_pum_level_impl3(
20     ap_uint<10> region_et[NR_CALO_REG],
21     ap_uint<10> pum_thr)
22 {
23 #pragma HLS PIPELINE II=6 // target clk freq: 250 MHz (~6 clks/BX)
24 #pragma HLS ARRAY_RESHAPE variable=region_et complete dim=1
25
26     ap_uint<NR_CALO_REG> tmp = 0; // important: do var init
27
28     loop_pum: for (int idx = 0; idx < NR_CALO_REG; idx++)
29     {
30 #pragma HLS UNROLL // fully unroll the loop
31         if (region_et[idx] > pum_thr)
32             tmp.set_bit(idx, true);
33         else
34             tmp.set_bit(idx, false); // !! The only difference with impl2 !!
35     }
36
37     return popcount(tmp);
38 }
```

- Fully ANSI compliant C impl.
- Vivado HLS compiler guided by the user with **#pragma** directives
- HLS impl. is significantly easier to validate compared to traditional HDL approach. It also produces better results compared to HDL in several studied cases.

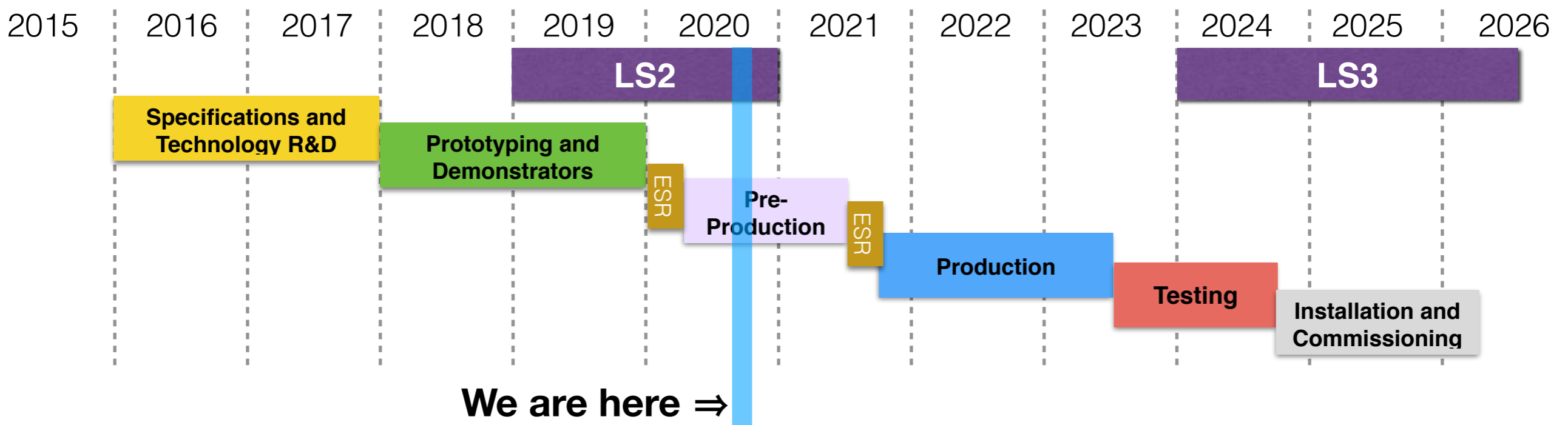
FPGA LUT count	2996
V7690T LUT [%]	~ 0.6
Latency in clk cycles @ 250 MHz	3



Trigger: On the road to Run-3 and the HL-LHC



- ▶ **Pre-TDR:** establish baseline and change control for interfaces and TPGs
- ▶ **Pre-ESR (2021Q3):** finalize interfaces. Slice tests of all for final design.
- ▶ **Full production batches delivered to CERN 2023Q3**
- ▶ 2.75 years available for testing and commissioning as interfacing electronics are installed (currently reserving ~6 months float)
- ▶ **Pre-beam commissioning:**
 - ▶ Internal relative timing/TMUXing of L1 (with ECAL pulses, e.g.) and available interfaces
 - ▶ Muon cosmics in LS3, run 3 muon data possible for some ingredients (GEM)
 - ▶ With Tracker inserted starting 2026



Common Hardware Platforms: **Advanced Processor Development Board**



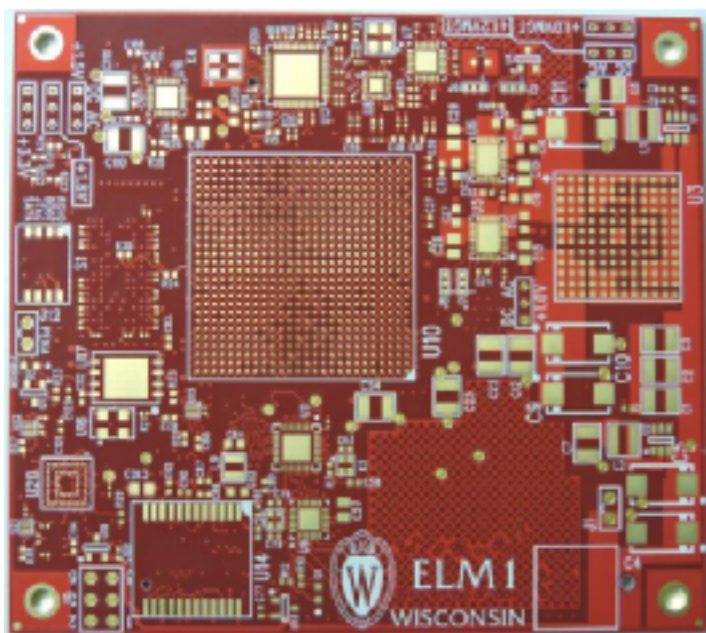
Mezzanines

DDR RAM

- ▶ Very large & fast LUT for tracking pT assignment
- ▶ Flexible – any algo. can be used, now or in future, no matter how complicated, and it will have low latency
- ▶ e.g. BDT algorithm used in Phase-1 EMTF
- ▶ Target DDR4 128 GB memory (from 1 GB for Phase-1)

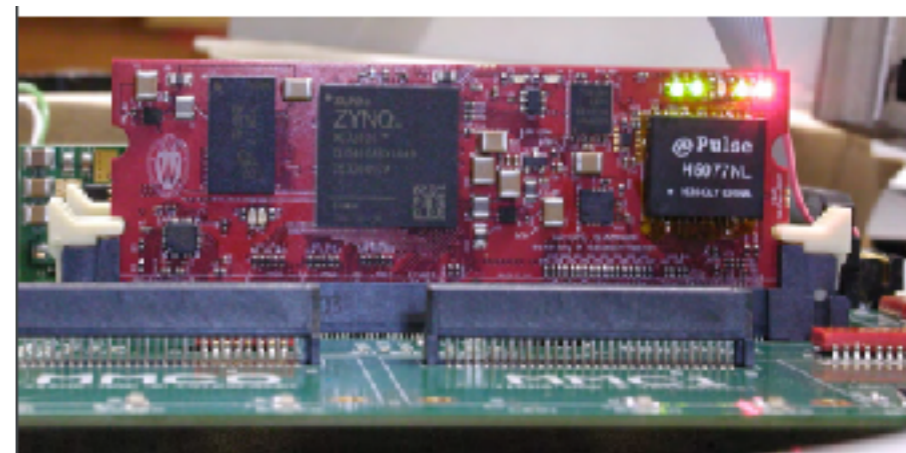


Embedded Linux Mezzanine



- ▶ **Embedded Linux** endpoint
 - ▶ both based on the Xilinx ZYNQ platform
 - ▶ used for control functions

- ▶ **IPMC**: IPMI controller for ATCA blades
- ▶ **ZYNQ 7020**, RTOS-based application

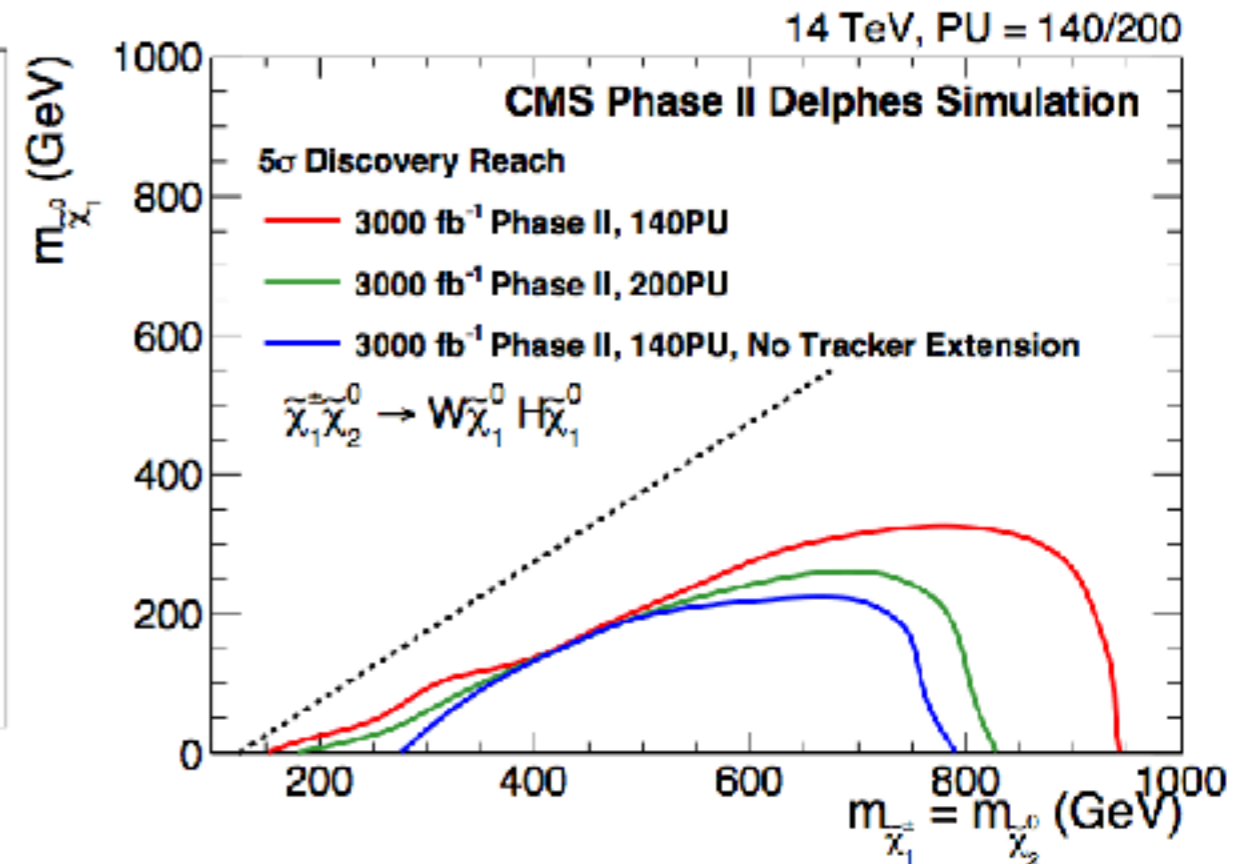
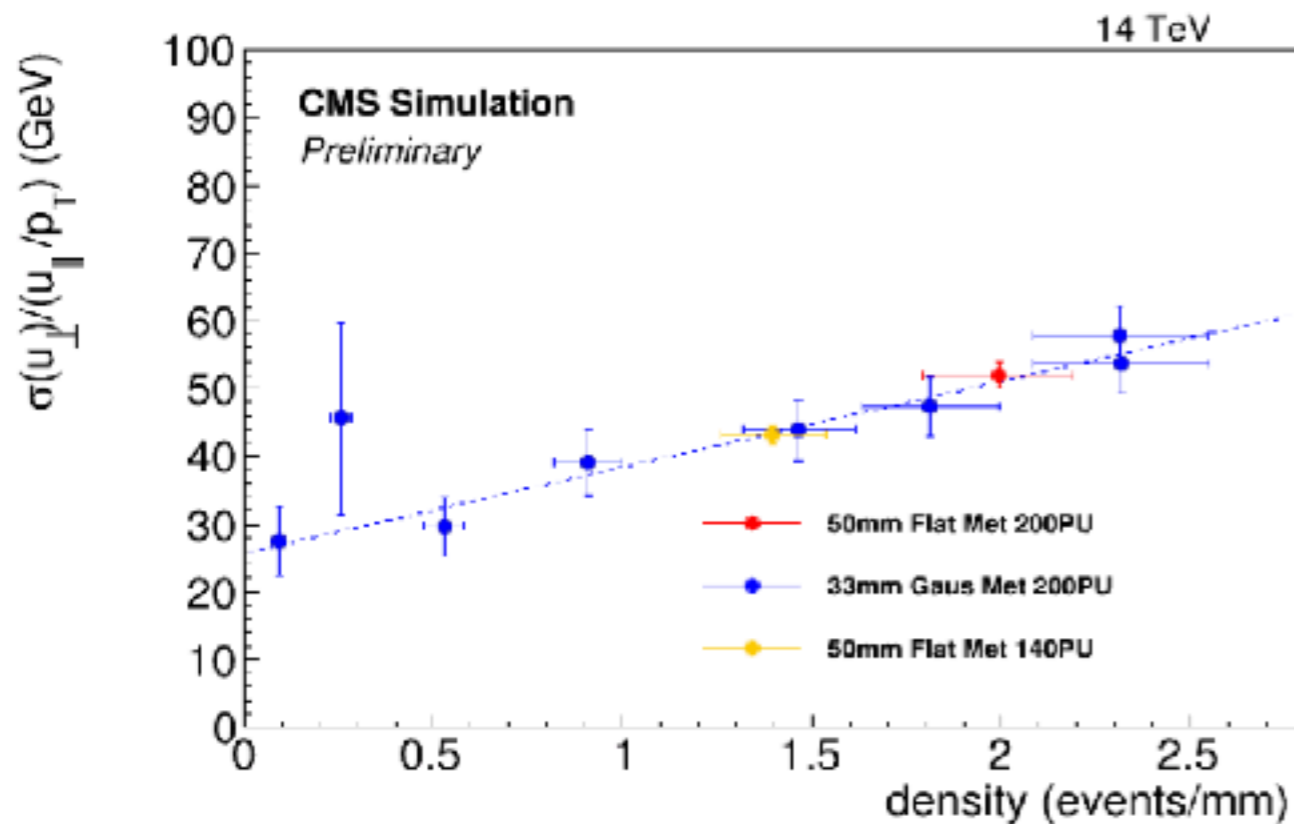


The Effects of High Pileup in Reconstruction

► Clearly visible in current upgrade studies

- $W^\pm H + E_T^{\text{miss}}$ Search sensitivity at high mass decreases when going from 140 to 200 PU

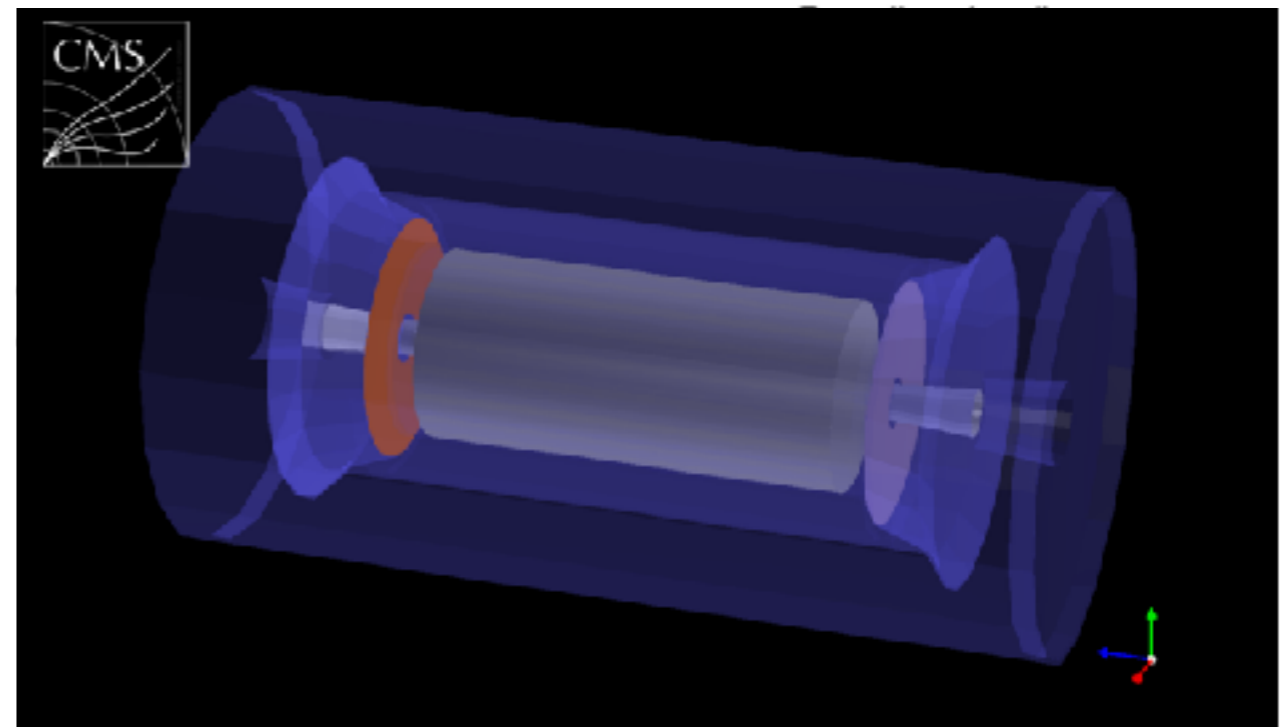
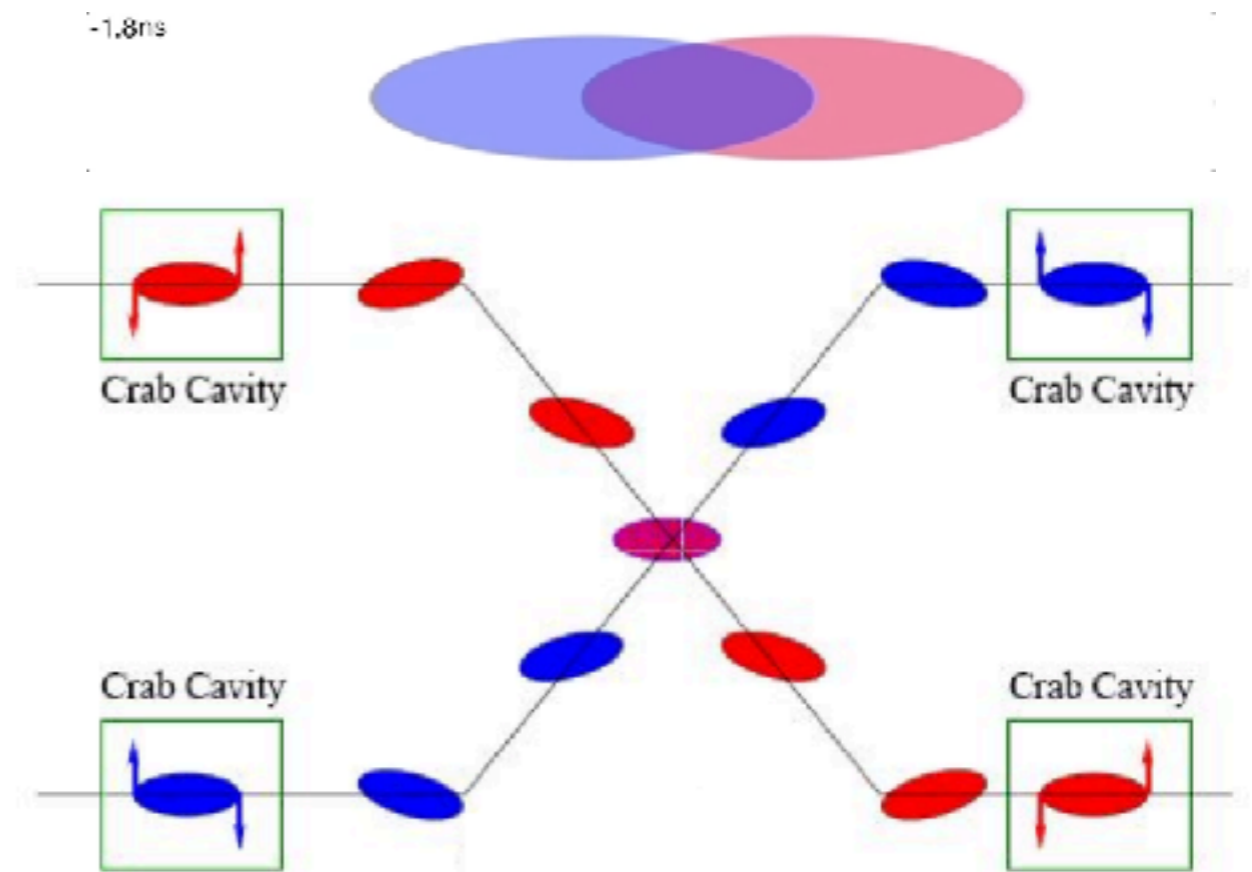
► From [CERN-LHCC-2015-19, LHCC-G-165] many analyses using Taus, Jets and E_T^{miss} are degraded as Pile Up increases, even with other detector upgrades



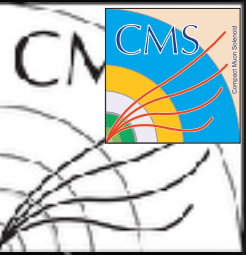
MIP Timing Detector

Proton Bunch Interactions are Spread in Time

- ▶ During collisions, **bunch crossing operates over a discrete time interval**
- ▶ **Currently CMS sees only the integral of this process over time**
- ▶ Need to discriminate between vertices over an RMS of ~ 180 ps
- ▶ Additional **thin MIP Timing Detector** between tracker outer layer and ECAL Front End cooling plates



HLS caveats, traps and pit-falls



It's a disruptive technology

it implies **change in the methodologies**, in the design processes, and to some extent, in the skills required.

Not all C/C++ coding styles are equal in terms of QoR, and there is **still the potential for ending up with poor quality RTL when the C++ code is not suited for HLS**

Required resource estimates provided by HLS tools might not be always reliable and need careful checking

Good style not only requires an understanding of the underlying hardware architecture of an algorithm, so that it is reflected in the C++ design, but also an understanding of how HLS works.



HLS Usage: Menu Development

80% of Trigger Menu already has basic firmware implementation

Trigger algorithm	L1 trigger with L1 tracks		Offline threshold(s) [GeV]
	Rate [kHz]		
$\langle PU \rangle$	140	200	
Single Mu (tk)	14	27	18
Double Mu (tk)	1.1	1.2	14 10
Ele* (iso tk) + Mu (tk)	0.7	0.2	19 10.5
Single Ele* (tk)	16	38	31
Single iso Ele* (tk)	13	27	27
Single γ^* (tk-iso)	31	19	31
Ele* (iso tk) + e/ γ^*	11	7.3	22 16
Double γ^* (tk-iso)	17	5	22 16
Single Tau (tk)	13	38	88
Tau (tk) + Tau	32	55	56 56
Ele* (iso tk) + Tau	7.4	23	19 50
Tau (tk) + Mu (tk)	5.4	6	45 14
Single Jet	42	69	173
Double Jet (tk)	26	43	2@136
Quad Jet (tk)	12	45	4@72
Single ele* (tk) + Jet	15	15	23 66
Single Mu (tk) + Jet	8.8	12	16 66
Single ele* (tk) + H_T^{miss} (tk)	10	45	23 95
Single Mu (tk) + H_T^{miss} (tk)	2.7	8	16 95
H_T (tk)	13	24	350
Rate for above triggers*	180	305	
Est. rate (full EG eta range)		390	
Est. total L1 menu rate ($\times 1.3$)	260	500	

Thresholds of Phase1 L1 @1.1E34

18
14 10
19 10
45
27
NA
22 16
NA
71
60 56
21 57
45 14
170
2@125
4@51
23 66
16 55
23 100
16 95
350

Menu for Interim Document - Already updated!



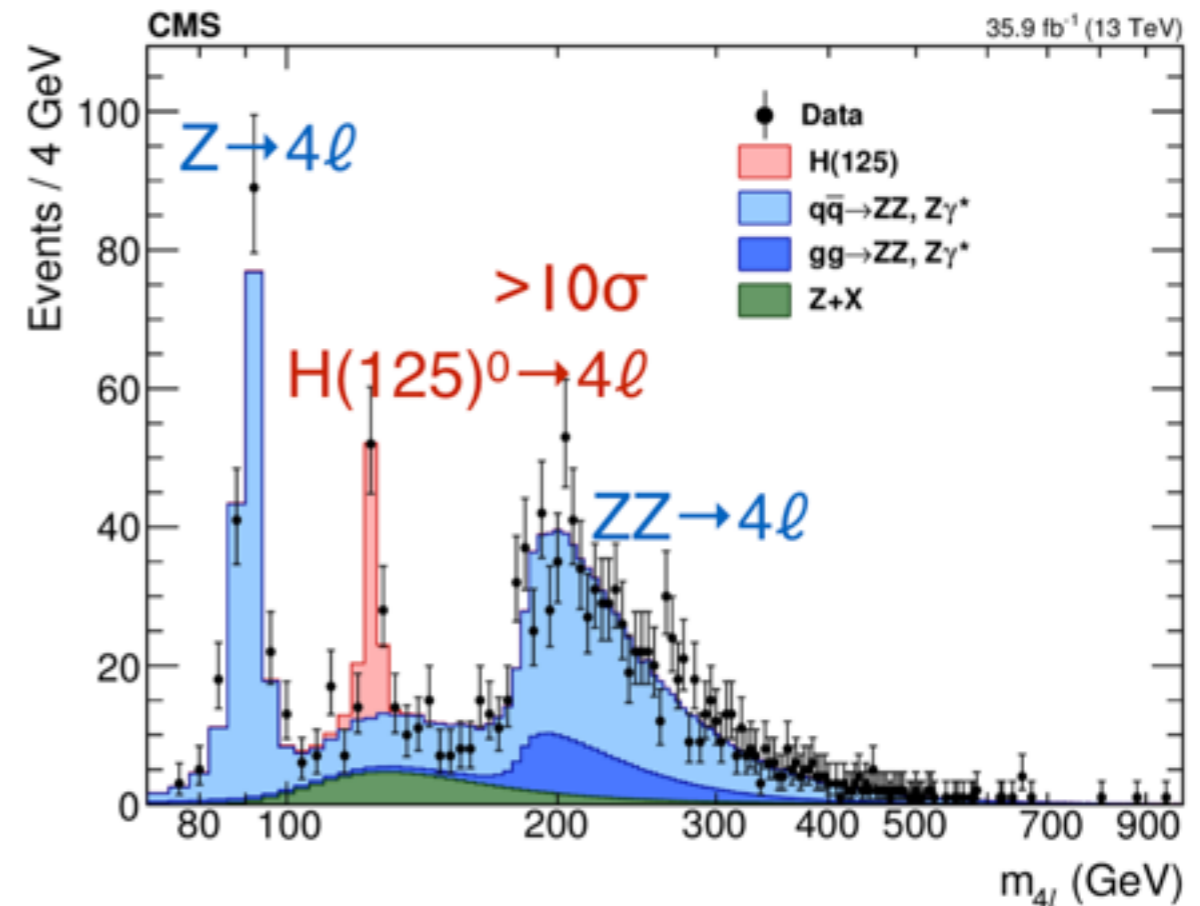
Current State of the Universe (to a Particle Physicist)



LHC Experiments have confirmed that the Standard Model is Robust!

However, there are still **many open questions** and it **is not an ultimate theory** for everything

- ▶ Why is the **Higgs Boson so light**?
- ▶ What is the nature of **Dark Matter/Dark Energy** (96% of the universe!!)
- ▶ Why is there **more matter** than **anti-matter**?
- ▶ Why are the scales of the weak force and the gravitational force so different?



With the HL-LHC we may be able to answer these questions!

Either Indirectly: Precision measurements of SM processes

or Directly: SUSY, Long Lived Particles, New Heavy Resonances, Dark Matter





Fundamental New Discovery

→ Represents a Window to the Unknown

Using Run I + Run II Data we have measured well the Higgs properties using $H \rightarrow ZZ$ and $H \rightarrow \gamma\gamma$

Discovered $H \rightarrow bb$

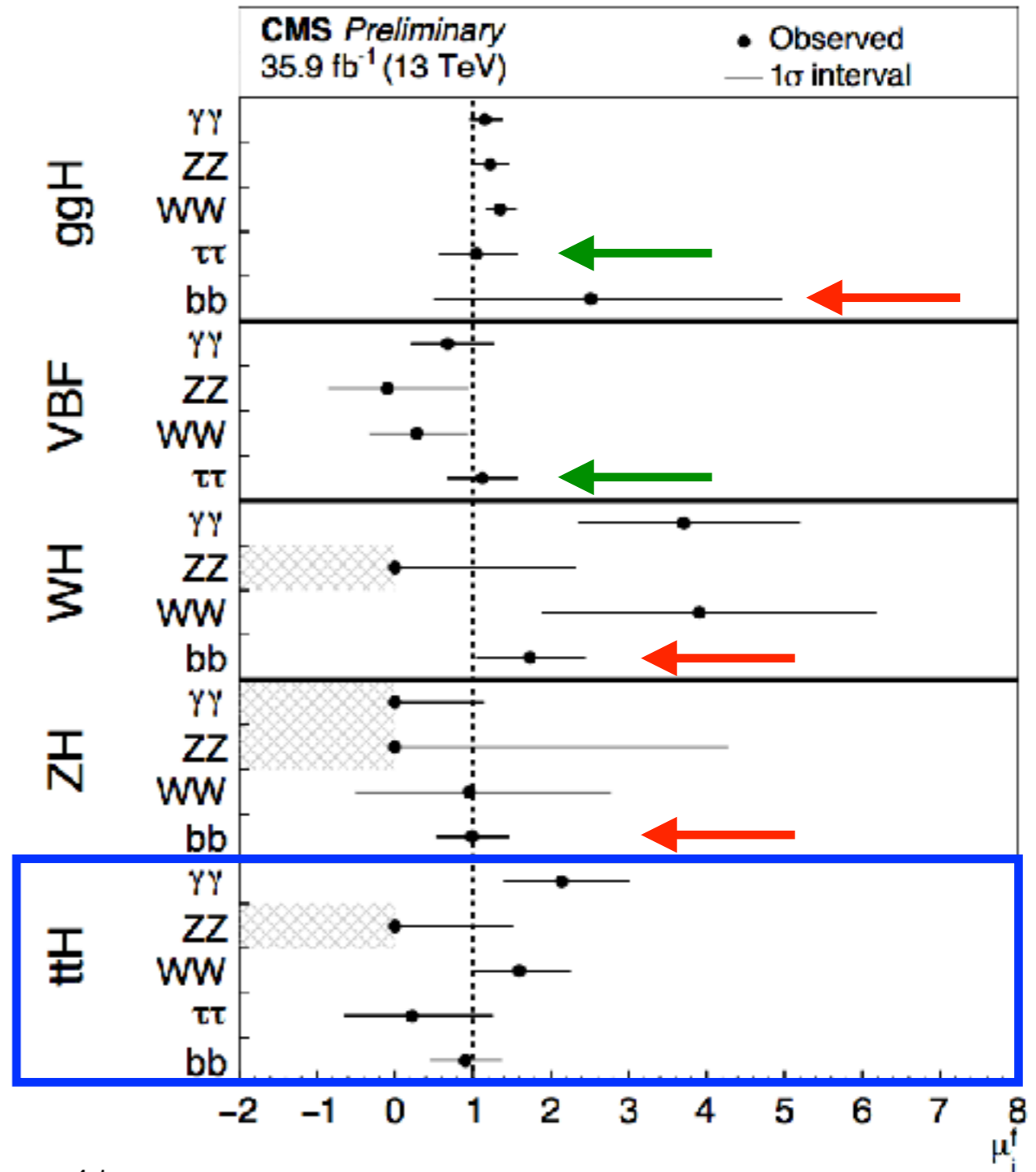
Discovered $t\bar{t}H$ production

Discovered $H \rightarrow \tau\tau$

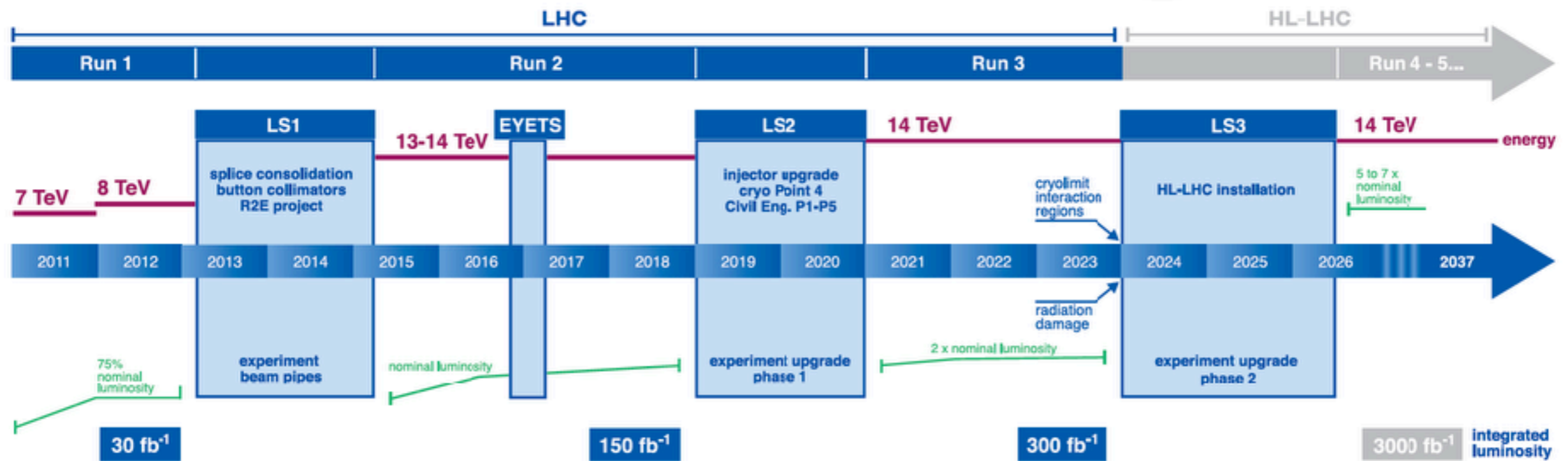
Remains important to study carefully this particle

But Also, Measure/Search for more Couplings (Production and Decay), Self Coupling, Rare Decays, Exotic Decays

Performance studies are used to motivate upgrade efforts!!

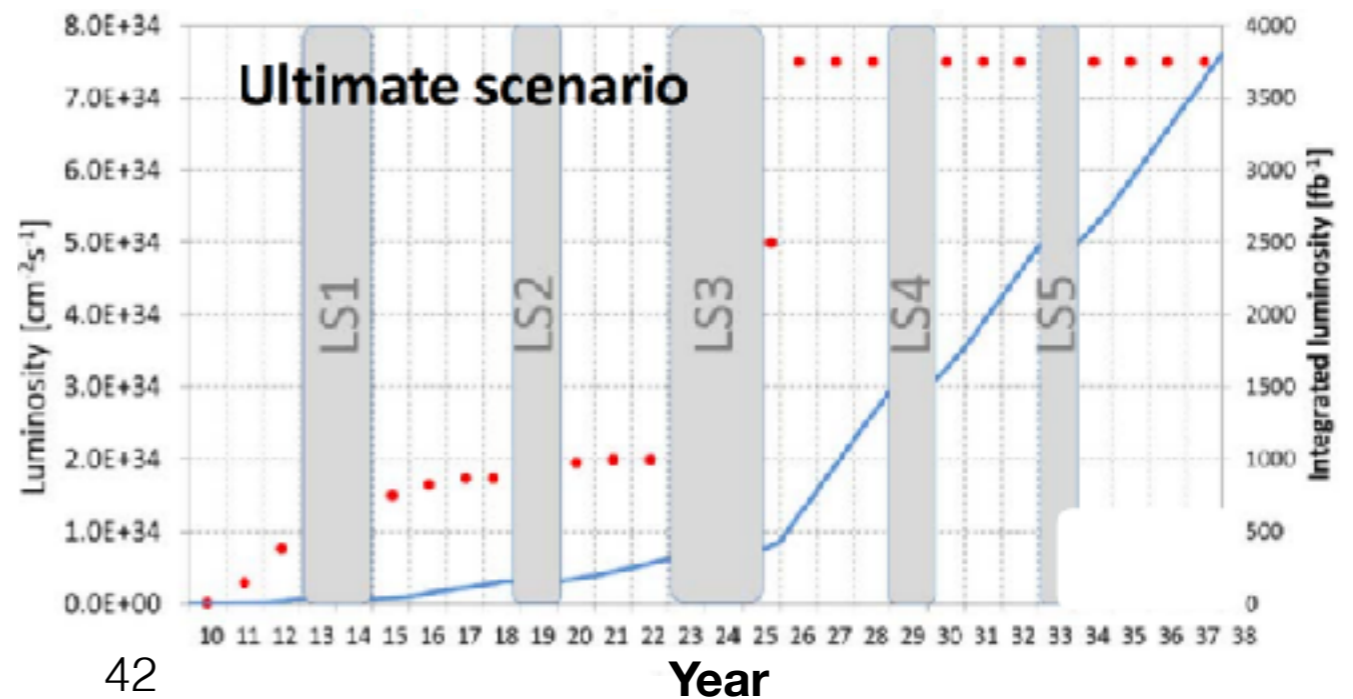


HL-LHC schedule



Nominal Scenario: $L = 5.0 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ up to 3000 fb^{-1} (140 PU)

Ultimate Scenario: $L = 7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ up to 4000 fb^{-1} (200 PU)

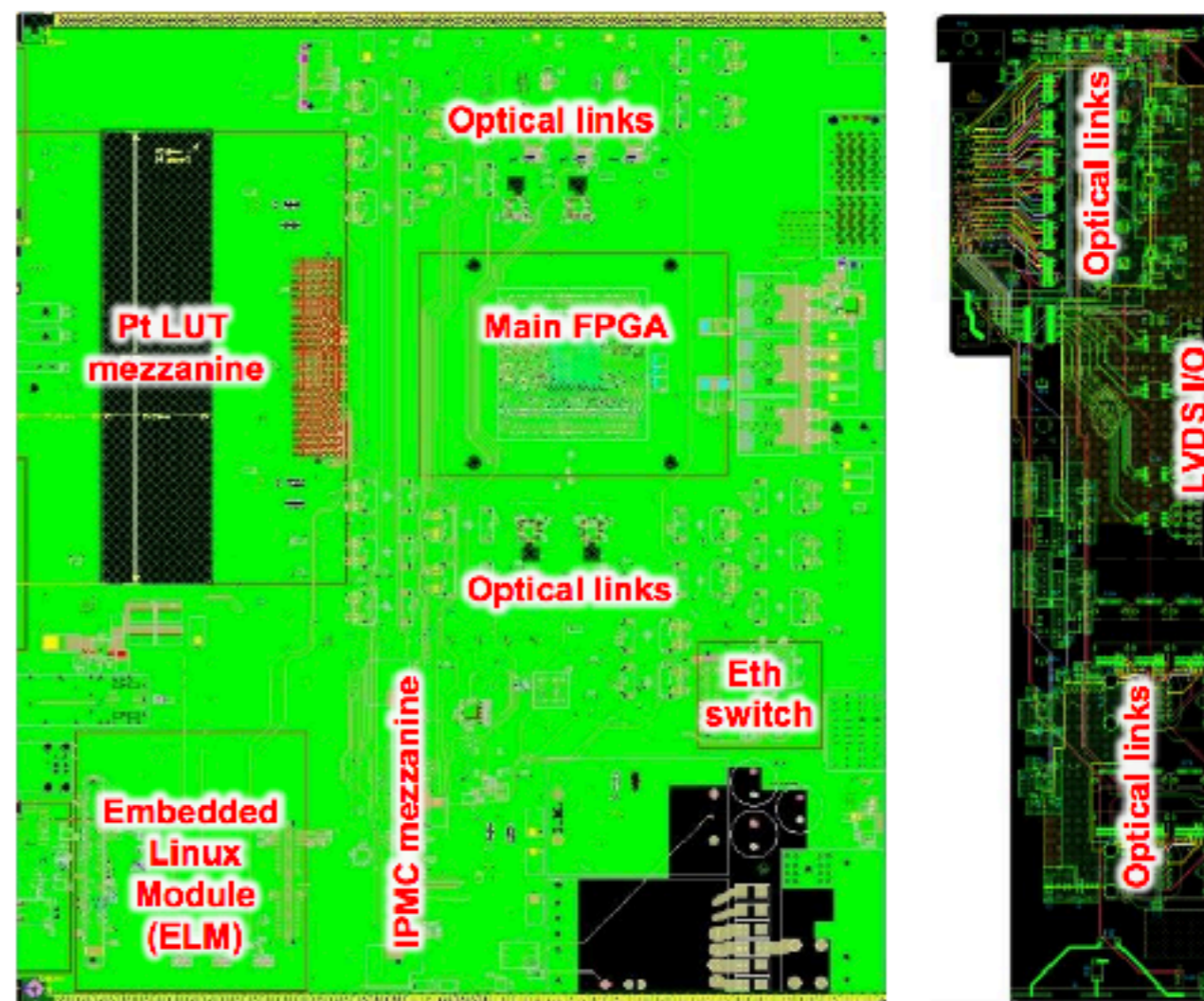


Targets one or more high-end Xilinx FPGA (C2104 package)

- ▶ Allows up to **96 optical link pairs**
- ▶ Supports speeds up to **28 Gb/s** using Samtec Firefly Modules

Mezzanines for adaptability/parallel development

- ▶ **Embedded Linux mezzanine** for control functions (**Xilinx Zynq**)
- ▶ **IPMC mezzanine** (another Zynq+Linux)
- ▶ **Gigabit Ethernet as main control interface**
 - ▶ Option for 10G Ethernet



Main board screenshot from T. Gorski

- ▶ Modular design philosophy, emphasis on platform solutions with flexibility and expandability

Common Hardware Platforms: Serenity

ATCA Development Platform

Main Board

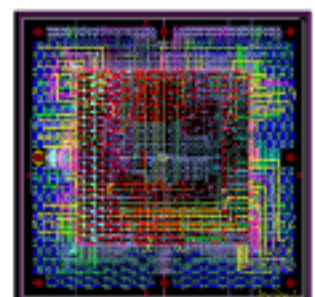
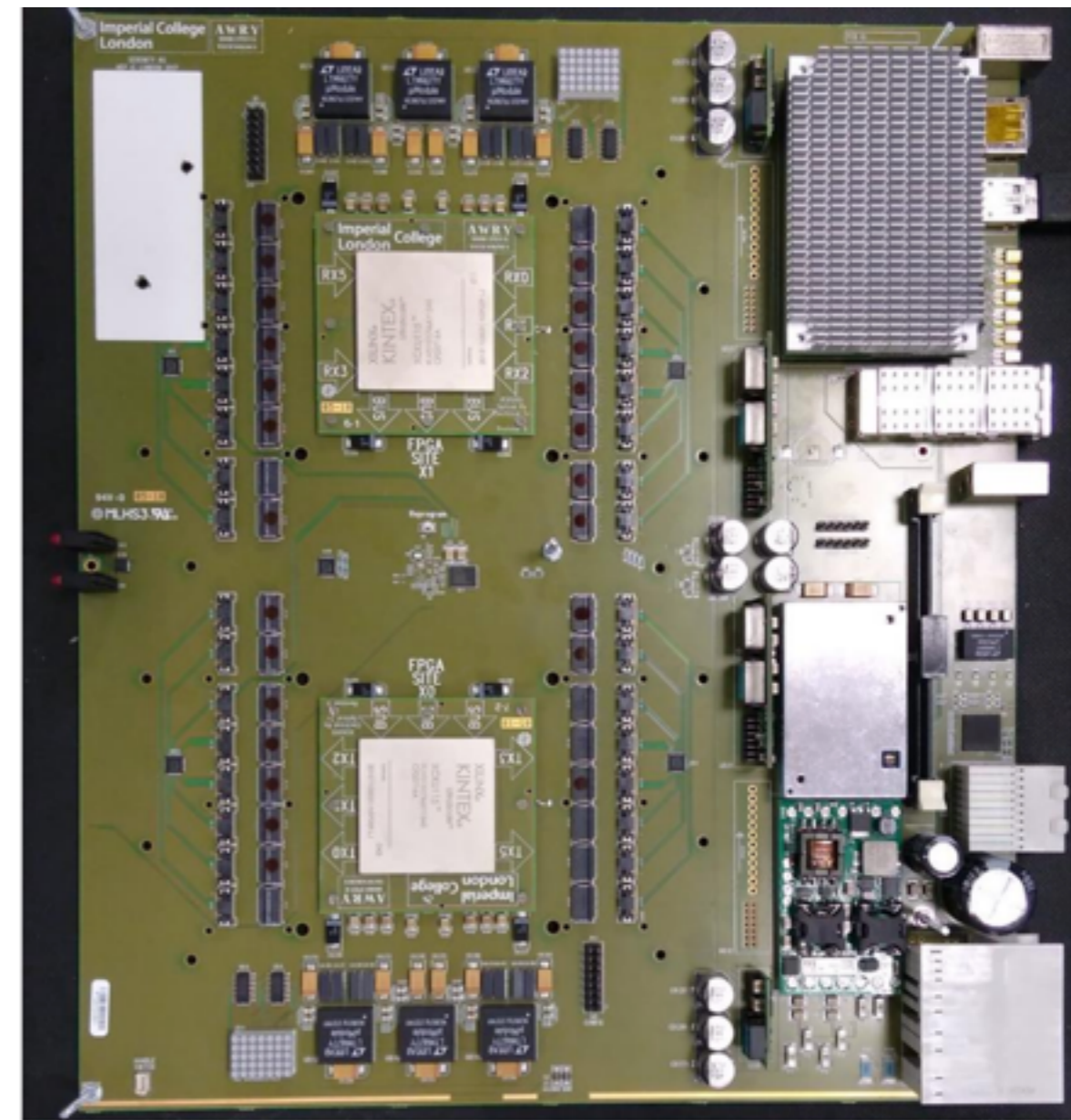
Services - Power, Clocks, Optics, Interconnects, IPMC & CPU

Daughter Cards

Data Processing FPGAs

- Showing 2 Xilinx Kintex KU115
- “Customer” able to choose preferred package/family/generation

Different groups developing daughter cards: Xilinx KU115, Xilinx KU15P, Xilinx VU9P



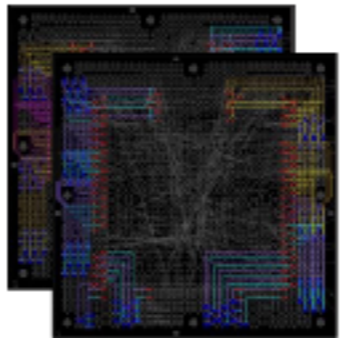
All optical KU115, Imperial



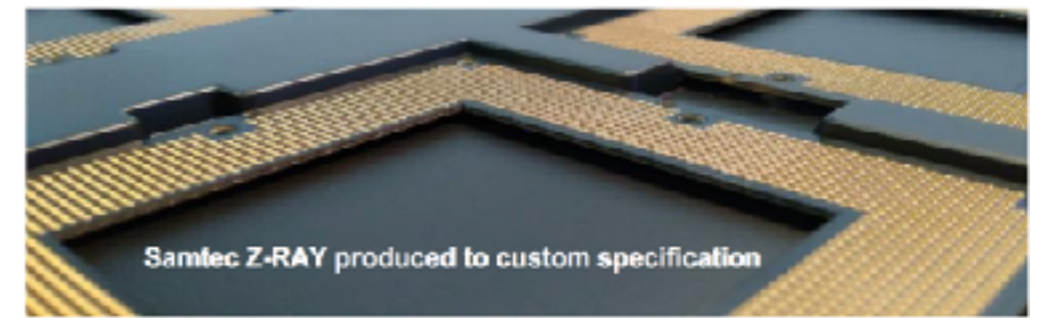
Mixed optical/electrical KU15P, KIT



Clock-performance analyzer GEA Saclay



In progress, All optical VU9P, TIF

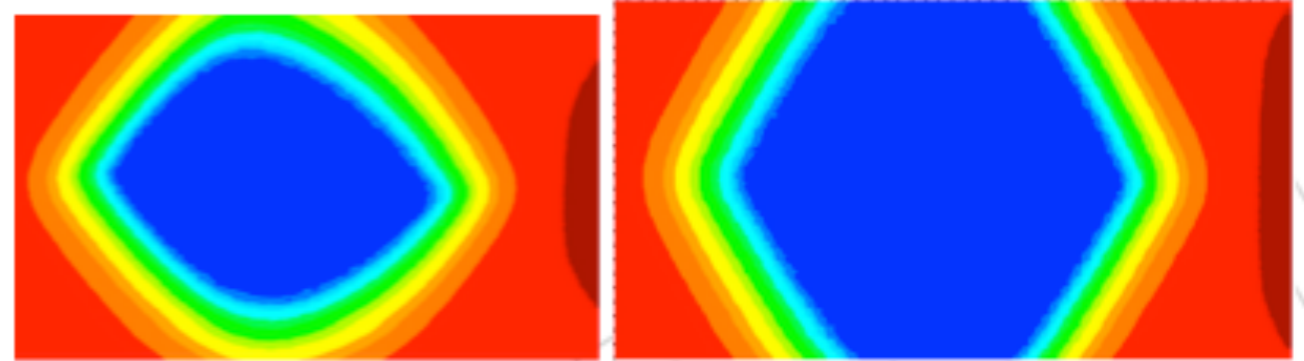


Samtec Z-RAY produced to custom specification



Key technologies/challenges :

- ▶ FireFly Modules, Multi-Gbit transceivers/optics
- ▶ ATCA form factor
- ▶ Embedded Linux
- ▶ Large RAM
- ▶ Power delivery and thermal management
- ▶ System level integration & maintenance



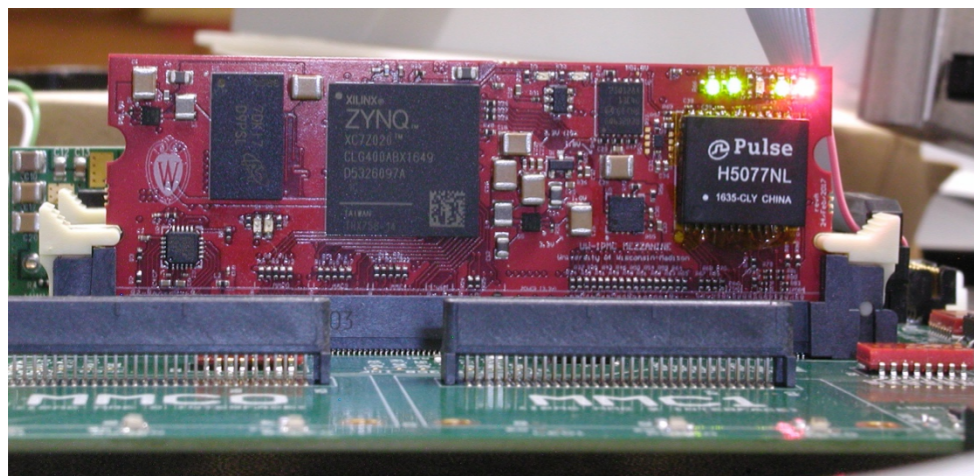
Eye diagrams for 26Gb/s transceivers



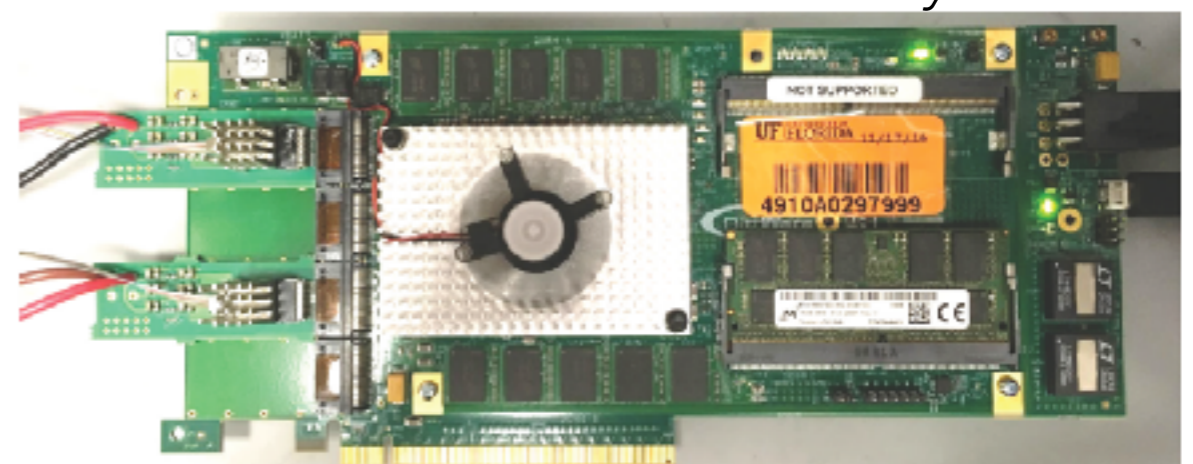
Hardware demonstrators



DDR Memory R&D



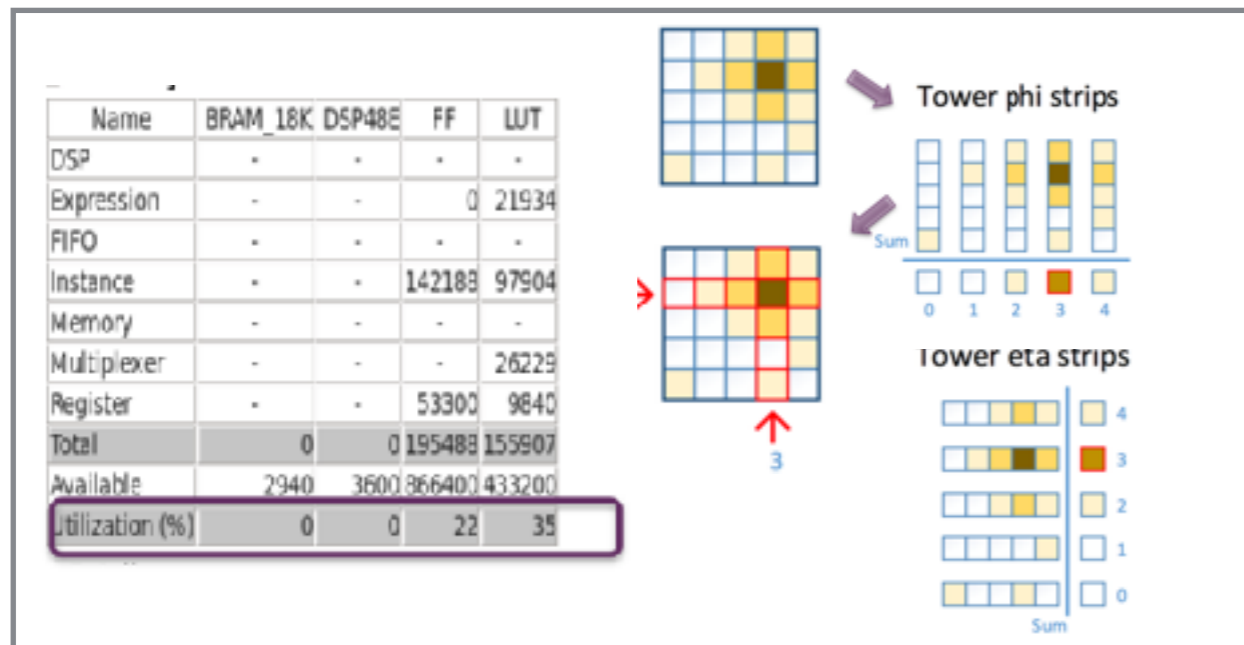
IPMS - IPMI for ATCA



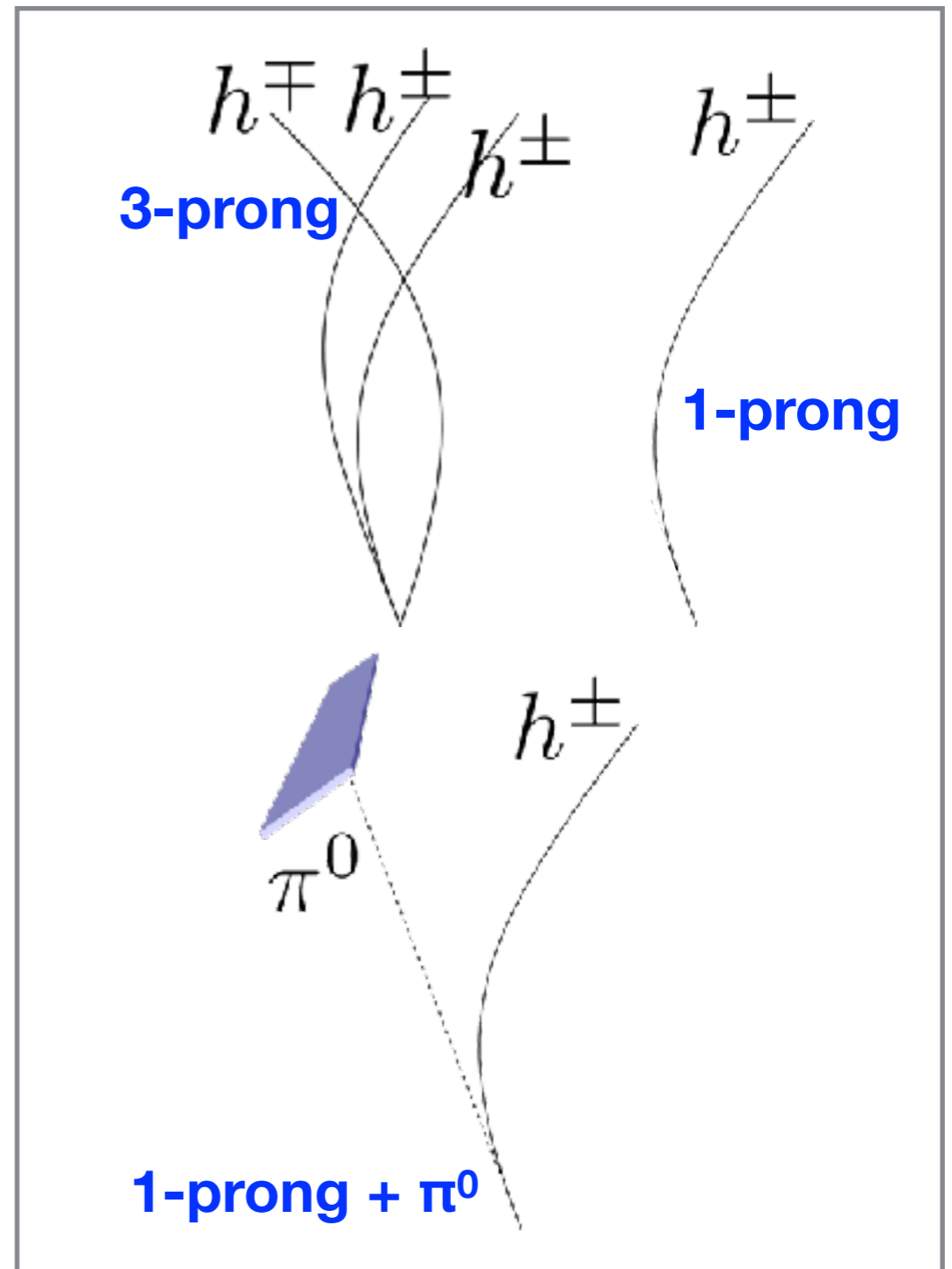
Moving Forward: HLS Development

A number of algorithms are being implemented in Vivado HLS

Cluster Producer



Tau Finding HPS@L1



Kalman Filter Muon Reconstruction

