Mu2ell calorimeter readout: sparse ideas

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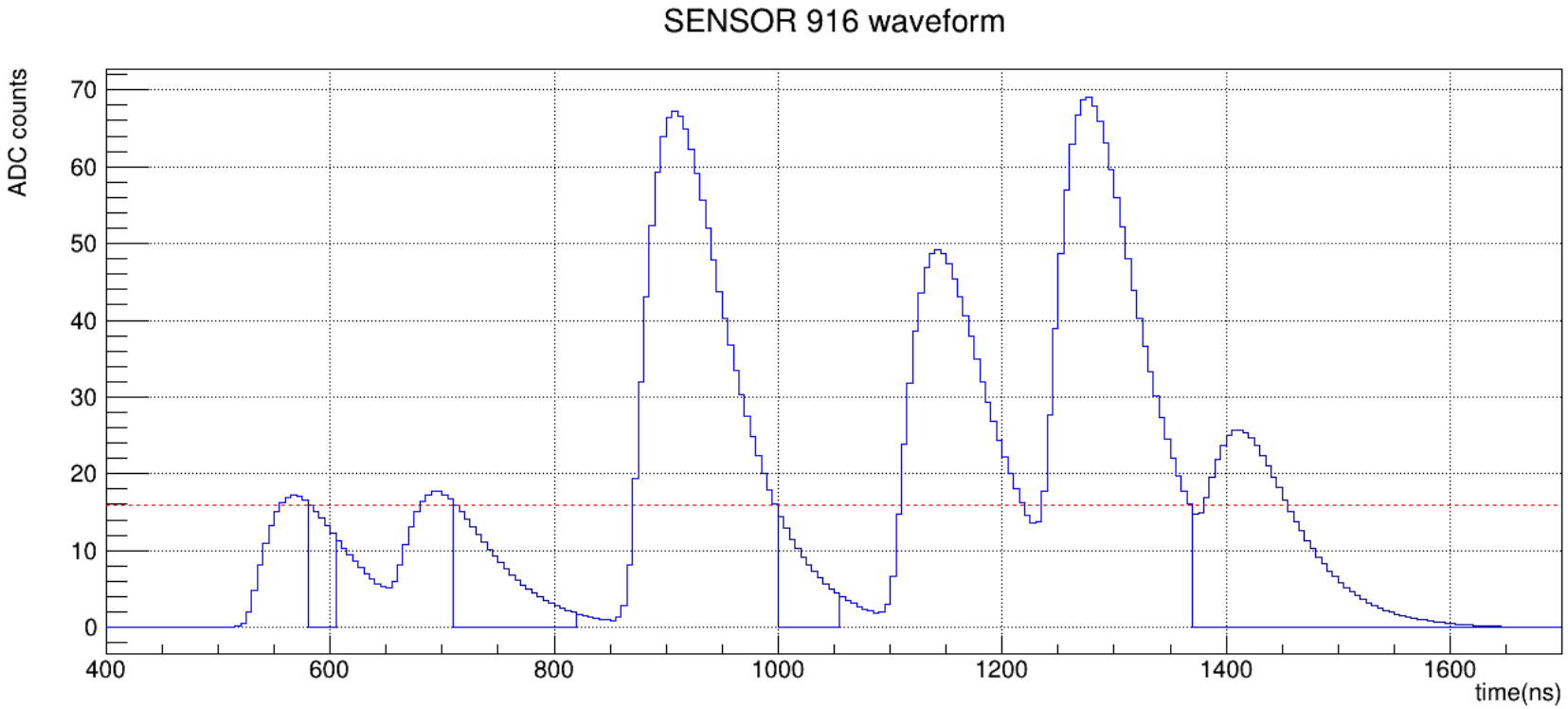
Mu2e event

- Current Mu2e ecal event (simulation, 1 channel, inner ring, crowded ...)



- One hit 100- 200 nsec

Mu2e

- Mu2eII beam luminosity is 3x -> we will have 3 times more hits ...
  - We have to change detector strategy ... (pile-up explosion ...)
- Lets' assume the same architecture: crystal + photodetector, and almost the same specs: timing resolution o(200 ps), energy resolution o(10 %)
  - We need faster crystal (BaF2, ...) and faster analog electronics (shaping amplifier)
- We might expect a signal length o(30 nsec) with a rise time o(5 nsec)

- Mu2e readout is based on 200 MHz 12 bits ADCs, shaper is tuned for rise time o(25 – 30 nsec) so we can fit 5-6 samples to calculate T0.
- We need a different readout scheme to reach the same requested o(200 ps) timing resolution

Readout techniques

- Ultra Fast ADC (1 GHz ...)
- TDC
- TDC + ADC

- Radiation o(1 Mrad) -> Radiation hardness is challenging ...

FAST ADC (> 1 GHz) 1/5

- Still quite costly (at least in 2020 ...)

AD9690-1000	1	14	1G	67.2	2.5	1.7	JESD204B	2	$292.19 (AD9690BCPZ-1000)
AD9234-1000	2	12	1G	64.2	35	1.34	JESD204B	3	$389.90 (AD9234BCPZ-1000)
AD9680-1000	2	14	1G	67.2	2.5	1.7	JESD204B	3.3	$584.38 (AD9680BCPZ-1000)

- Power hungry (3W vs 0.5 W Mu2e)
- Each needs 4 JESD 204 FPGA serializers ...
    - A mu2eII DIRAC eq. board would need 40 multi Gbit serializers ...
        - 2 – 3 FPGA high end (at 2020)
- A 20 channel board would be very expensive and power hungry (60 – 100 W /board)
- Not keeping in account radiation tolerance (faster signals requires shorter cables ...)

FAST ADC (> 1 GHz) 2/5

- Fast ADC solves pile-up problem
- Bandwidth needs to be carefully simulated:
  - 5 x sampling frequency
  - more hits but shorter.
- Probably each board would require a faster link (10 gbit ?)

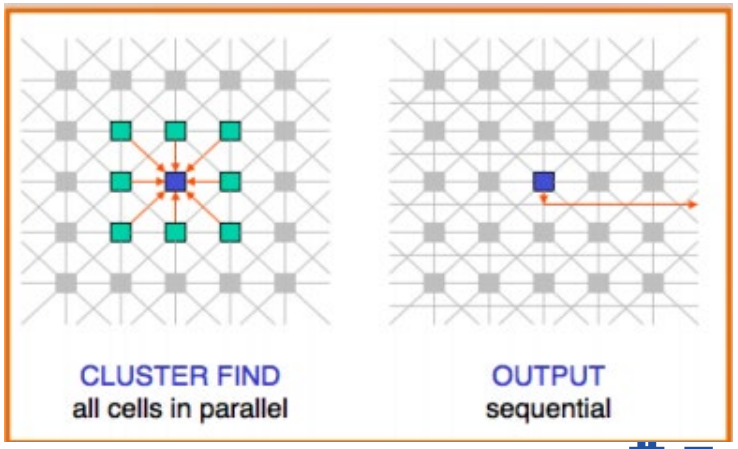
FAST ADC (> 1 GHz) 3/5

- Solution to limit the bandwidth and stored data:
  - analyze raw ADC data on the flight and send back only hits physics parameters at the offline level. (T0, E, pile-up, shape ...)
- Something in the middle ?
  - Calculate in real time some parameters with intermediate resolution and send them as trigger primitives to a L0 trigger system
  - Store raw data in a big buffer
  - Send raw data only after receiving a L0 accept

- Requires a trigger system for mu2e II ...

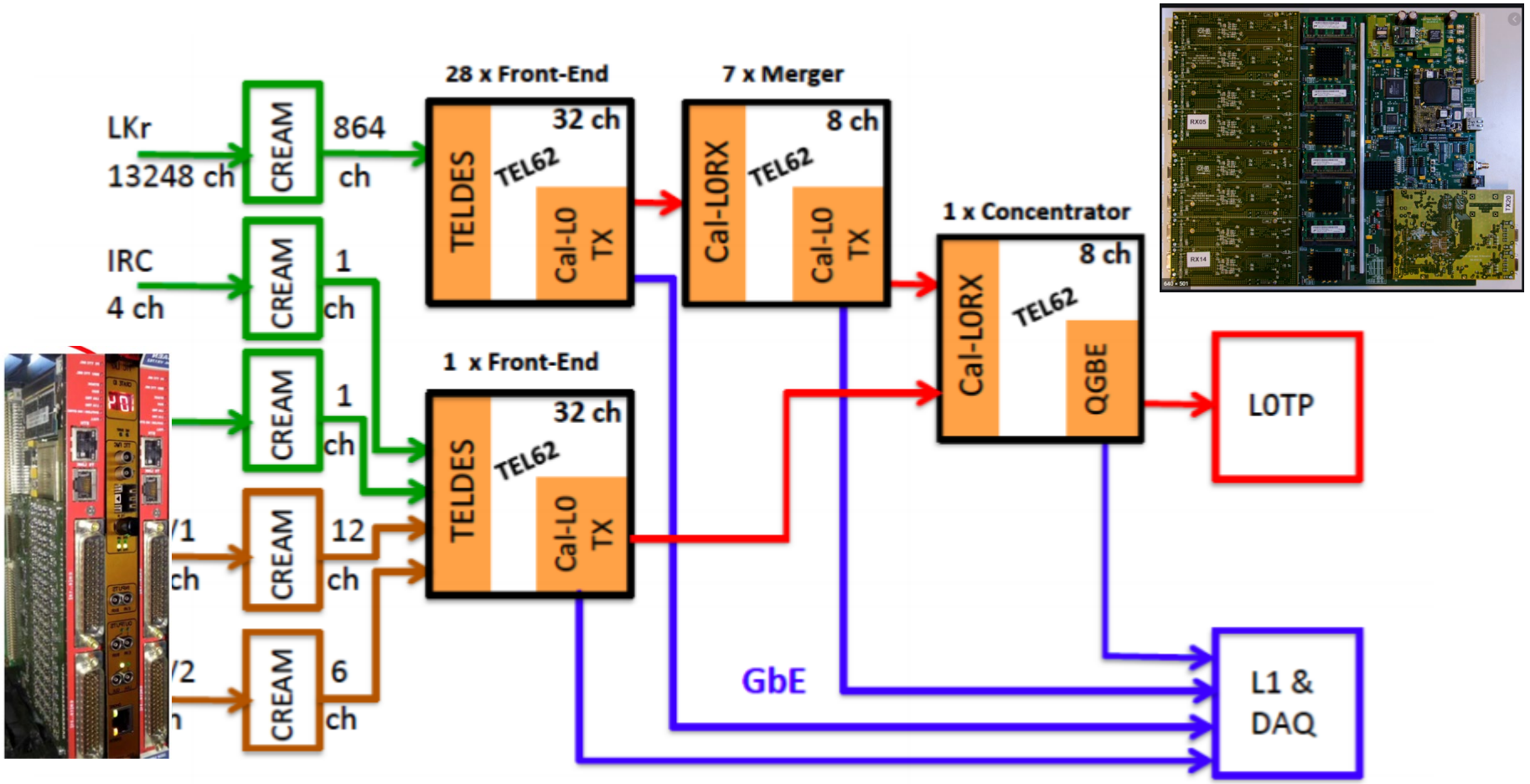
FAST ADC (> 1 GHz) 4/5

- Calculate parameters in real-time is in principle doable ... (better with 2030 FPGA)
- An FPGA could be splitted in a square of n x n «engines»
  - Each engine receives samples relative to one hit and fits the parameters.
  - All engines work in parallel (like a custom made highly optimized GPU, with no latency due to bus sharing etc etc)
  - Each engine could be programmed using HLS compilers and OpenGL ...
  - We did something similar some years ago implementing the Retina algorithm in an FPGA to perform track finding in real time



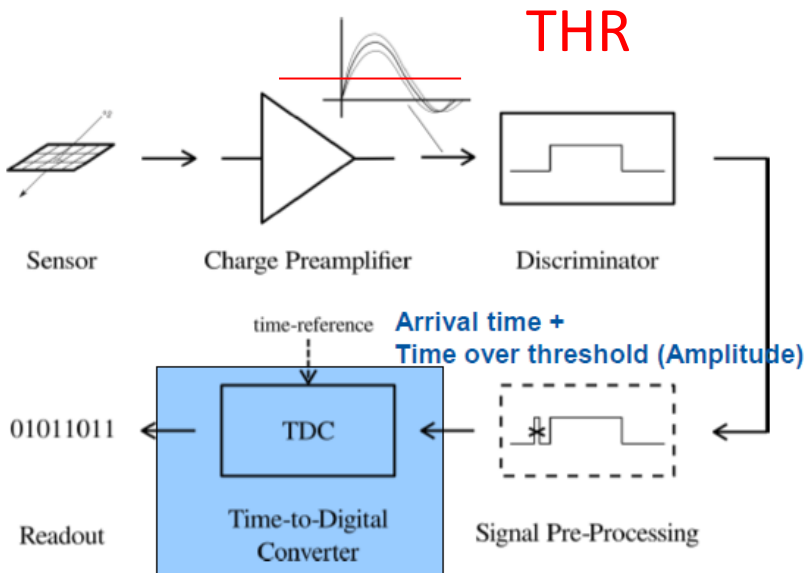
FAST ADC (> 1 GHz) 5/5

- Mixed readout (primitives + raw data) is implemented in the NA62 calorimeter readout system (CAEN CREAM digitizer boards + TEL62)



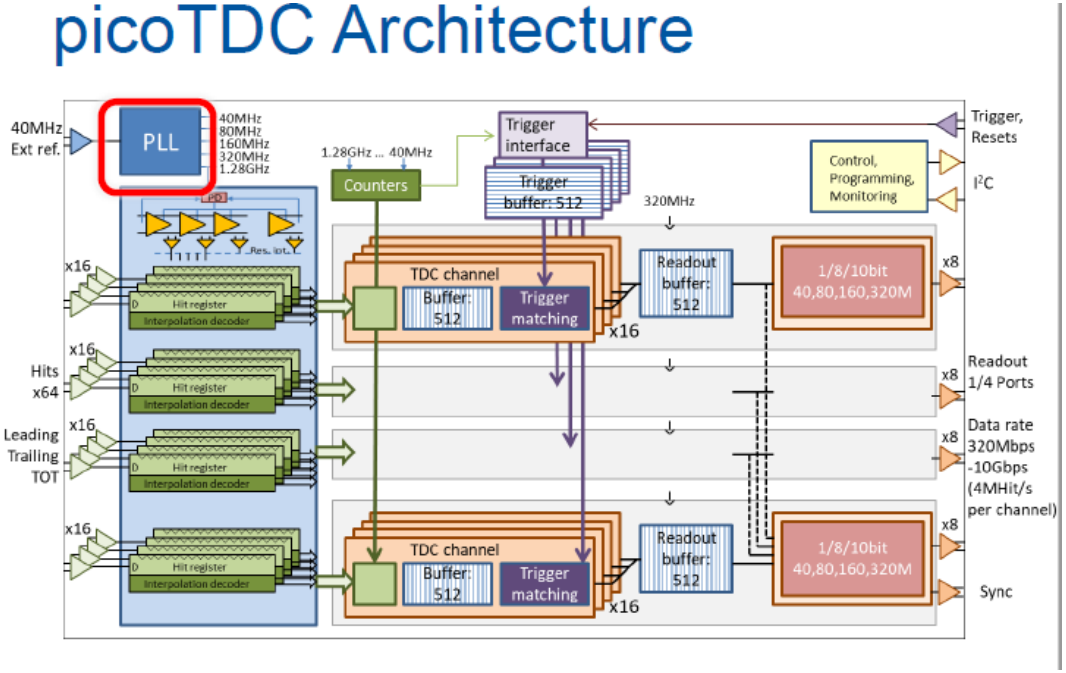
TDC 1/4 TDC

- TDC solves a lot of issues toward ADC:
- Only 2 words/hit (start/stop TimeOverThreshold)
- Very good time resolution
- Energy resolution o(10%) could be reached (all hits have same shape scaled with energy)
- Very high integration scale, low power, low cost, rad hard (next slide)
- BUT:
- Does not solve pile-up (easily ...) ...



TDC 2/4 CERN PicoTDC

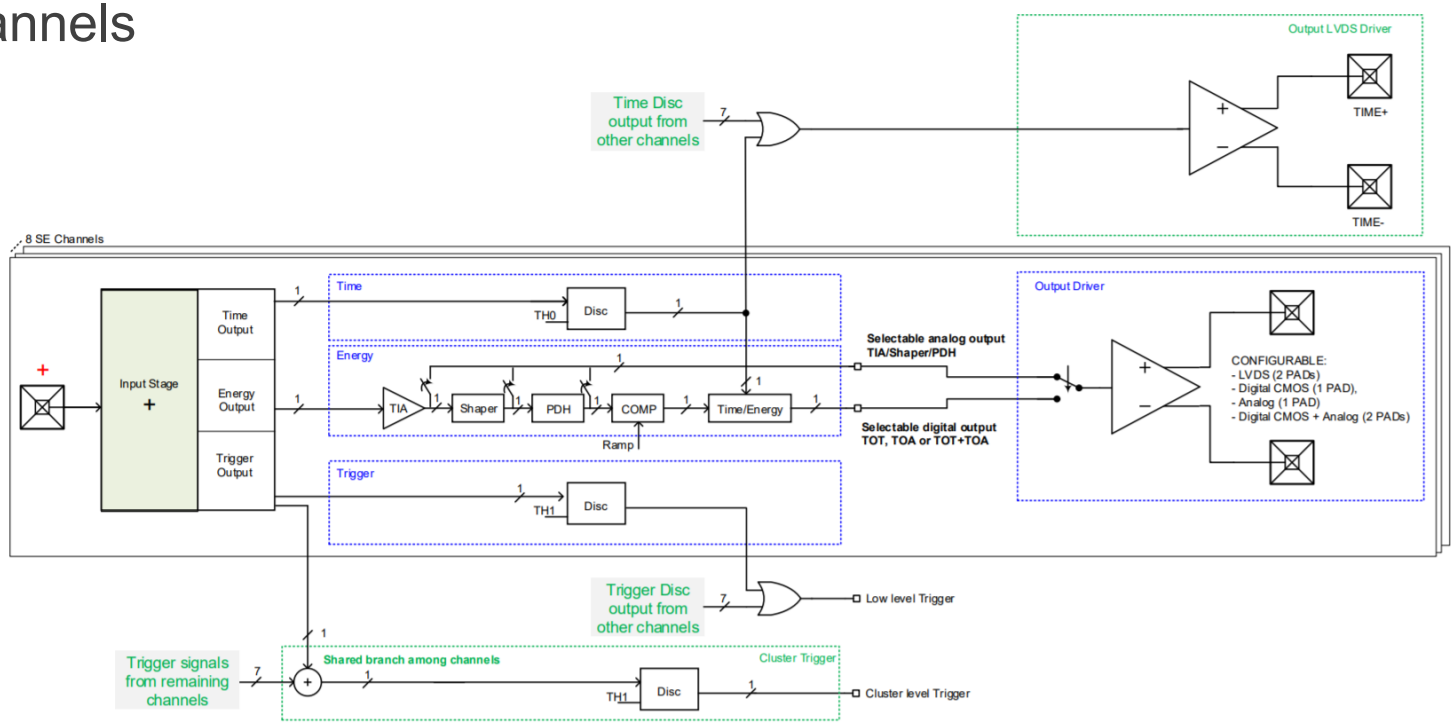
- CERN is developing a new RadHard ADC (samples available)



- 64 channels /chip
- 3 ps resolution RMS (12 ps low resolution mode)
- Rad hard
- Relatively cheap (1-2$ /channel)

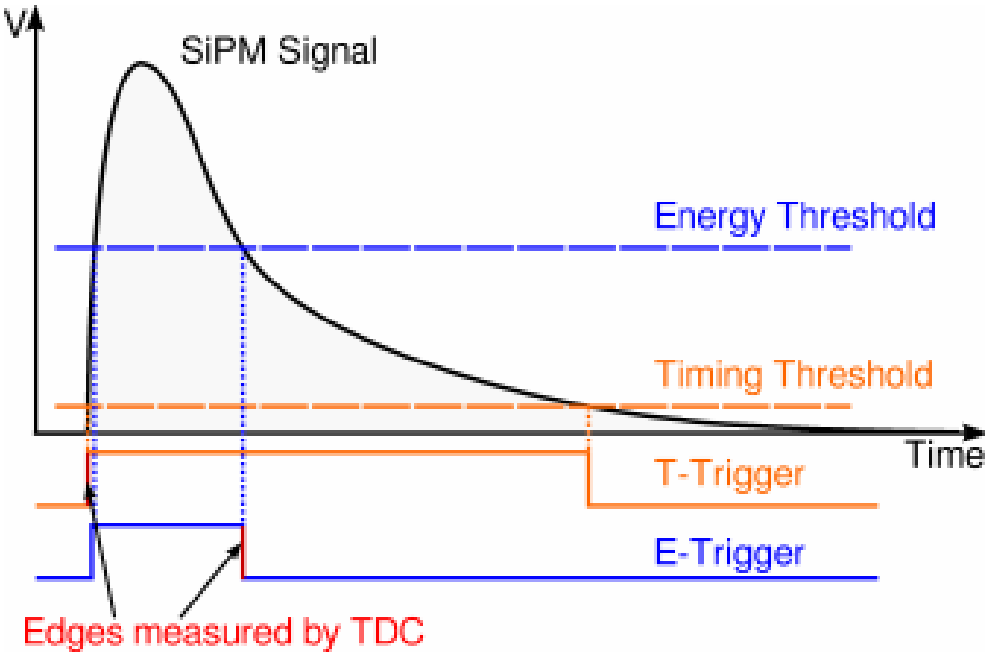
TDC 3/4 FastIC: PicoTDC companion chip (disc.)

- Discriminator with variable threshold
- Additional peak amplitude to time converter to measure energy could help to track pile-up
- Fast OR to be used as trigger
- 4 channels



TDC 4/4 Double threshold discriminator

- TDCs are cheap ... And Ecal has not so many channels ...
- We could send the same detector signal to 2 discriminators with different threshold
- Technique already used by NA62, improves time resolution and energy resolution. Maybe helps to recognize pile-up ?
- 3 thresholds ?



TDC + “slow” ADC 1/

- To solve pile-up problem we could use a TDC (PicoTDC) + a relatively slow ADC.
  - How much slow ? If signals o(30 nsec) 100 or 200 Msamples should be ok.
- Bandwidth not too high (3 or 4 ADC samples /hit)
- We could still try to fuse TDC and ADC data on the flight and directly send hit parameters to DAQ ...

Radiation hardness ...

- Mu2eII Integrated dose around 1 Mrad
  - PicoTDC ok ...
  - FPGA ? Today (2020) only Xilinx Virtex5-QV space grade FPGA are qualified for dose 1 MRad(Si) but $$$$$$$
  - ADC ? Need to be qualified ...

Conclusions

- The type of detector that will be chosen for the Mu2eII ECAL will drive also the design of the readout system ...
  In any case it will be challenging ... Several architectures needs to be carefully evaluated
- We will need a lot of simulations and laboratory R&D to choose the best solution in terms of performance and cost ...