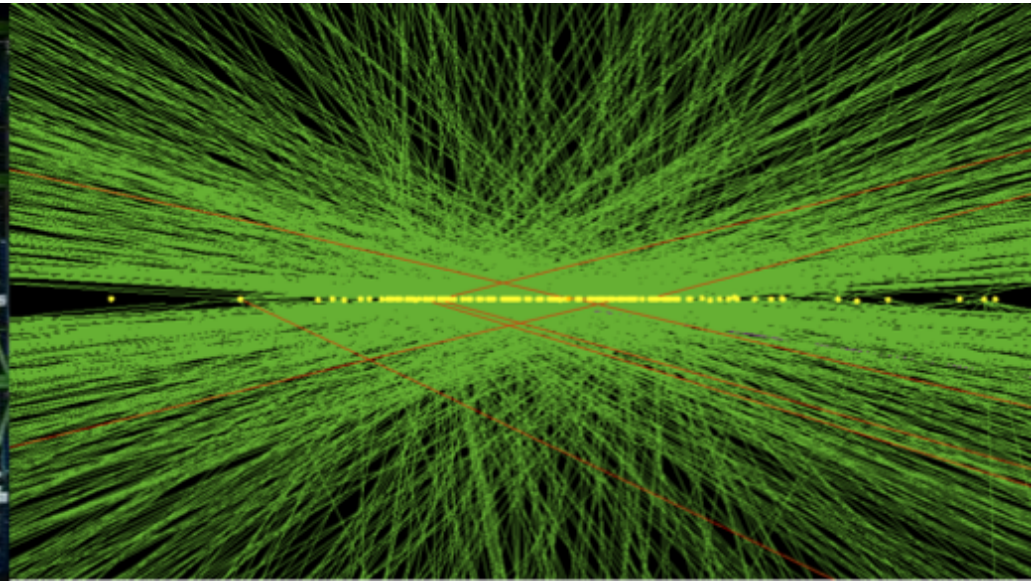
ETROC Status

Ted Liu (Fermilab)

Sept 14th, 2020



ETROC: ETL ReadOut Chip

ETROC bump-bonded to LGAD,
To handle 16x16 pixels
Each 1.3 mm x 1.3 mm

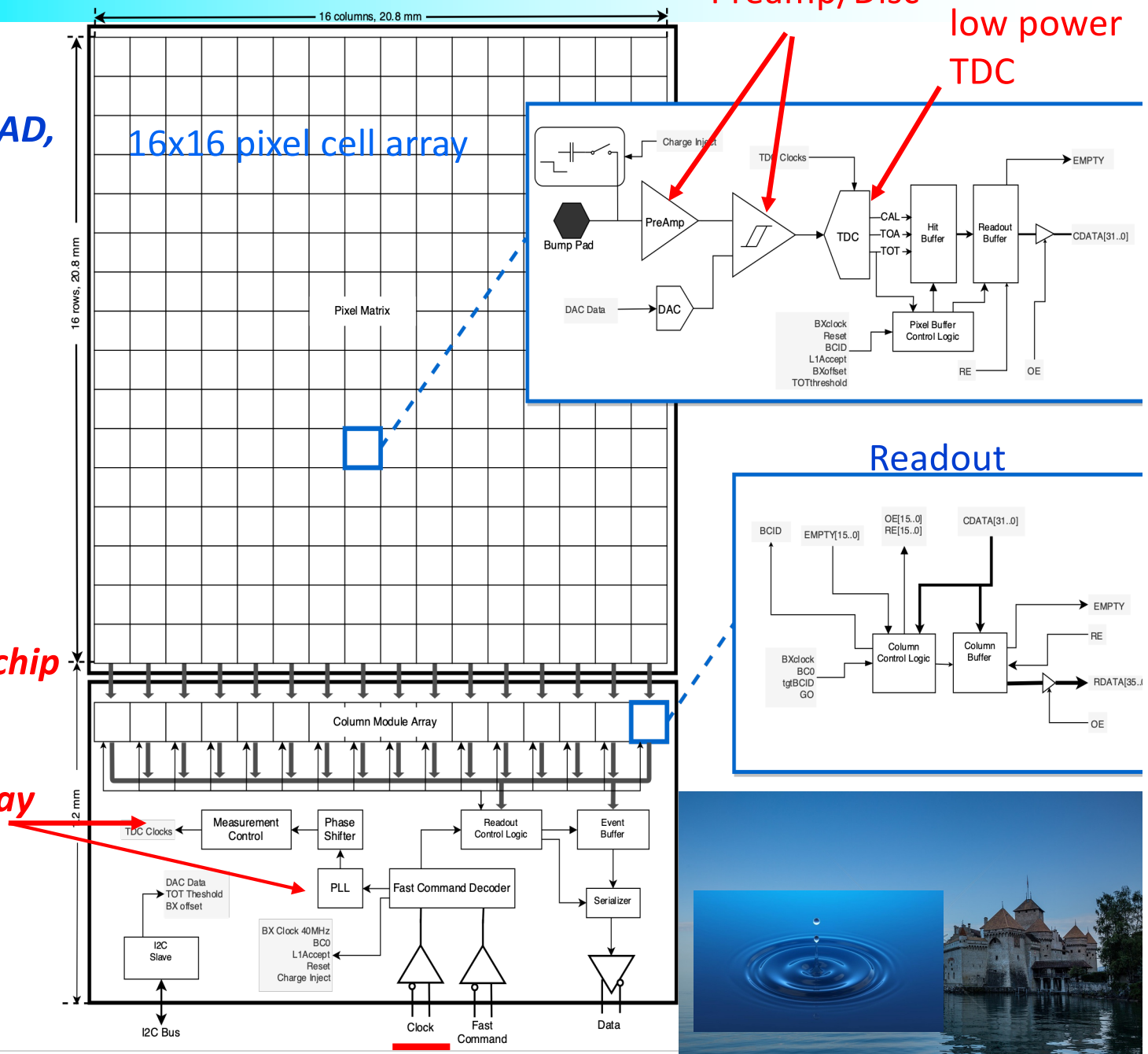
Requirement:
ASIC contribution to
time resolution < ~40ps

Deal with small signal size
(~20fC down to ~6fC)

Power consumption < 1W/chip
L1 buffer latency: 12.5 us

clock distribution all the way
into each pixel
On-chip PLL

Desirable to have
waveform sampler for 1-2 pixels
for monitoring/calibration purpose



ETROC Development: *divide & conquer*

ETROC0: 1x1 pixel channel with preamp + discriminator (submitted Dec 2018)

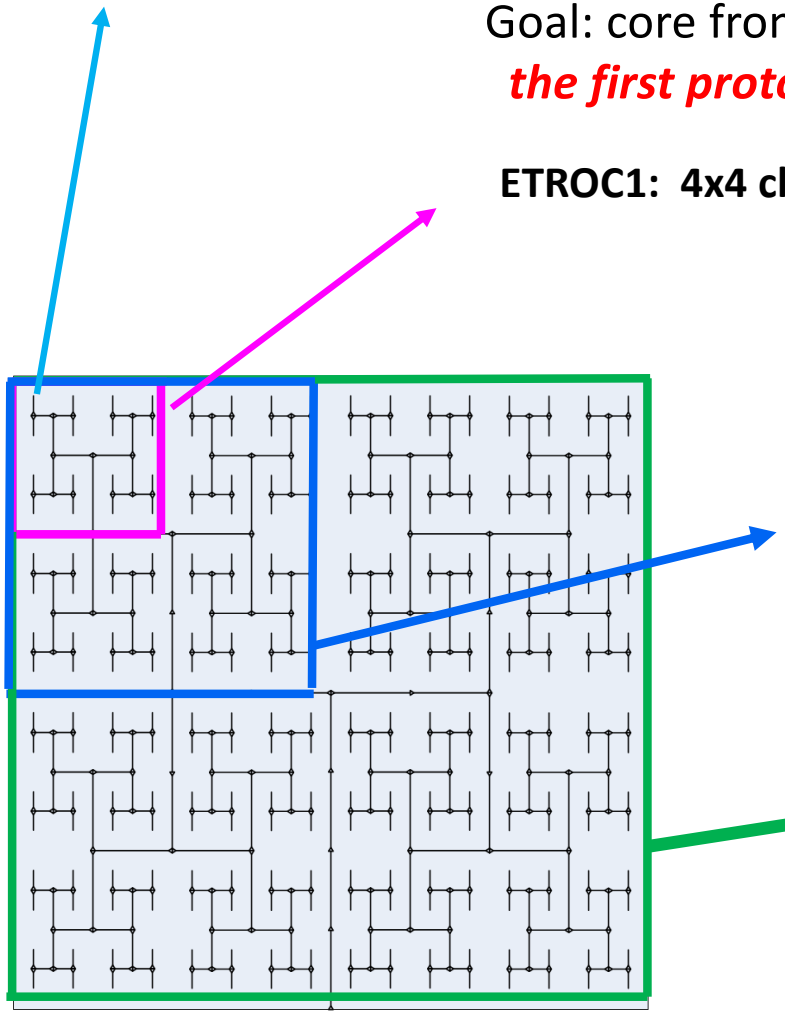
Goal: core front-end analog performance

the first prototype chip works well and agrees with simulation

ETROC1: 4x4 clock tree, preamp + discriminator + TDC (submitted Aug 2019)

Goal: full chain front-end with TDC, 4x4 clock tree

This is the first full chain precision timing prototype



16 x 16 clock H-Tree

ETROC2: 8x8 → 16x16, *full functionality* (Q1 2021)

Aug 2021 (Covid delay)

Goal: supporting circuitries, clock tree

PLL, phase shifter, fast/slow control, I/O, L1 buffer…

ETROC3: 16x16 (full size): (Q1 2022)

Oct 2022

Goal: full size with full clock tree

We have followed this plan since project started (Sept. 2018) …

Timeline: ALTIROC vs ETROC

ATLAS HGTD

- ALTIROC0-v1
  - Started early 2016
  - Submission Dec 2016
- ALTIROC0-v2
  - Submission Dec 2017
- ALTIROC1-v1
  - Submission June 2018
- ALTIROC1-v2
  - Submission Feb 2019
- ALTIROC1-v3
  - Submitted April 2020
- ALTIROC2-v1
  - Submission scheduled Nov 2020

A few months

CMS ETL

ETROC design started (from scratch) about ***2.5 years later*** than ALTIROC…

In addition, with waveform sampler

- ETROC0 (3 months)
  - Started Sept 2018
  - Submission Dec 2018
- ETROC1 (7 months)
  - Submission Aug 2019
- ETROC2
  - Scheduled for Q1 2021
    - COVID delay to Aug 2021

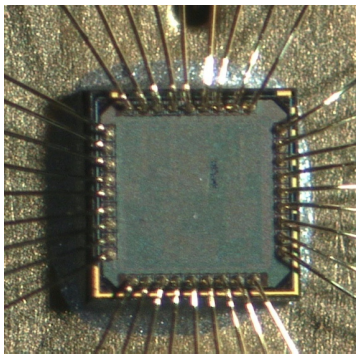
Other ETROC chips:
Single channel ADC (May 2019)
Waveform sampler (March 2020)
PLL mini-ASIC (May 2020)

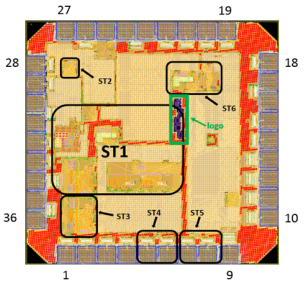
Outline: ETROC status

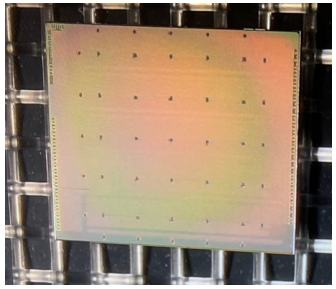
- ETROC development strategy and plan
- ETROC0 status (front-end)
- ETROC1 status (front-end + TDC)
- ETROC Waveform Sampler prototype status
- ETROC PLL prototype status
- ETROC2 design status
  - ***All critical components have been prototyped (above)***
  - The rest of digital blocks and system interfaces being implemented and prototyped in the ETROC emulator
    - ETROC emulator status

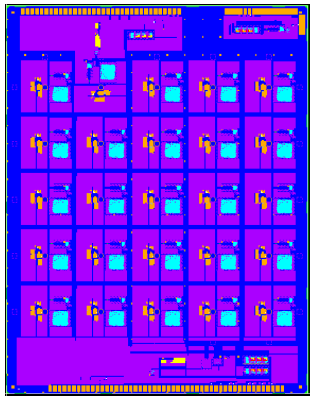
From ETROC0 to ETROC1 to ETROC2/3

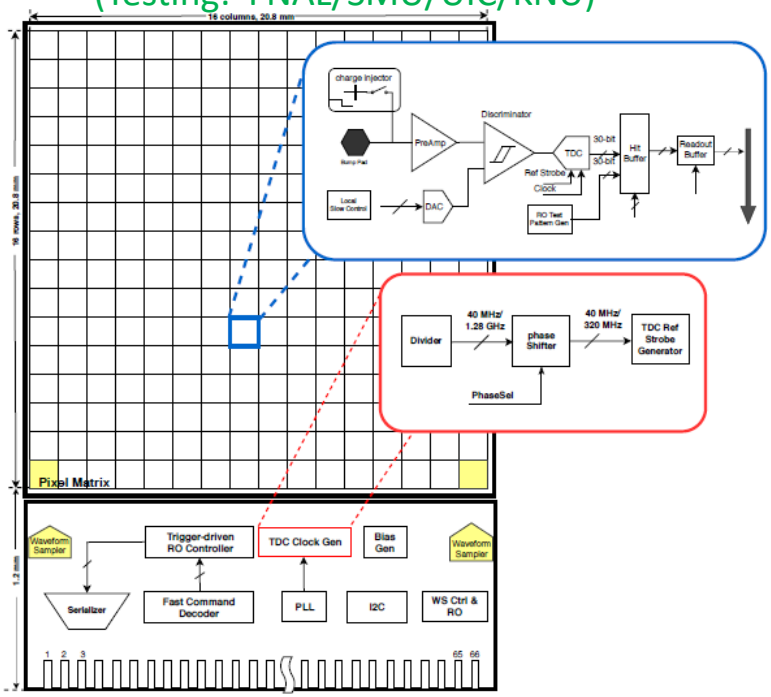
ASIC designers from FNAL/SMU
& in collaboration with lpGBT team
(Testing: FNAL/SMU/UIC/KNU)











ETROC0

- ***Submitted in Dec. 2018***
- Analog Front-end
- First round beam test early 2020, reached ~30ps
- good

ETROC1

- ***Submitted in Aug. 2019***
- 4 X 4 pixel array with full front-end including TDC
- Chips received middle Dec 2019
  - TDC block: good
  - Full chain: good
  - Laser: just started

ETROC2

- ***Aim to submit in Aug 2021***
- Designed to be compatible with 16 X 16 pixel array with *full functionalities*
- *Key new design blocks:*
  - *Waveform sampler:*
    - *1st ADC mini-ASIC good*
    - *8-channel sampler chips received in May 2020 good*
  - *PLL: submitted in May 2020*
    - *Initial results promising*

ETROC3

- Aim to submit in Q3 2022
- Pre-production version

Since project started Sept 2018,
Designed 5 different kinds of prototype chips
to address different design challenges:

All successful

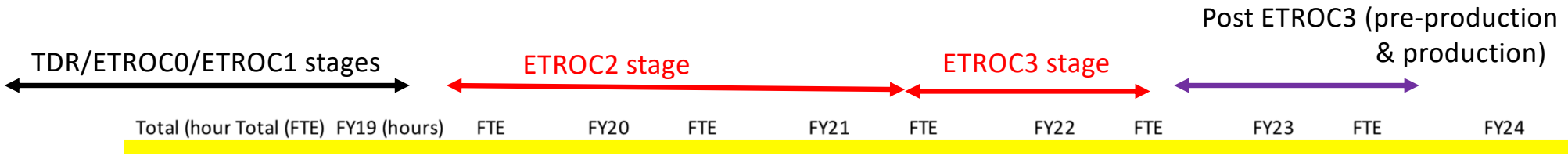
ETROC prototyping status

- ETROC0
  - Charge injection done
  - Cosmic done
  - Laser testing done
  - TID test to 100Mrads done
  - Beam testing ~30ps achieved in beam
- ETROC1 (good progress made despite COVID delay)
  - TDC extensively tested: excellent performance (<~6ps resolution)
  - Full array full chain ETROC1 charge injection testing: results good
  - ETROC1 and 5x5 LGAD sensor bump-bonded
    - ***Laser testing (on going) followed by beam testing (Dec – Feb 2021)***
- Waveform sampler prototype: works well
- PLL mini-ASIC chips***: first day test results promising***
- ETROC emulator: *design completed, firmware advanced*
  - ***fast command decoding, pixel DAQ readout, system interfaces***
    - ***The main digital blocks being prototyped in the emulator***

Summary (after two years very hard work)

- ETROC0 status summary: front-end good (TID & beam)
- ETROC1 status summary: front-end+TDC good
  - TID and SEU test to be done
  - Beam test to be done (need more bump-bonded with sensors)
- Waveform Sampler prototype chips: good
  - TID test to be done
  - Testing/interfacing with ETROC0 preamp output
- PLL prototype chips: initial results promising (1st day test)
  - TID and SEU test to be done (collaboration with lpGBT team)
- ETROC2 design status: marching forward
  - All critical components are prototyped
  - The rest of the digital circuitries and system interfaces are *being implemented/prototyped in ETROC2 emulator*
    - *To be tested with the system (including backend) soon*

ASIC resource needs in FY21 and beyond



ASIC resources needed (designers + EE students)	4	4	~1
Quan Sun (FNAL) full time on ETROC	1.0	1.0	~0.5
Datao Gong (SMU)	0.5	0.5	~0.2
SMU EE students	?	?	?
Design verification effort mostly needed from FNAL	1.5	1.5	

Production expected Year 2024

- Note: additional ETROC revisions are reserved in risk registers. So the numbers above should be considered as minimal… and may need more in FY23 and FY24

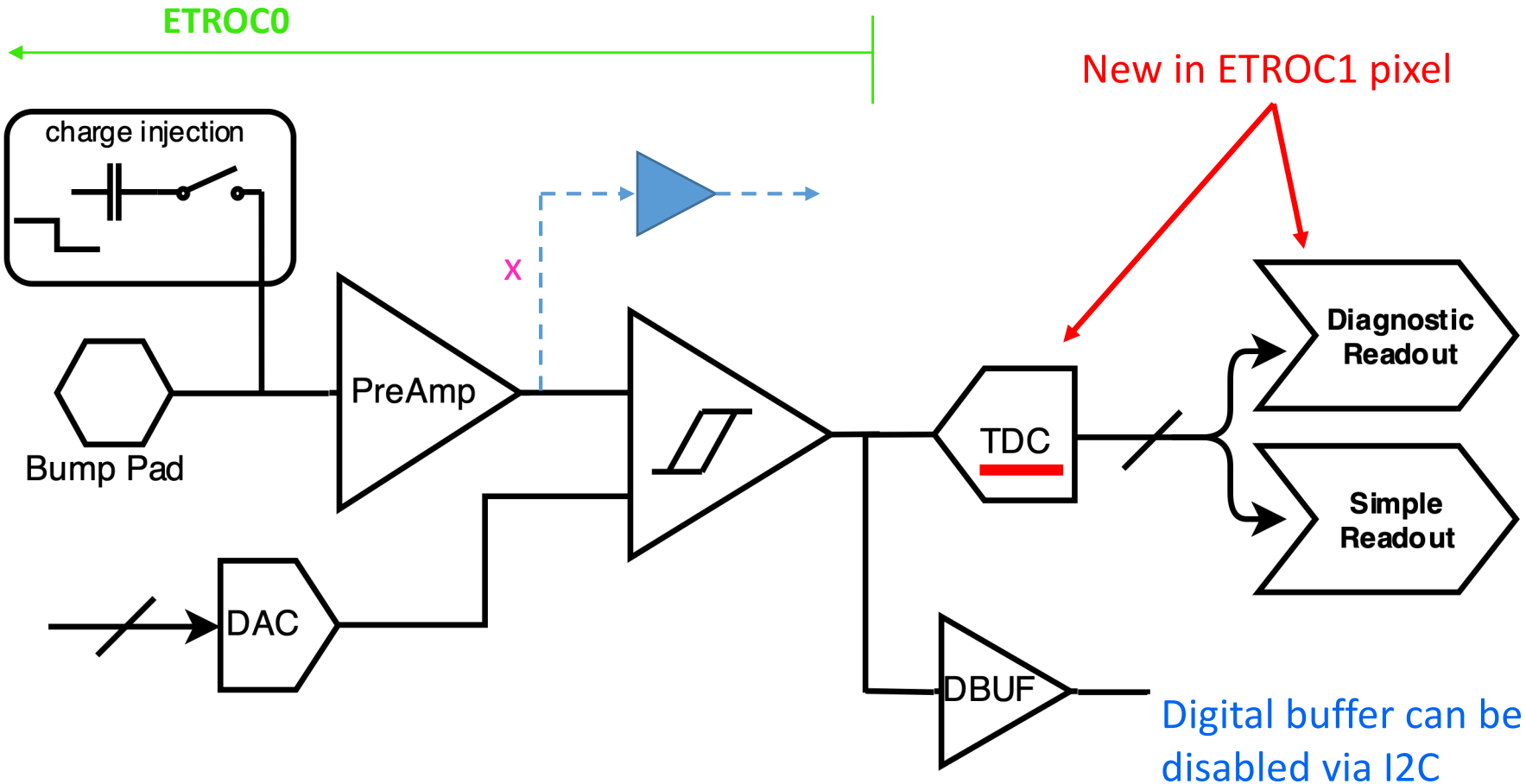
  tons of testing work to be done in FY21, 22 and 23.
  resource needs for testing not included here

Backup: Highlights of testing results in 2020

- ETROC0 beam test
- ETROC1 TDC prototype test
- ETROC1 4x4 array prototype test
- Waveform sampler prototype test
- PLL mini-ASIC prototype test
- ETROC2 design status
  - ETROC2 Emulator prototype in FPGA

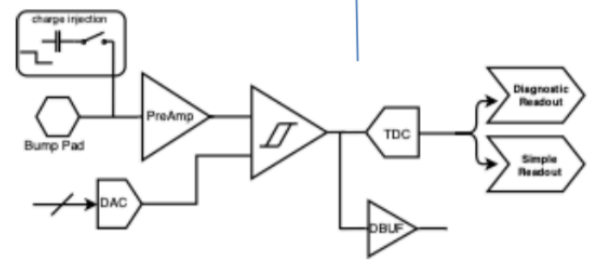
ETROC1 pixel: uses ETROC0 front-end

ETROC0 is used directly in ETROC1



The TDC is brand new design (low power)
~ one year development effort

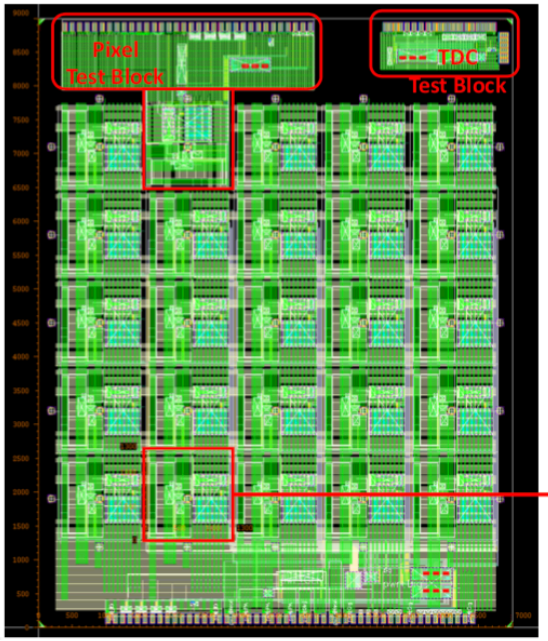
ETROC0



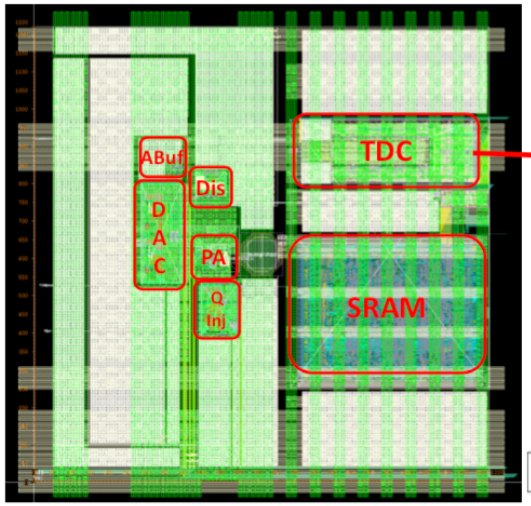
Extensive design verification has been done, mostly by EE students.

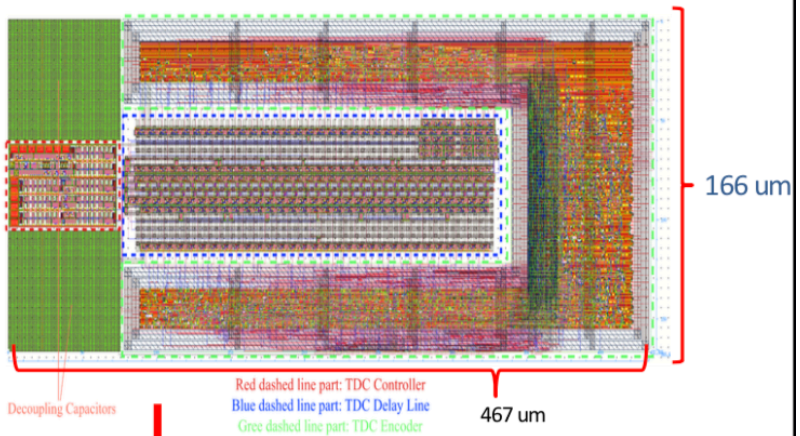
Low power TDC: <0.1mW

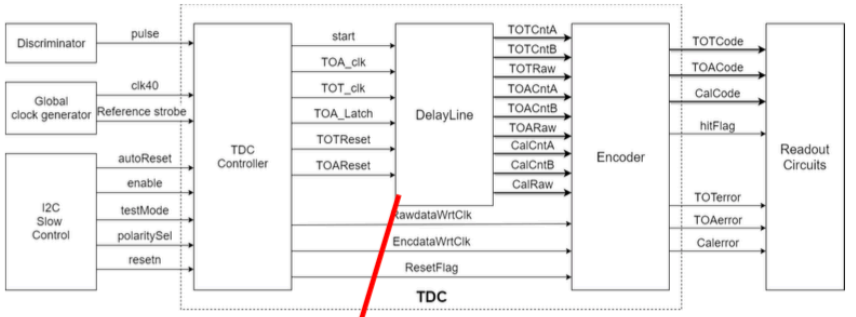
ETROC1 Top Layout



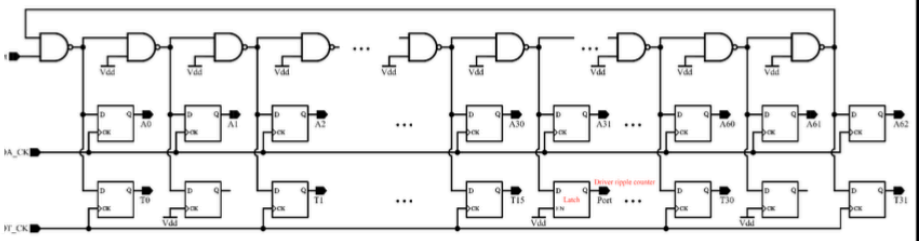
ETROC1 Single Pixel Layout







TDC core logic: gated ring oscillator

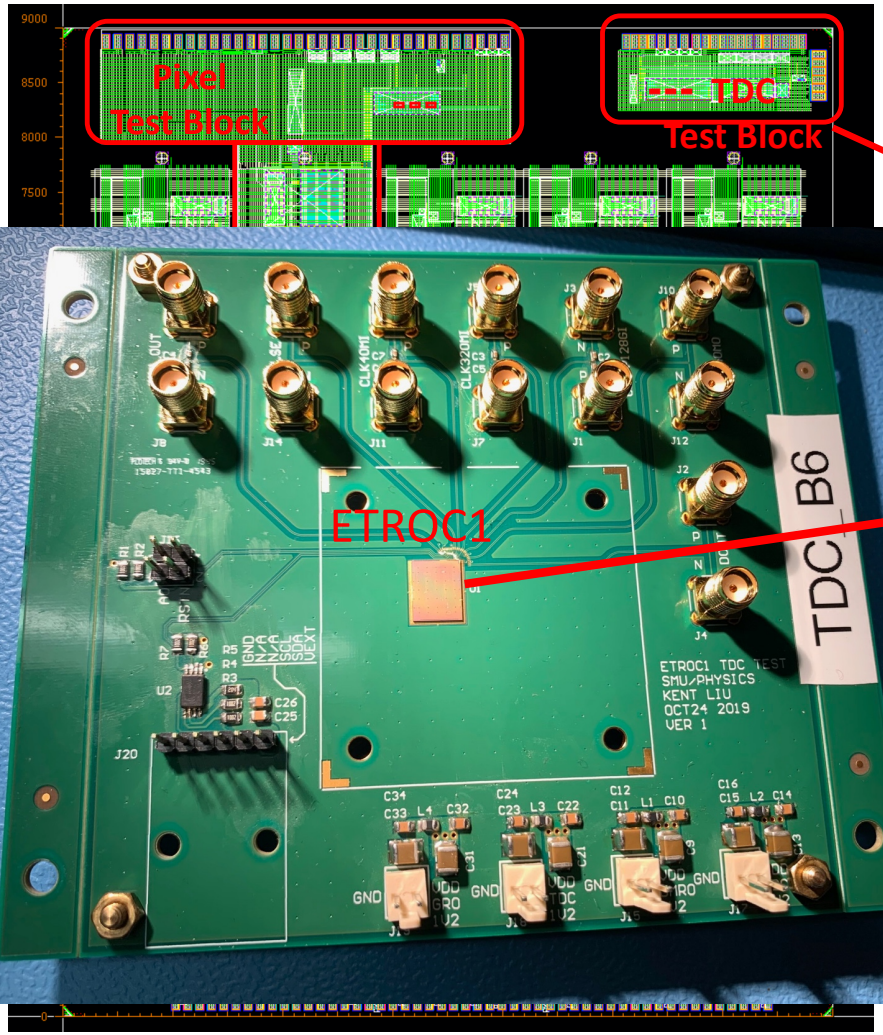


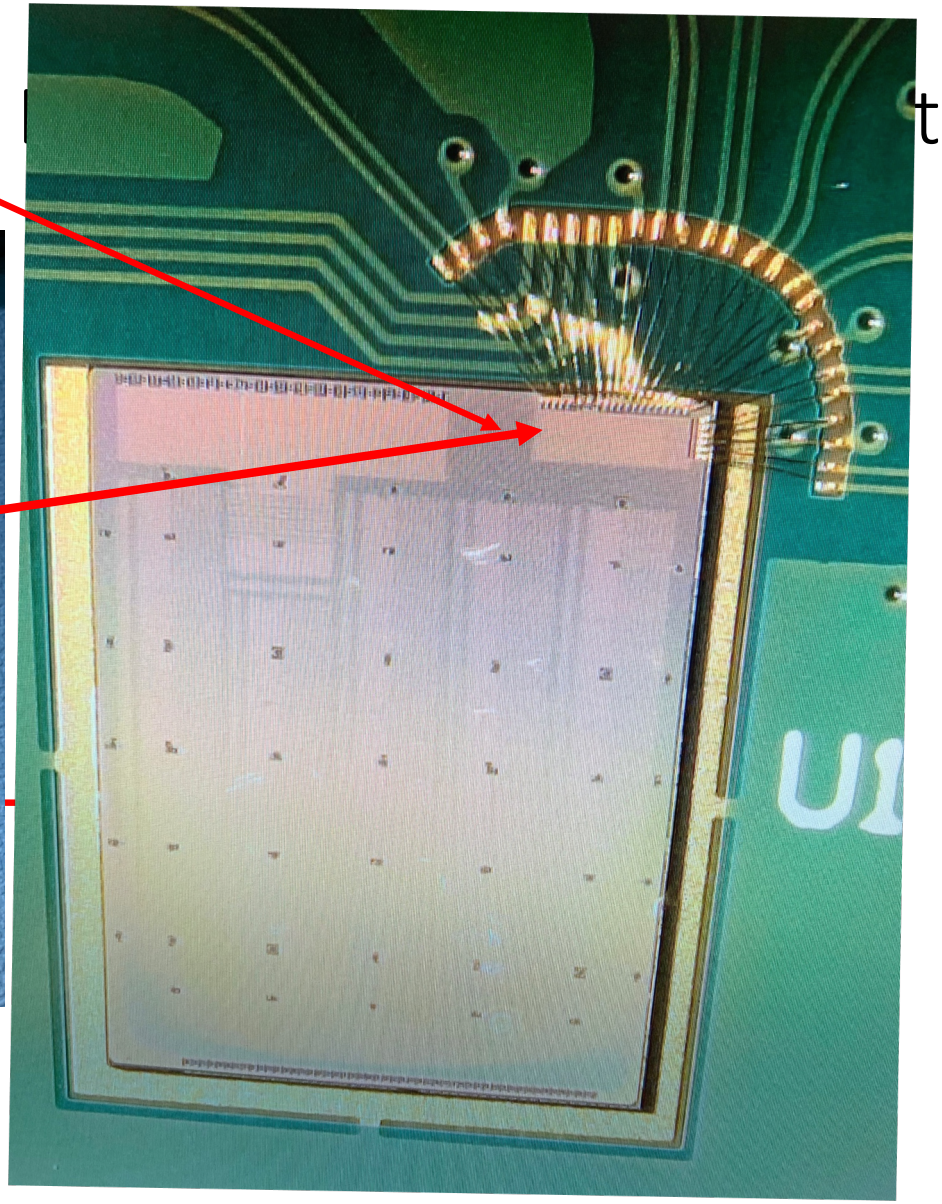
ETROC1 TDC Design

- TDC requirements
  - TOA bin size < ~30ps, TOT bin size < ~100ps
  - Lower power highly desirable
    - ***ETROC TDC design goal: < 0.2mW per pixel***
- ETROC TDC design optimized for low power
  - A simple delay line without the need for DLL's to control individual delay cells, with a cyclic structure to reduce the number of delay cells, to measure TOA & TOT at the same time
- ***In-situ delay cell self-calibration technique***
  - For each hit, will use two consecutive rising clock edges to record two time stamps, with a time difference of the known 320 MHz clock period: 3.125ns
  - Crucial to reach the required precision using a tapped delay line with uncontrolled delay cells (thus lower power)

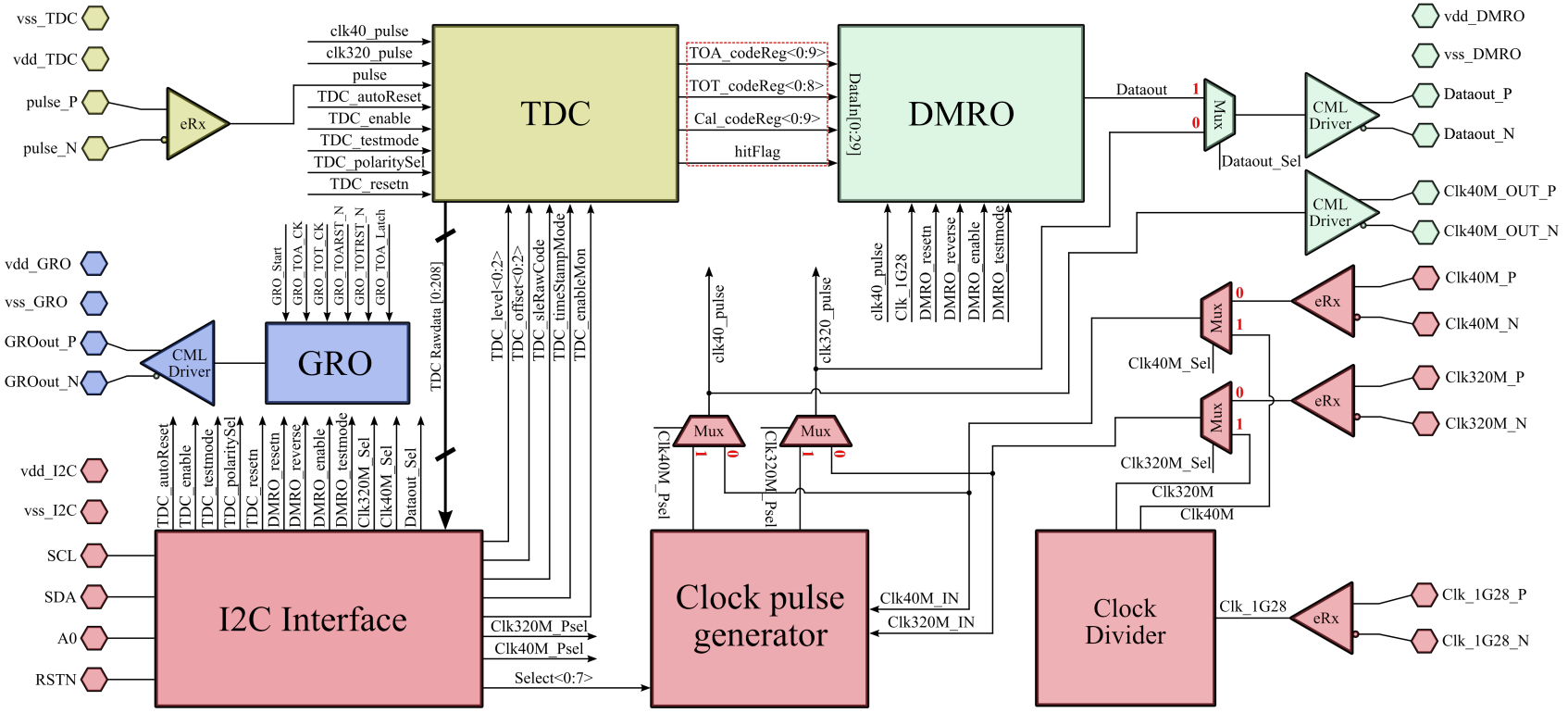
ETROC1 TDC standalone testing

ETROC1 Top Layout





Standalone TDC test setup at SMU



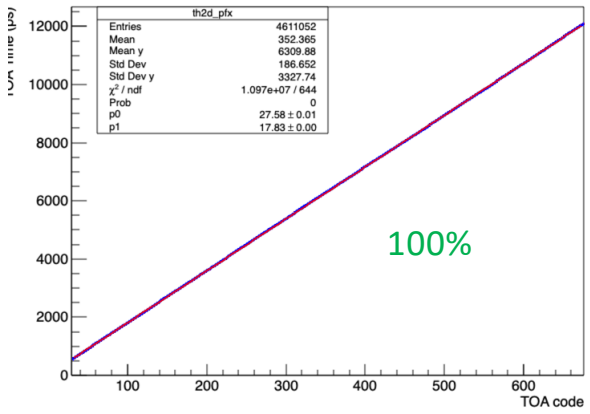
DMRO: Diagnostic Mode Readout

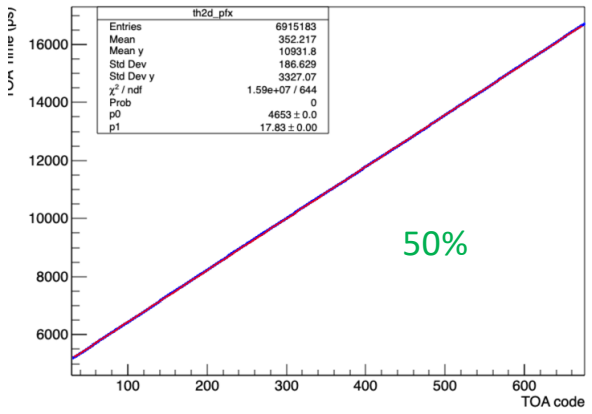
- Except the TDC core, the standalone TDC module also includes: GRO, BMRO, I2C slave and clock system.

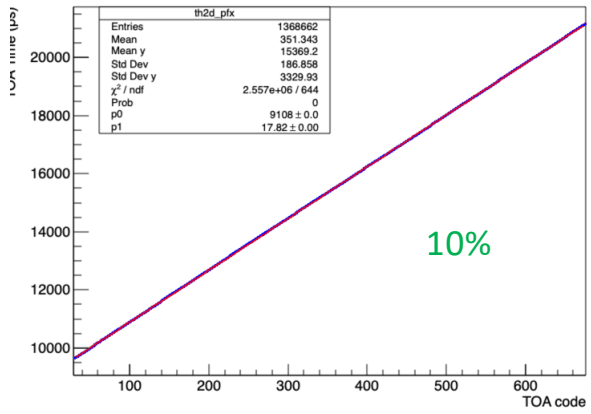
Bin size and transfer function

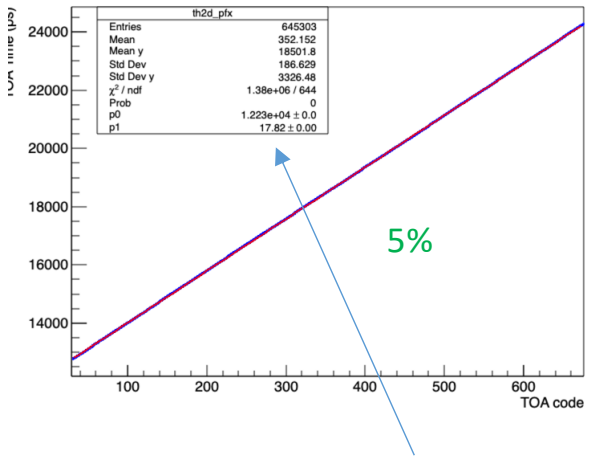
At different hit occupancy

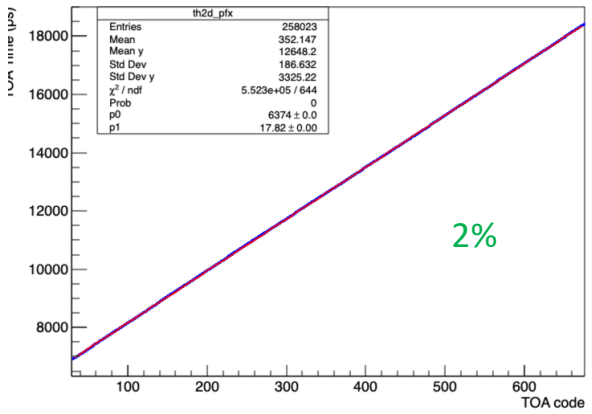
For ETL, expected hit occupancy: ~1% up to a few %

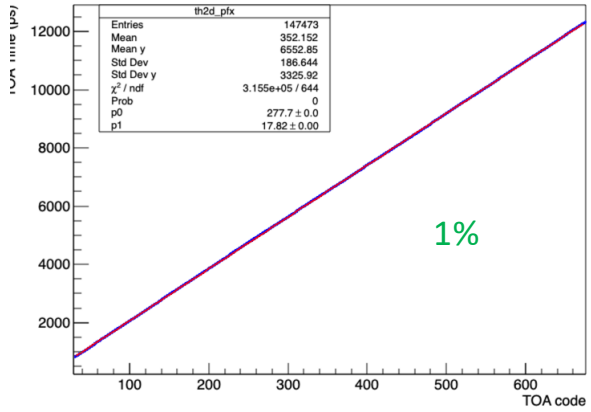










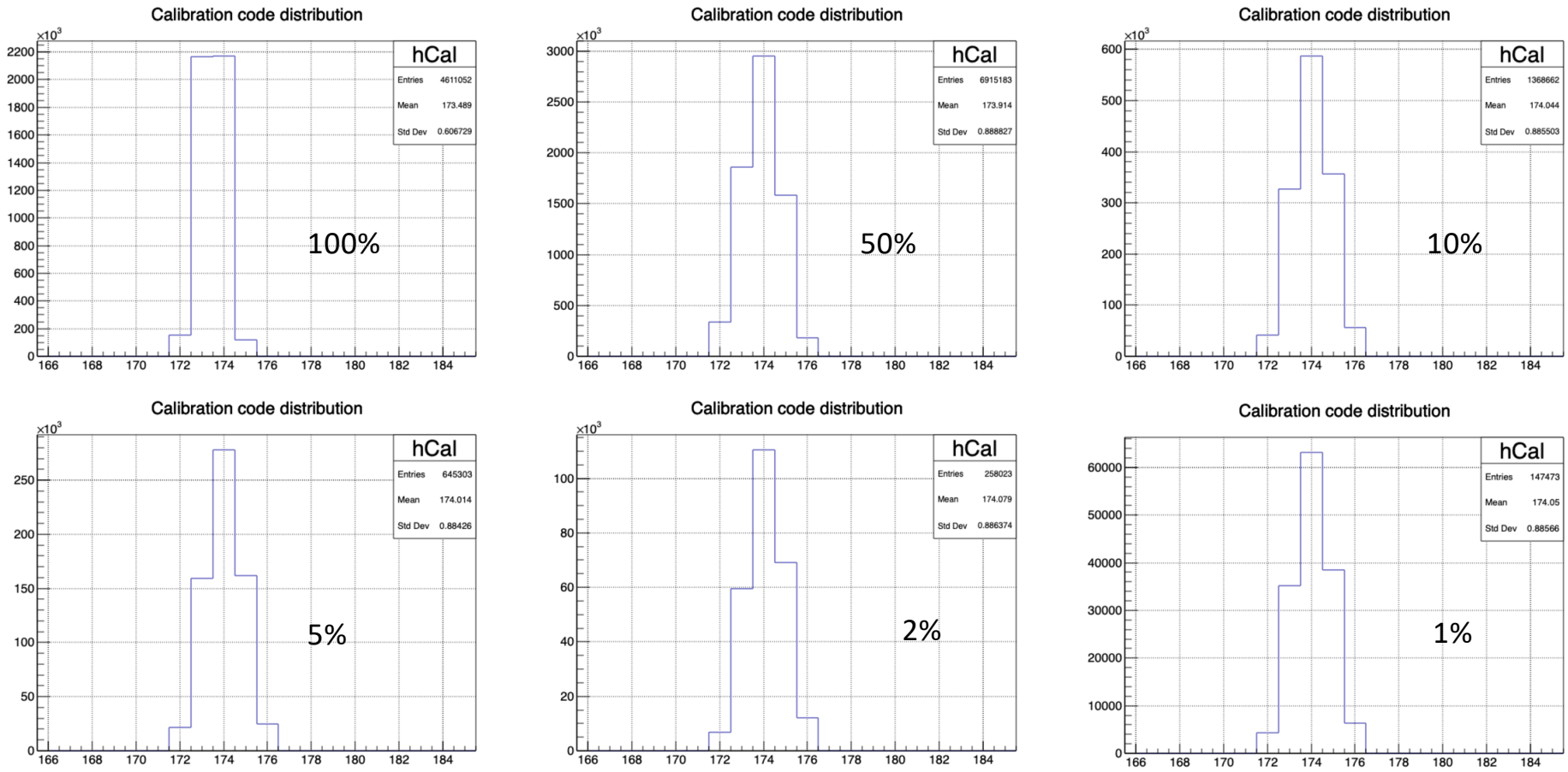


TDC bin size is measured to be: 17.82ps (design goal: <30ps)

Self-Calibration code: double snapshots/timestamps

At different hit occupancy

For ETL, expected hit occupancy: ~1% up to a few %



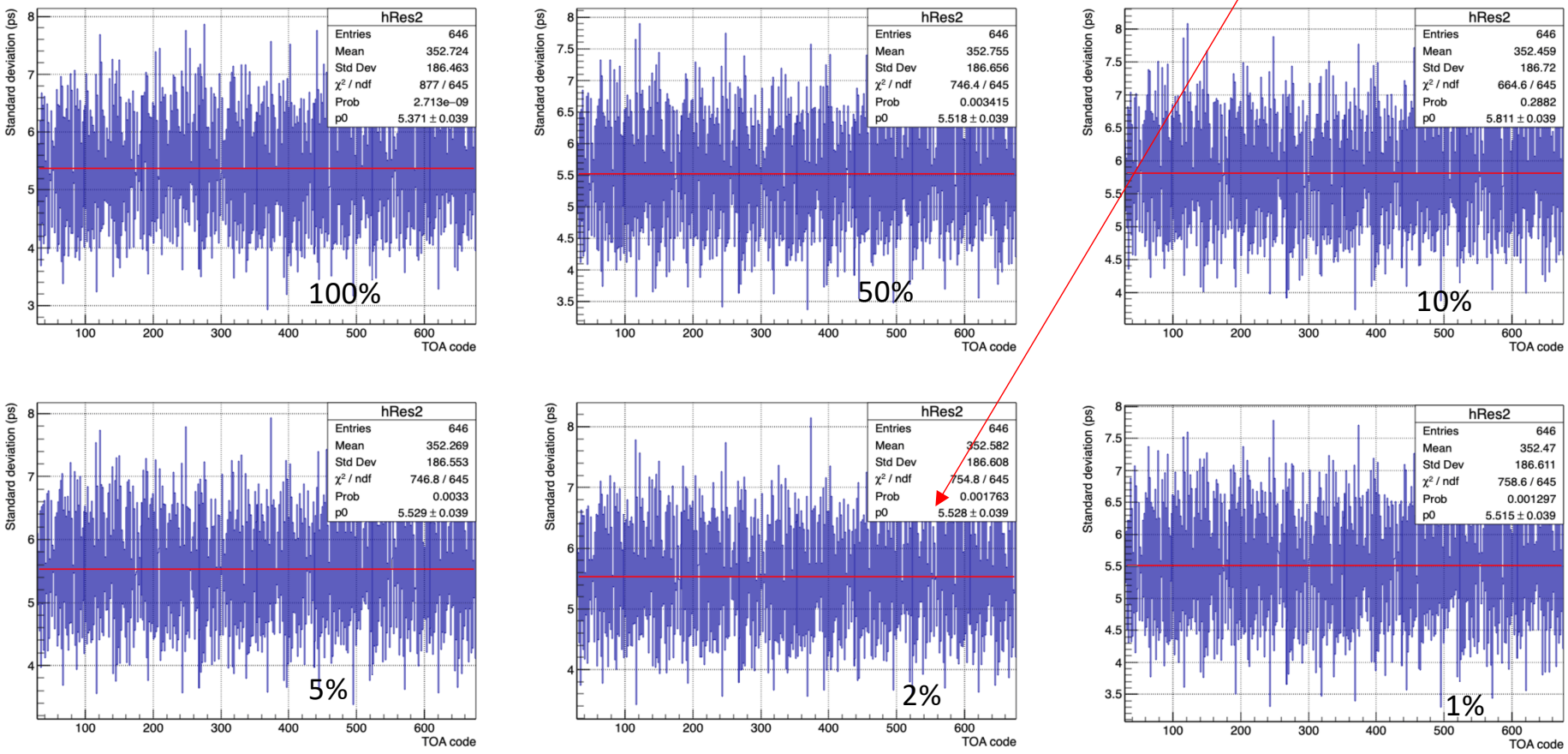
TDC bin size derived from calibration is consistent: ~18ps

320 MHz period (3.125ns) / 18ps ~ 174

TDC Precision vs occupancy: achieved ~ 5.5ps

At different hit occupancy

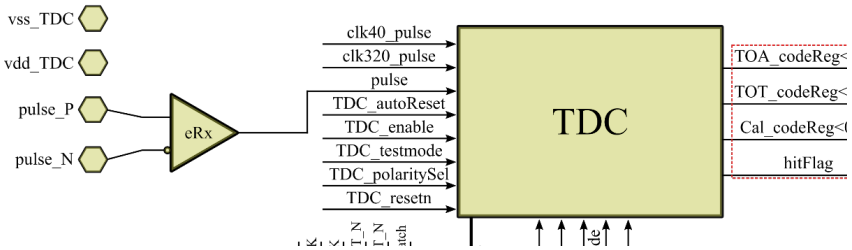
For ETL, expected hit occupancy: ~1% up to a few %



TDC bin size: 17.83 ps /sqrt (12) → Quantization ~5.15ps

Precision dominated by quantization

Power consumption as expected

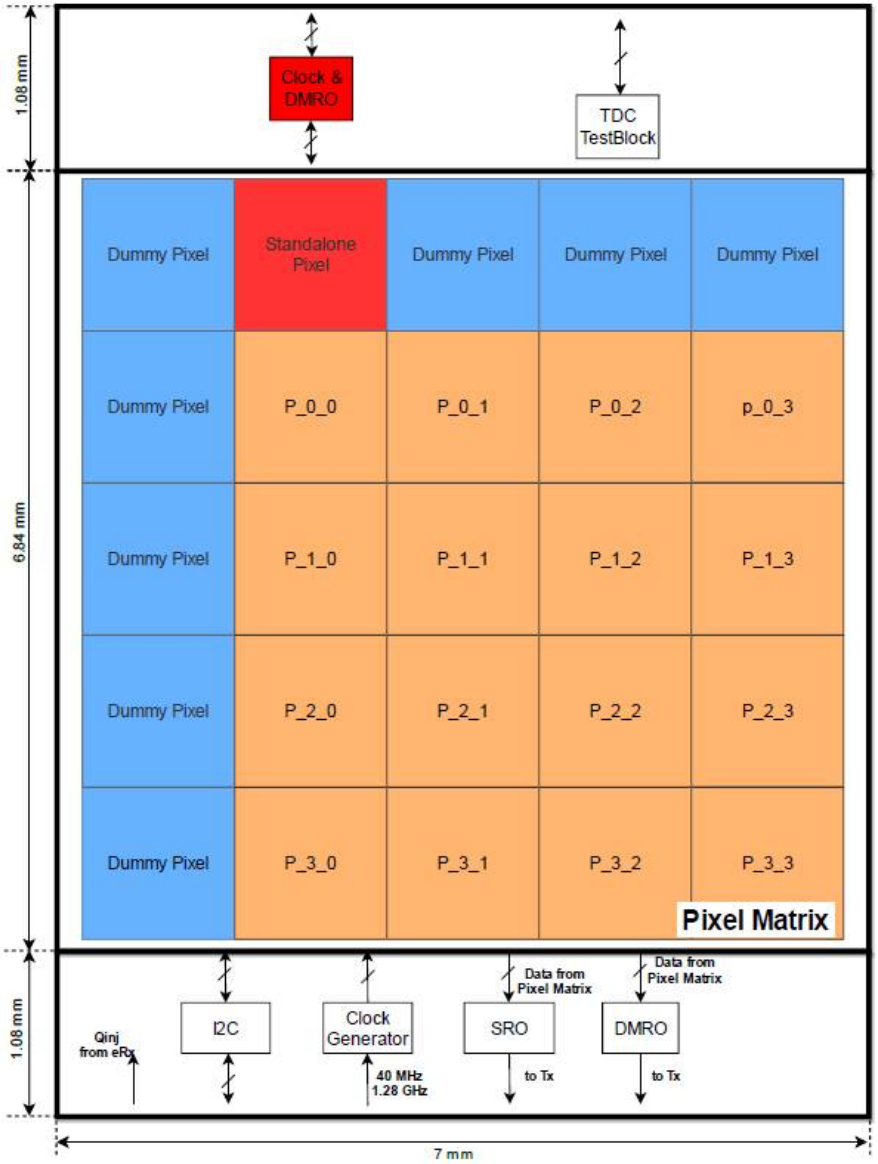


eRx status	TDC status	Current(mA)	Power components
on	on	3.170	$TDC_{sta}+TDC_{occu}+eRx_{on}$
on	off	1.132	$TDC_{sta}+eRx_{on}$
off	on	0.068	$TDC_{sta}+eRx_{off}$
off	-	0.007	eRx_{off} (Estimate from simulation)

- The power domain of TDC includes both eRx and TDC core, we measure their current directly from the power supply. Both TDC and eRx can be turned on/off by I2C interface.
- TDC power comprises of **standby power**, corresponding to power when input signal occupancy is 0, and **occupancy power** which proportional to occupancy of input signal.
- Input signal typical case: TOA: 3.125 ns, signal width(TOT): 6.25 ns
- The measured TDC **occupancy power** is **2.446 mW** = 1.2x(3.170-1.132);
- The current of eRx is estimated to be 7uA when it is off, the **standby power** of TDC is 73 = 1.2*(68-7) uW
- When occupancy is 100%, the TDC power is 2.519 = 2.446+0.073 mW
- When occupancy is 1%, the TDC power is 73+2446*1% = 97 uW (agree w simulation)

Design spec is: < 200uW at 1% occupancy

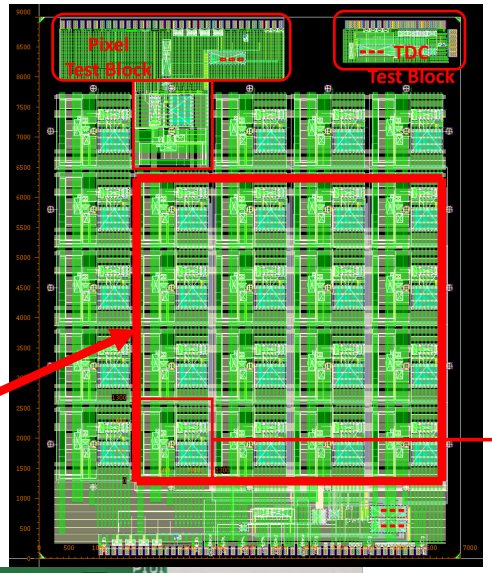
ETROC1 4x4 pixel array



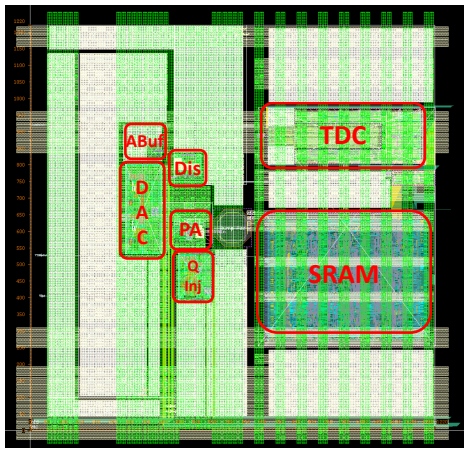
P_0_0 index: 0	P_0_1 index: 4	P_0_2 index: 8	P_0_3 index: 12
P_1_0 index: 1	P_1_1 index: 5	P_1_2 index: 9	P_1_3 index: 13
P_2_0 index: 2	P_2_1 index: 6	P_2_2 index: 10	P_2_3 index: 14
P_3_0 index: 3	P_3_1 index: 7	P_3_2 index: 11	P_3_3 index: 15
Chip peripherals			

ETROC1 4x4 array testing board

ETROC1 Top Layout



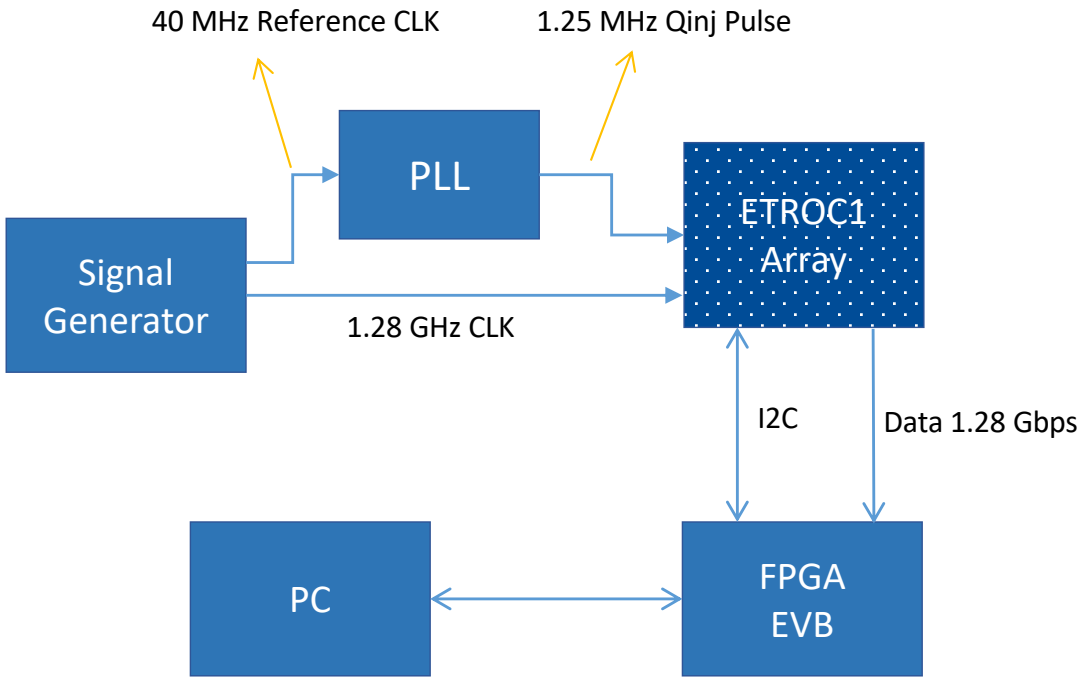
ETROC1 Single Pixel Layout



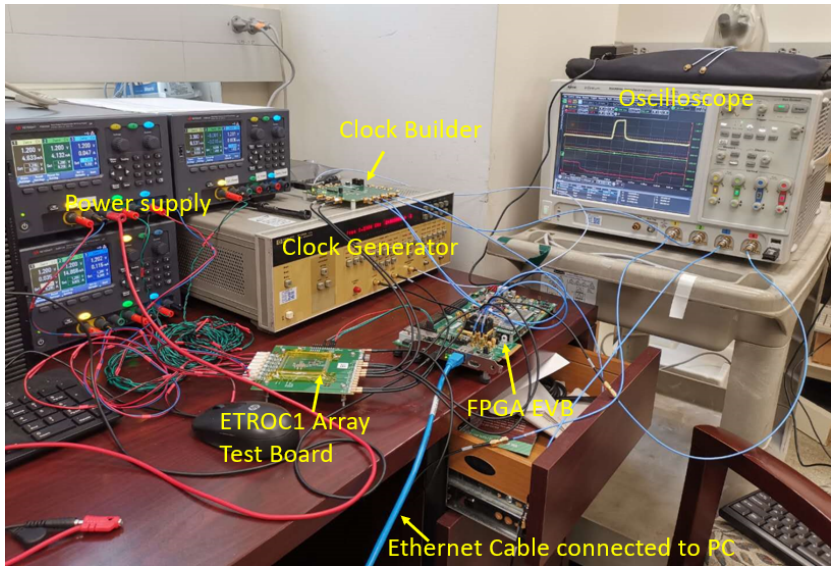
Test done so far with bare ETROC1 chips (good enough for initial charge injection testing).

ETROC1-LGAD bump-bonding at Barcelona (chips received last Friday)

ETROC1 4x4 array test-stand at SMU



Simplified block diagram of the test bench



ETROC1 Test at SMU

- 1.28 GHz clock as the input clock of ETROC1
  - generating lower frequency internal clocks
  - data transmission
- 1.25 MHz clock(pulse) for charge injection
  - In sync with 1.28 GHz clock
  - One discriminator pulse in 32 clock cycle
- 1.28 Gbps serial data sent to a FPGA EVB
- The FPGA EVB also acts as the I2C master
- A PC communicates with FPGA through ethernet
- The setup allows remote testing

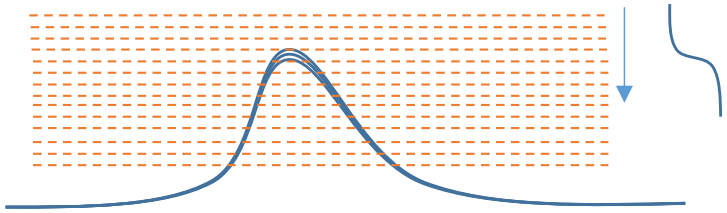
Test setup was prepared as soon as COVID lockdown opening up in Texas …

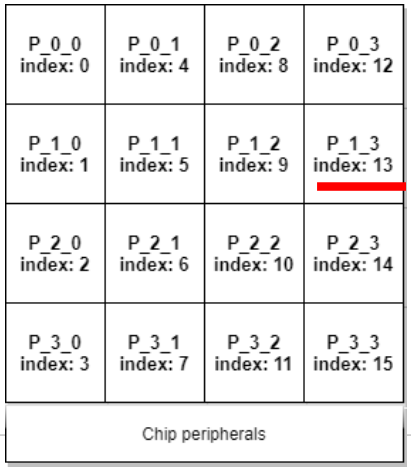
Now much of the testing is done remotely from home …

Example shown for Pixel 13

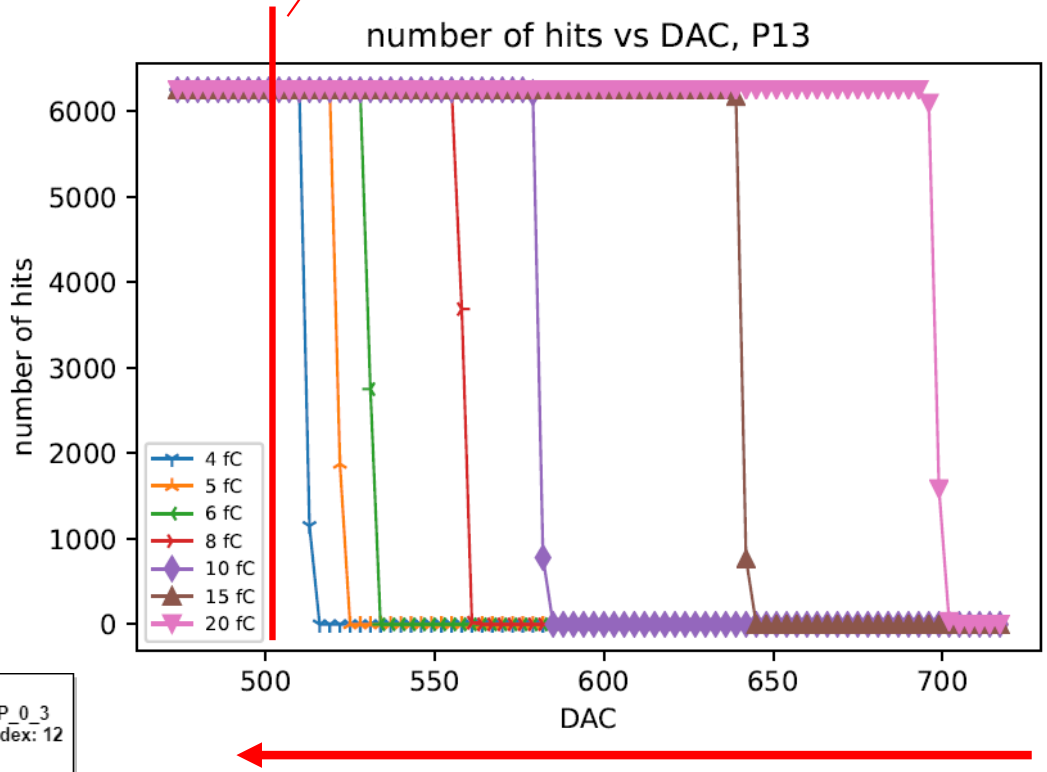
S-curve measurement

- Procedure for S-curve measurement
  - Injected various charge: 4fC, 5 fC, 6 fC, 8 fC, 10 fC, 15 fC, 20 fC
  - Scan threshold of the discriminator for each injected charge
  - Charge injection rate: 1.25MHz



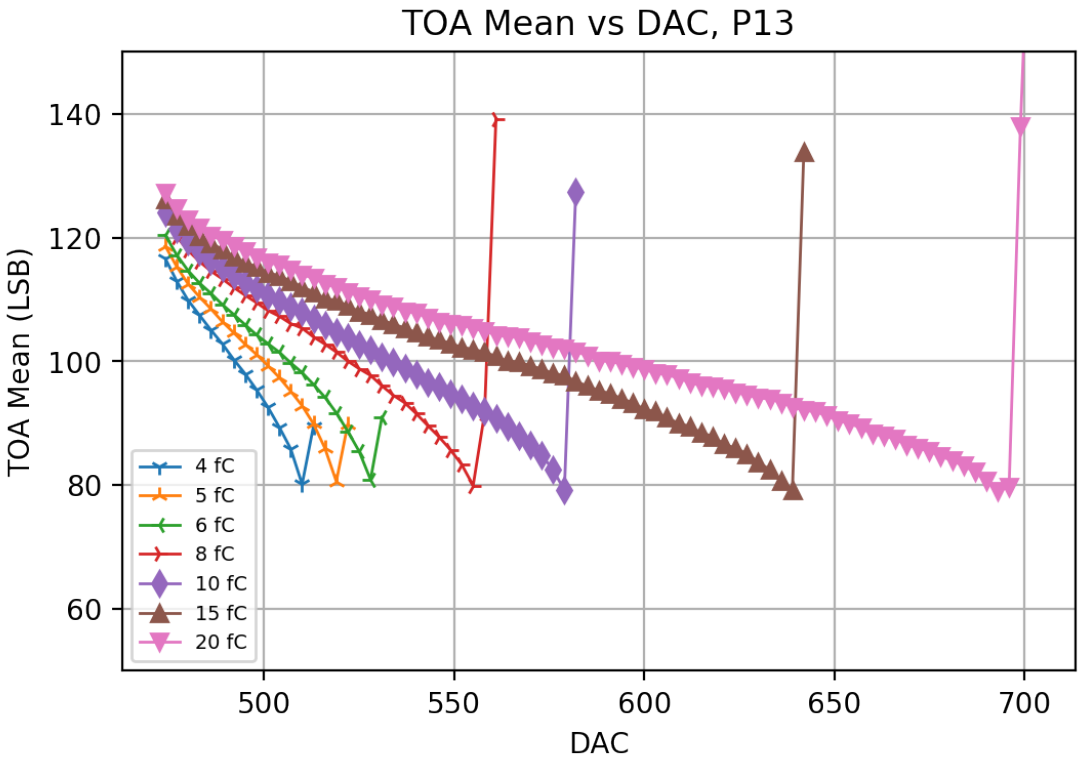


3 fC threshold for the results in rest of talk

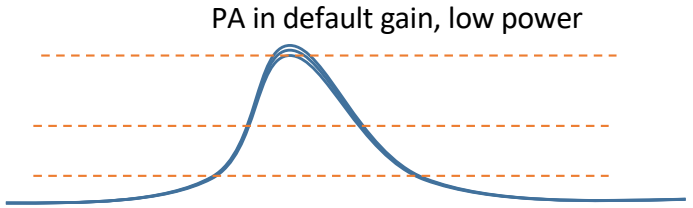


DAC scan

Time of Arrival (TOA) with charge injection



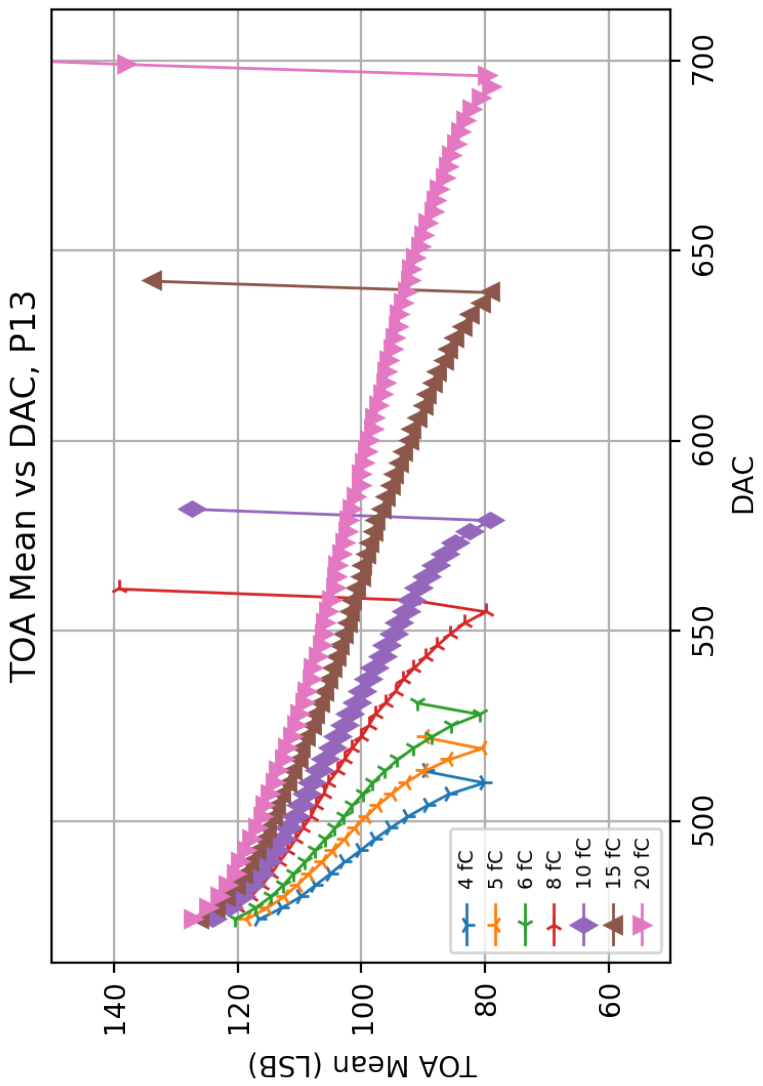
DAC scan



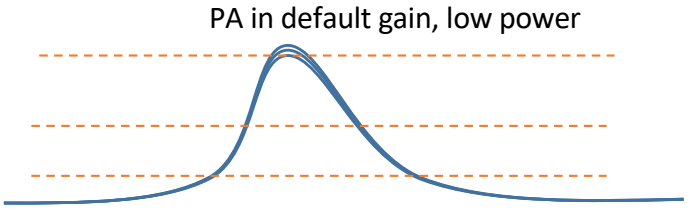
- The TOA vs the threshold look reasonable.
  - The higher the threshold, the late the discriminator fires(smaller TOA Code)
- With one feature observed:
  - When the threshold is approaching the peak, the TOA/TOT/Cal are not well determined, which is not unexpected
  - Some of the discriminator pulses didn't reach to 'high' level due to the small inputs
  - Usually accompanied by wrong Cal value
- In real operation, this would only happen to very small signal

TOA

View it differently …



DAC scan



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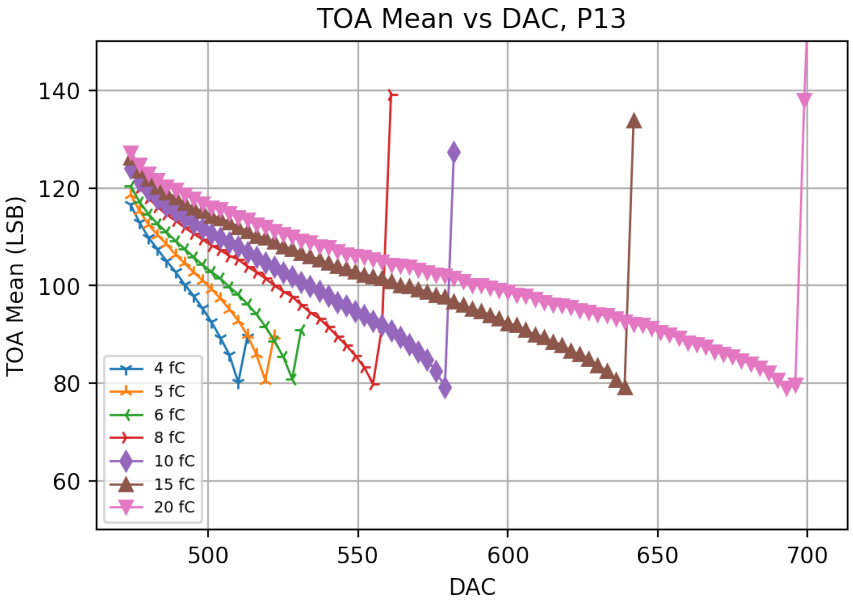
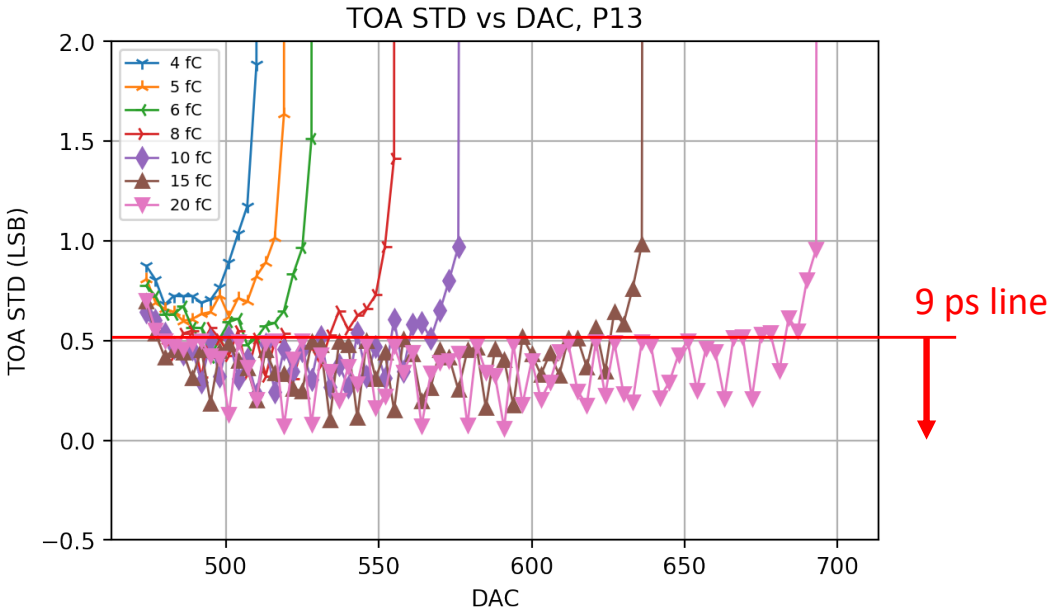
ETROC1 TOA mean and std, with charge injection





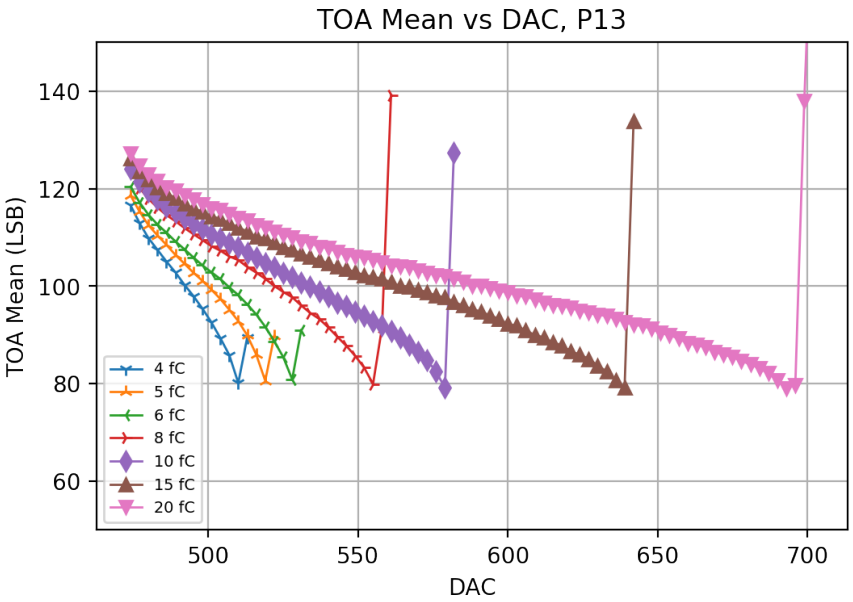
- 1 LSB = 18 ps
- PA in default gain, low power

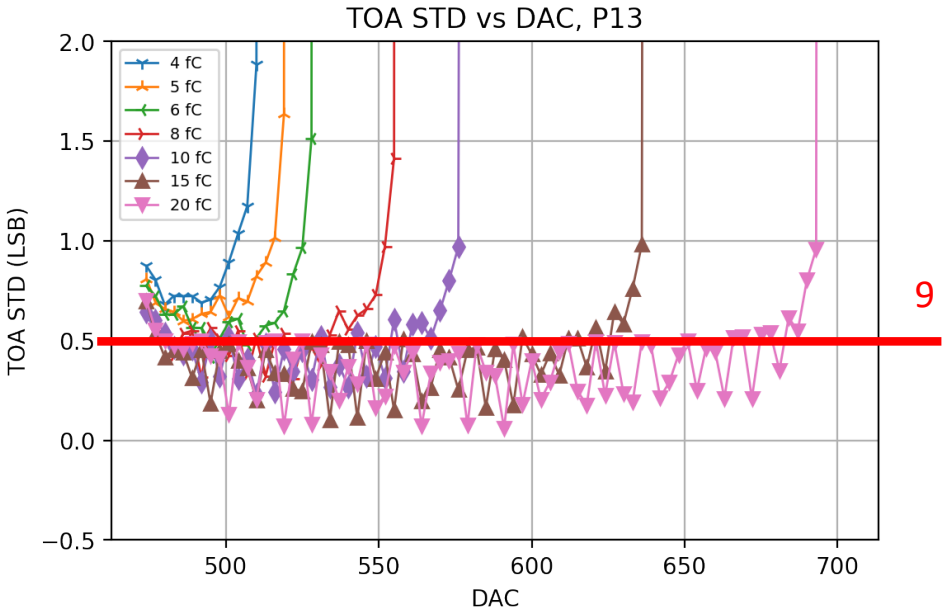
Performance as expected

TOA mean and std

Bare ETRCO1, pixel 13

- 1 LSB = 18 ps
- PA in default gain, low power

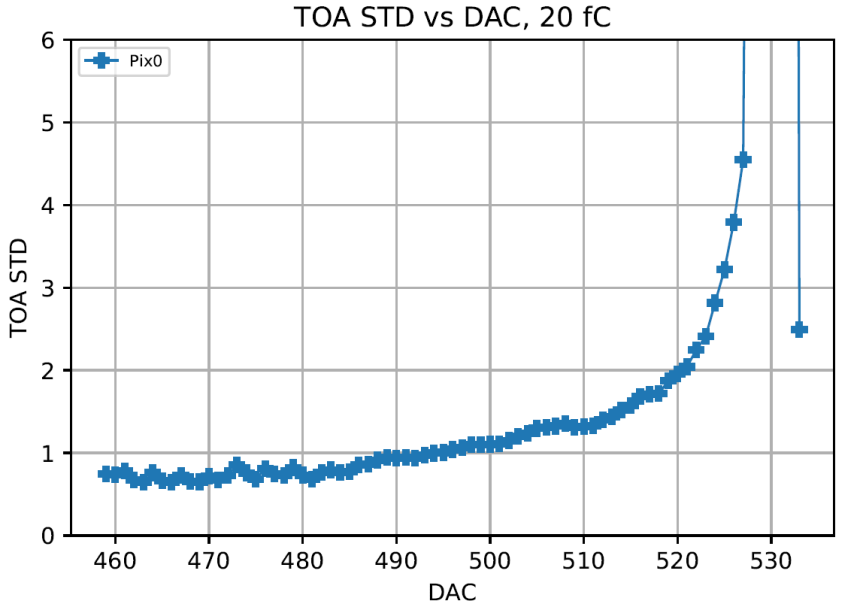




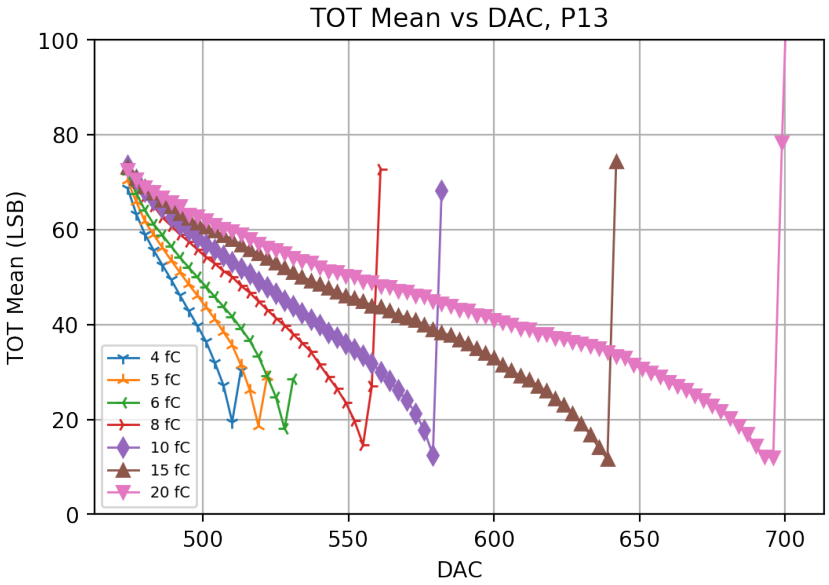
9 ps line

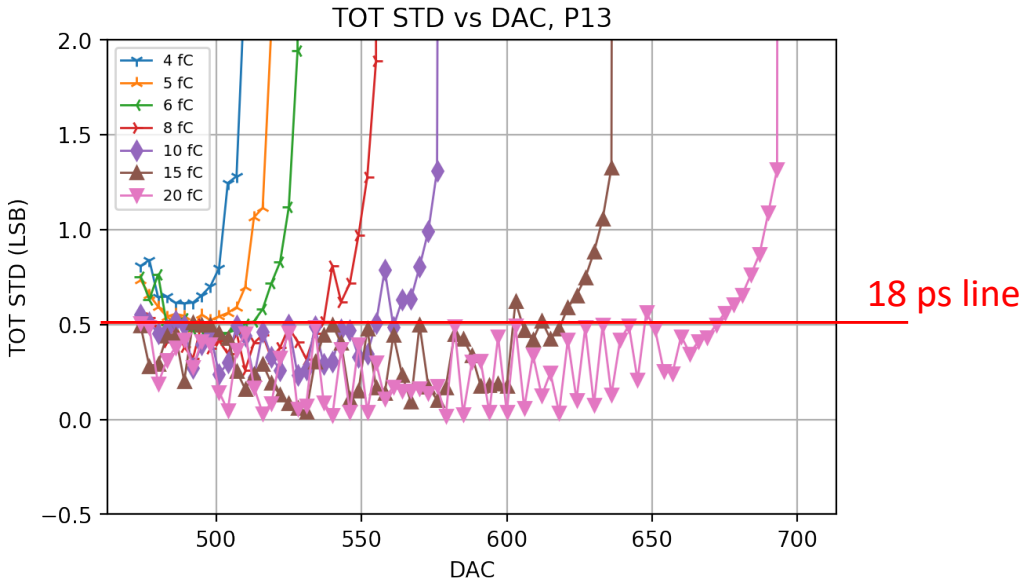
With sensor bump-bonded
On a different board/chip
(pixel 0)
Now with sensor
capacitance loaded

18ps line



ETROC1 TOT mean and std with charge injection

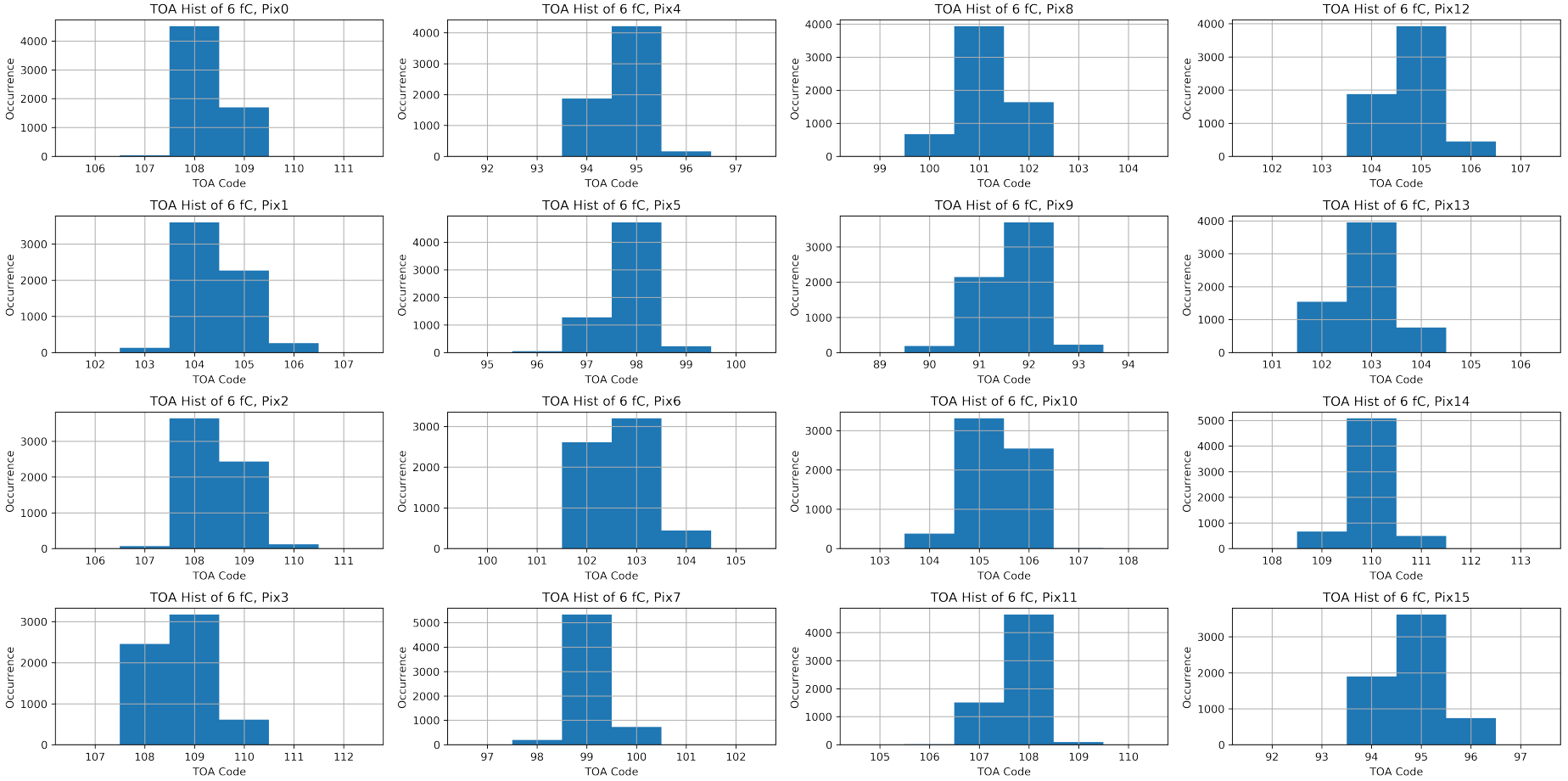




- 1 LSB = 18 * 2 ps
- Preamp in default gain, low power

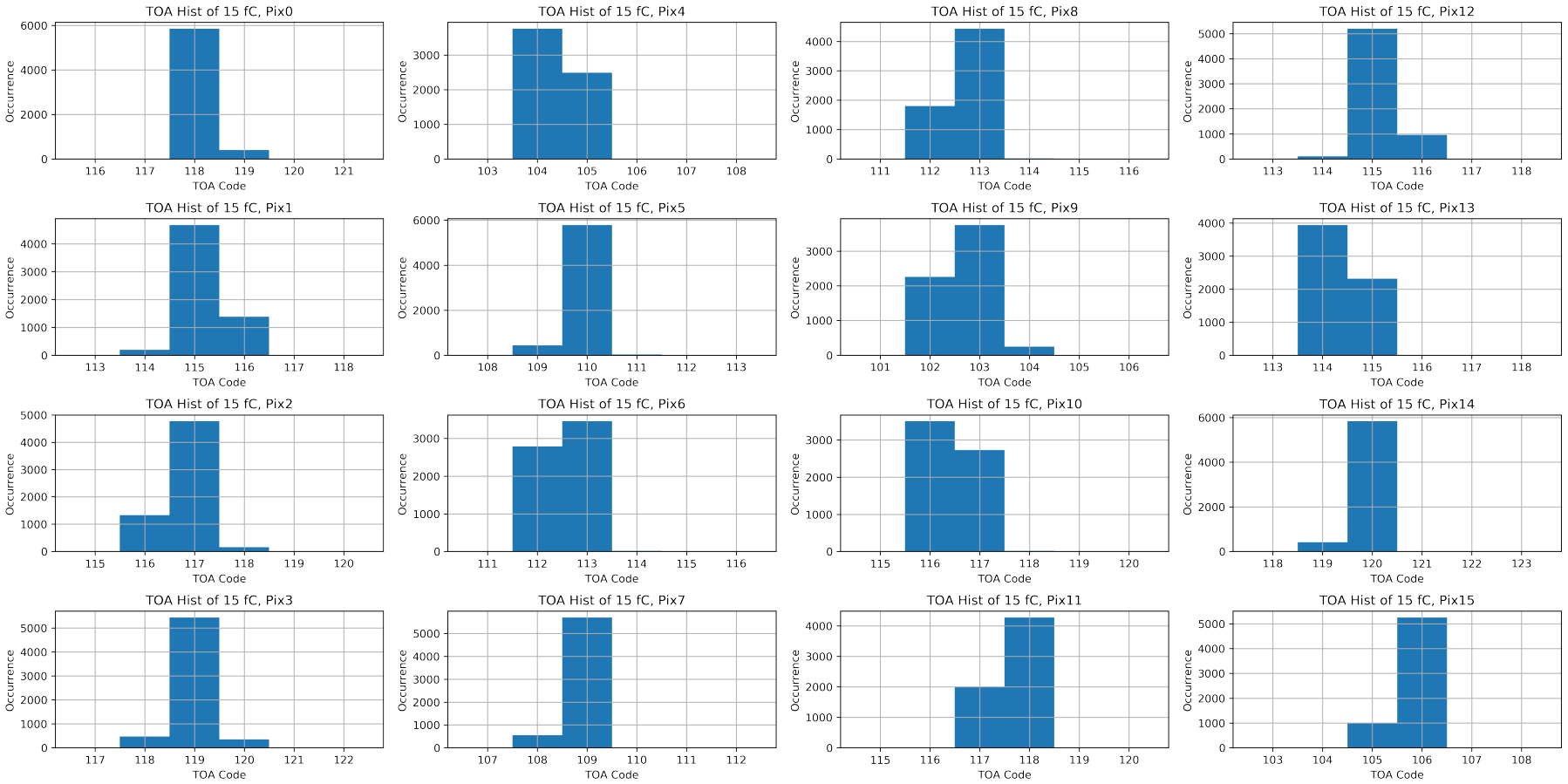
Performance as expected

ETROC1 TOA histogram of the array at 6 fC



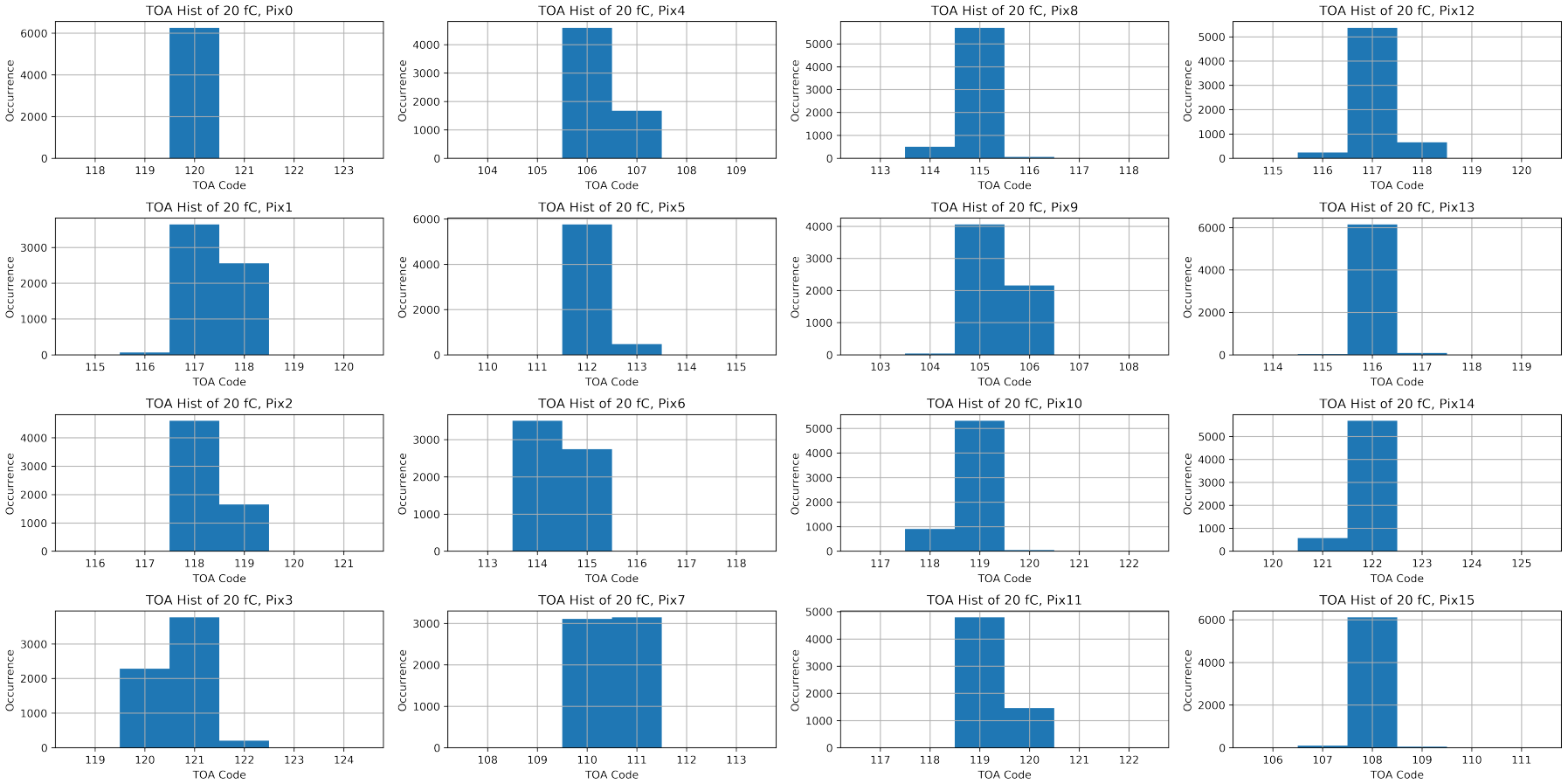
Performance as expected

ETROC1 TOA histogram of the array at 15 fC



Performance as expected

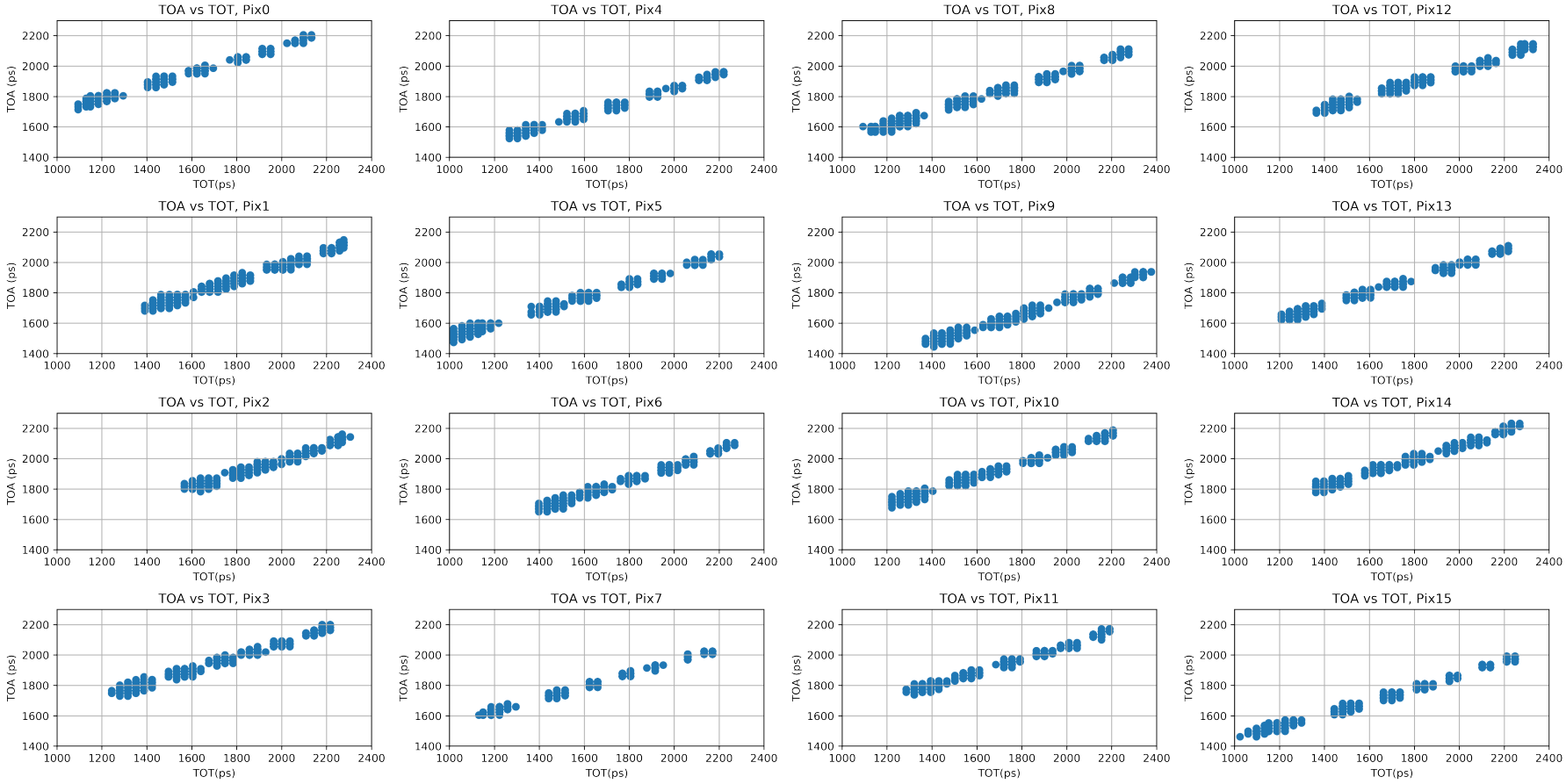
ETROC1 TOA histogram of the array at 20 fC



Performance as expected

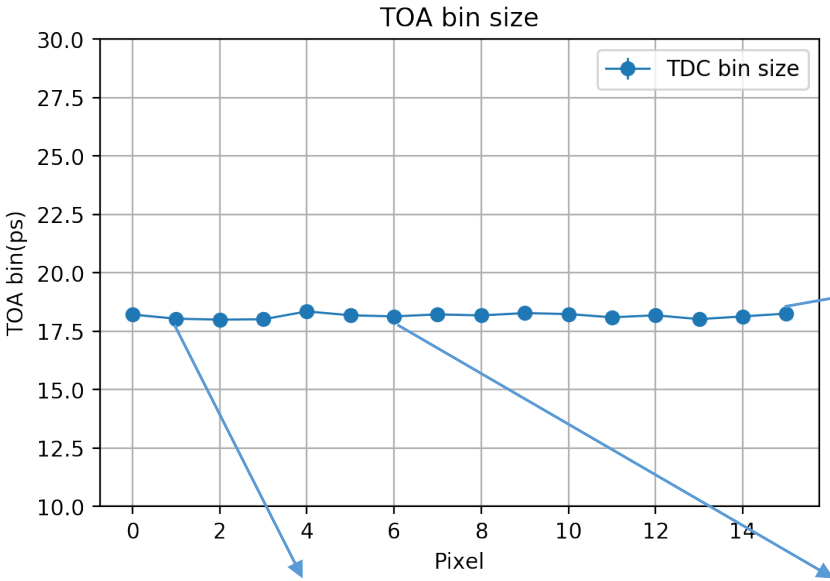
The timing is so good that it often falls within one TDC bin

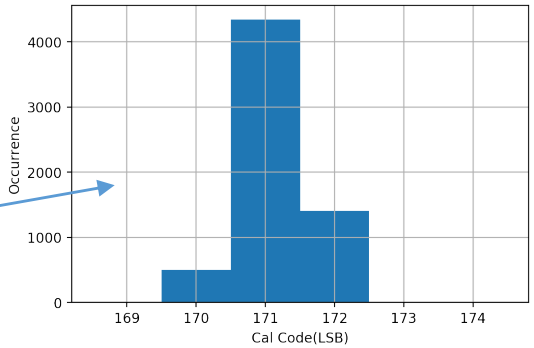
ETROC1: TOA vs TOT of the array

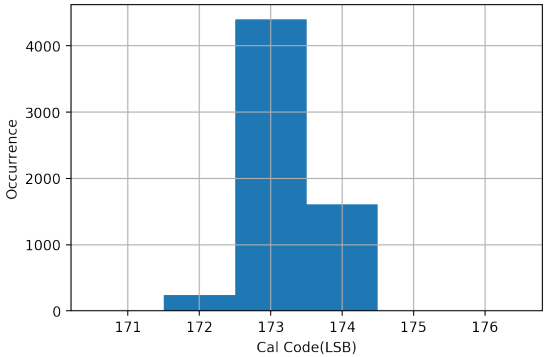


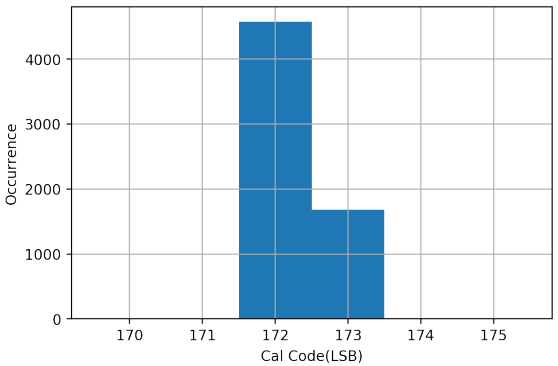
Performance as expected

Measured TOA bin size based on self-calibration (online)







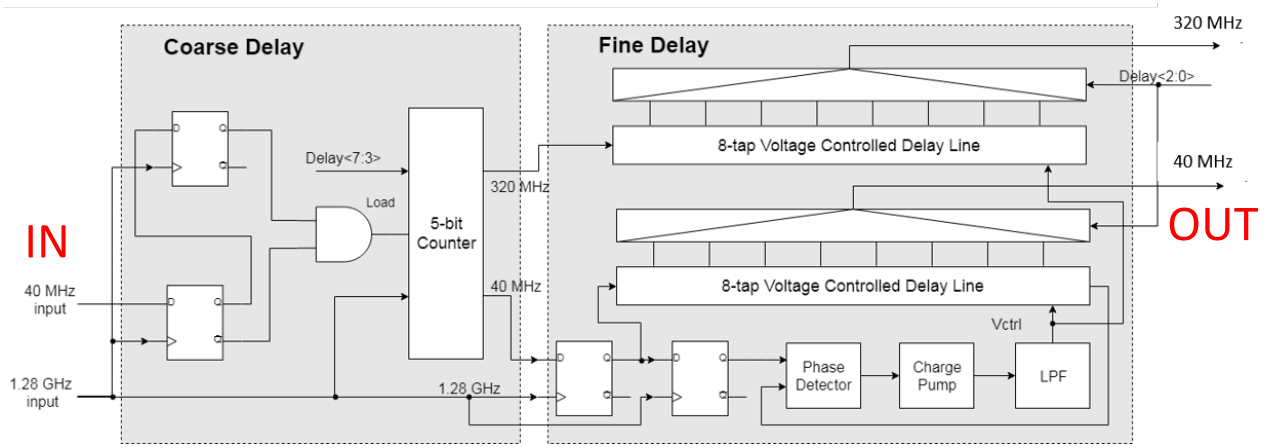


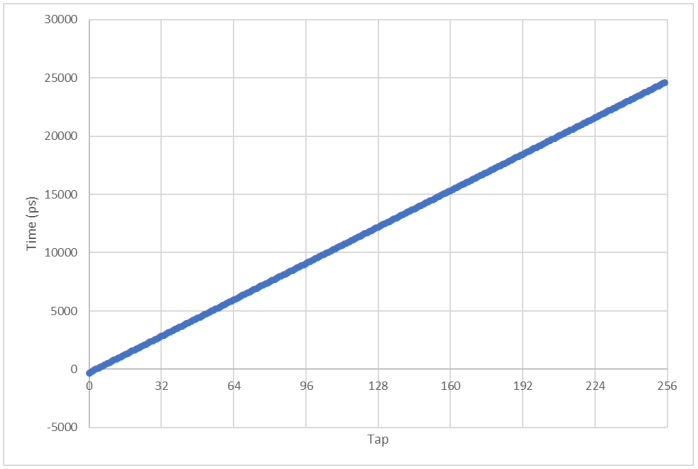
- ~18 ps bin size from the calibration code
- Good uniformity among pixels

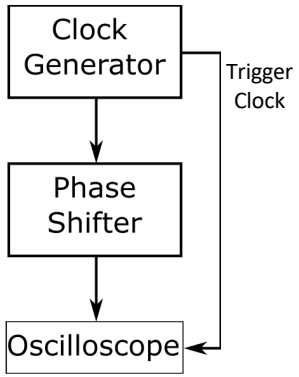
Performance as expected

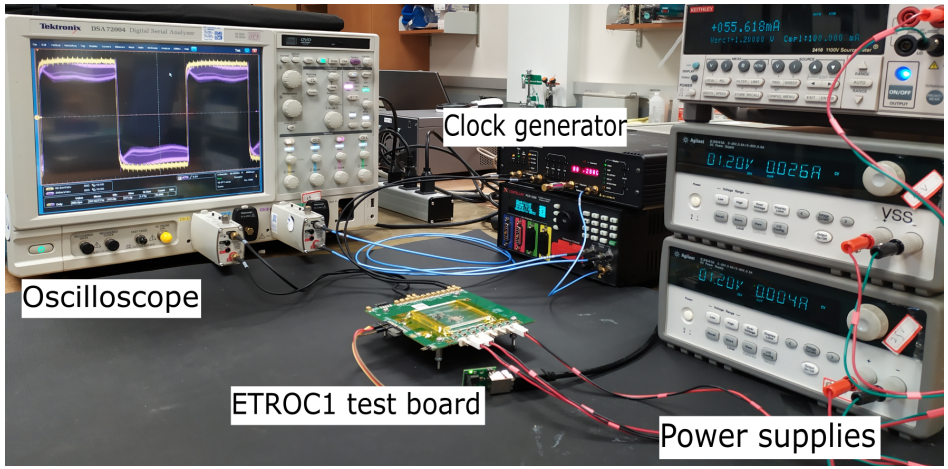
P_0_0 index: 0	P_0_1 index: 4	P_0_2 index: 8	P_0_3 index: 12
P_1_0 index: 1	P_1_1 index: 5	P_1_2 index: 9	P_1_3 index: 13
P_2_0 index: 2	P_2_1 index: 6	P_2_2 index: 10	P_2_3 index: 14
P_3_0 index: 3	P_3_1 index: 7	P_3_2 index: 11	P_3_3 index: 15
Chip peripherals			

Testing ETROC1 phase shifter









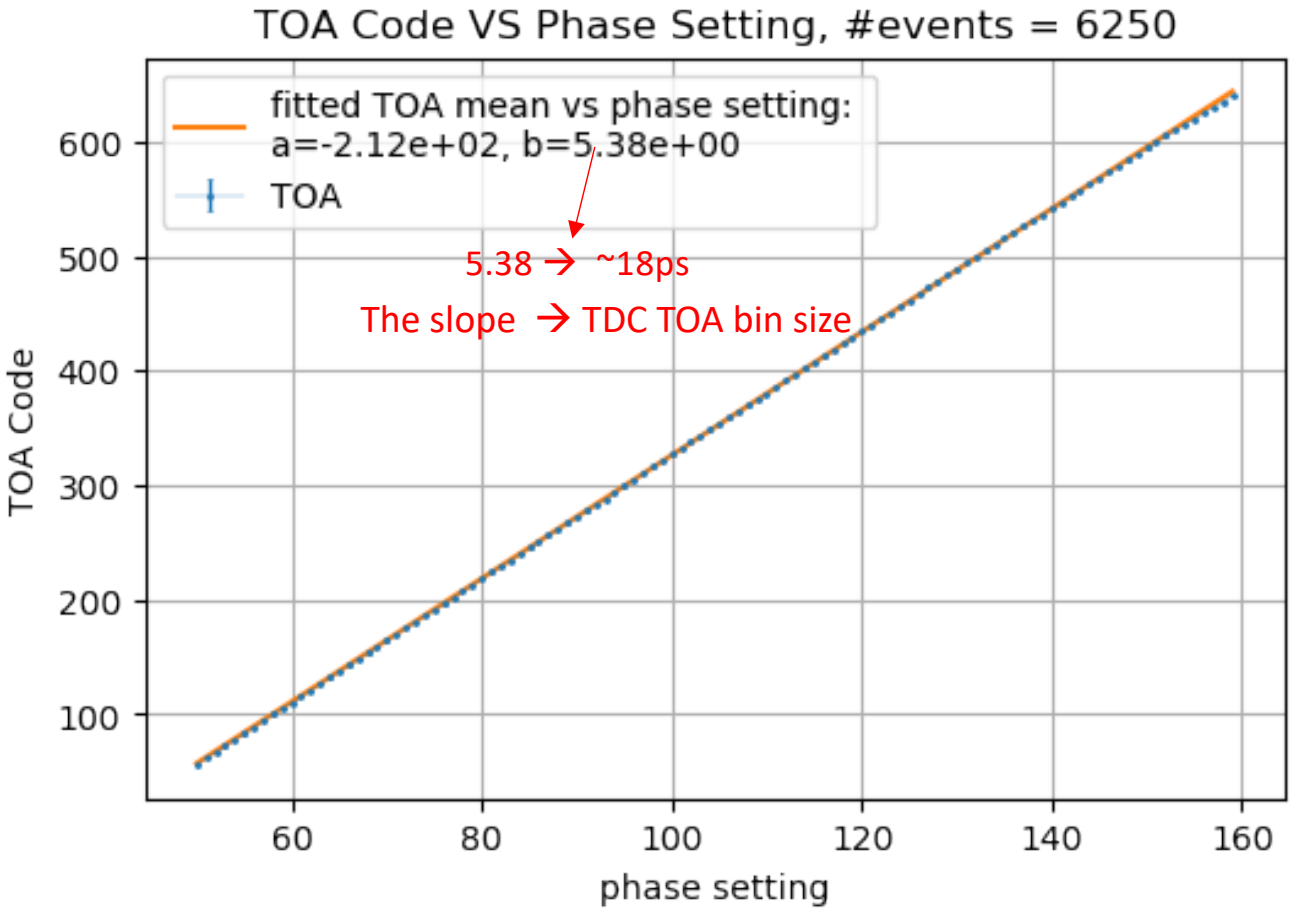
Preliminary test results of
the phase shifter look good

Phase shifter step: 98ps

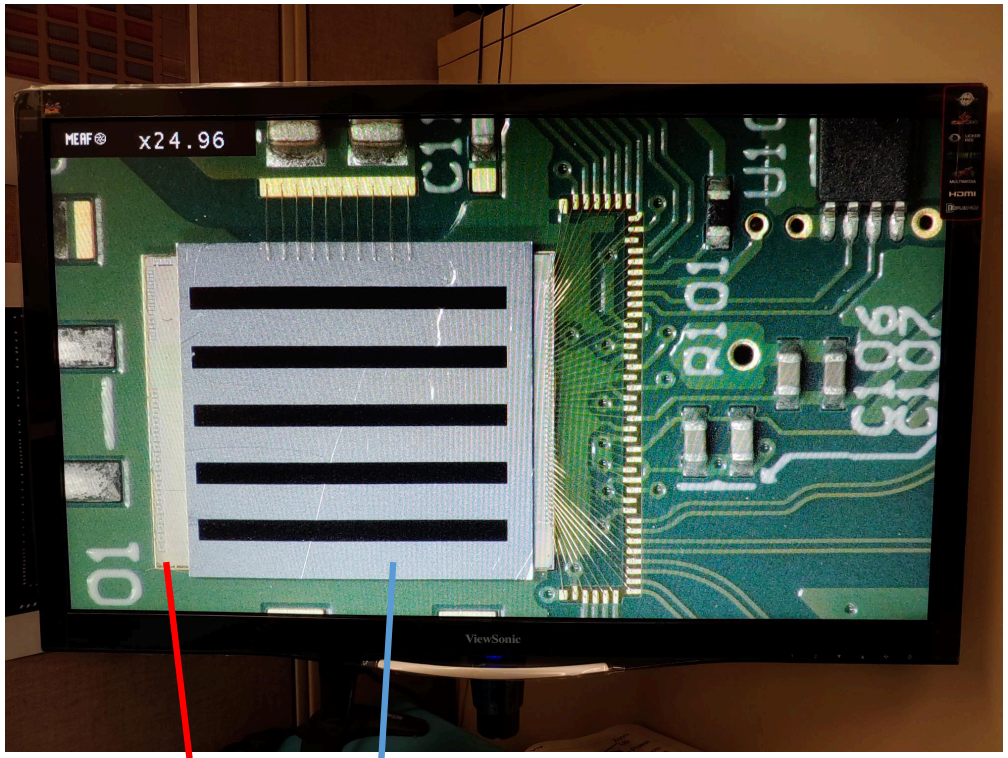
Use phase shifter to perform full chain Phase scan (like in real operation)

A different way to measure TDC bin size (online)

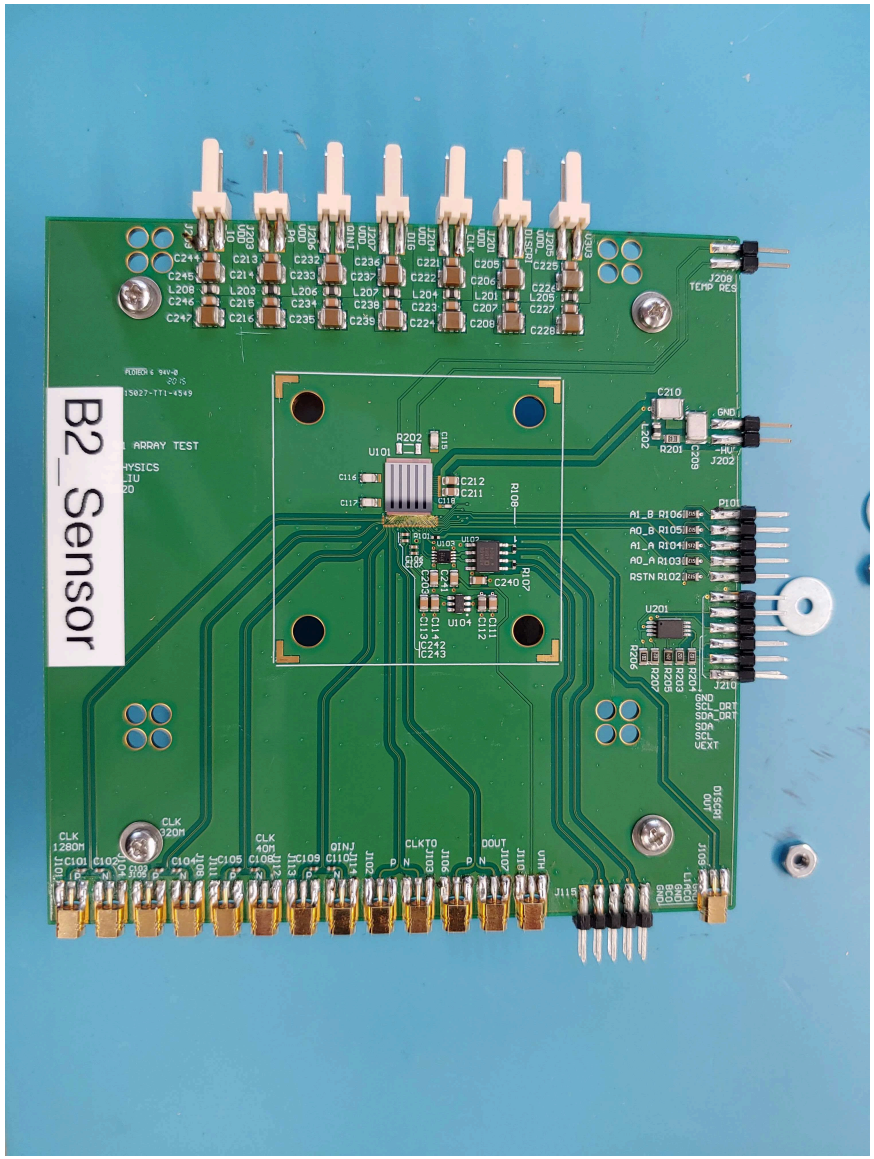
6 fC charge injection
1.25MHz rate
Pixel 15
Threshold ~ 3 fC



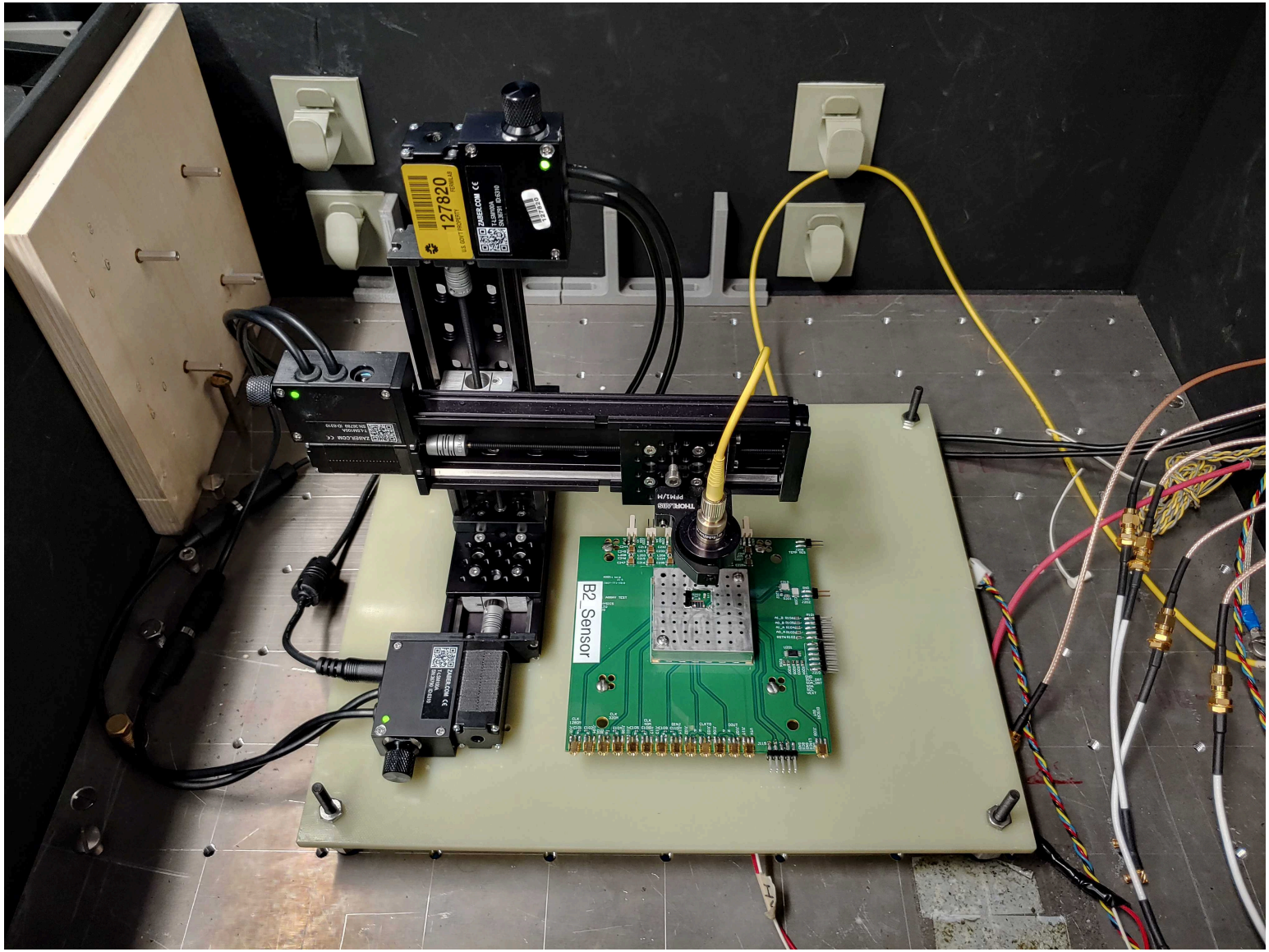
With bump bonded sensor/ETROC1



ETROC1
bump bonded
to 5x5 LGAD

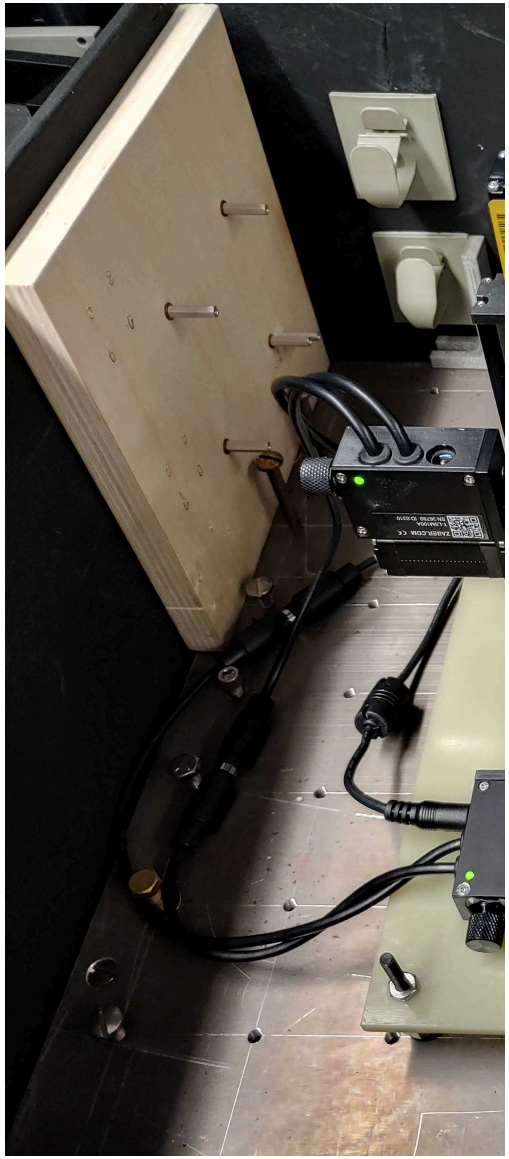


Laser testing setup at FNAL (14th floor)



Laser testing setup at FNAL (14th floor)

Very first ETROC1 laser response from Chris Edwards
Last Friday (discriminator output)



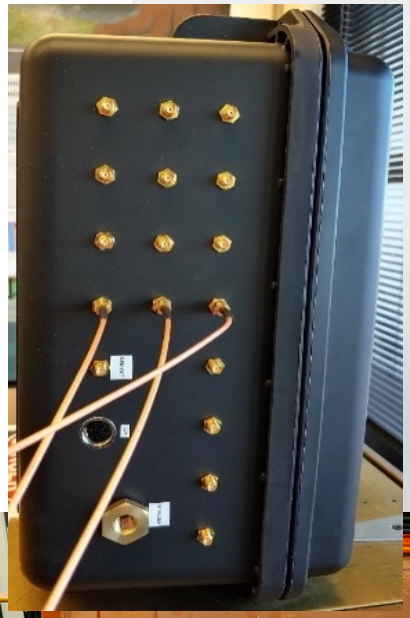
Jitter Performance

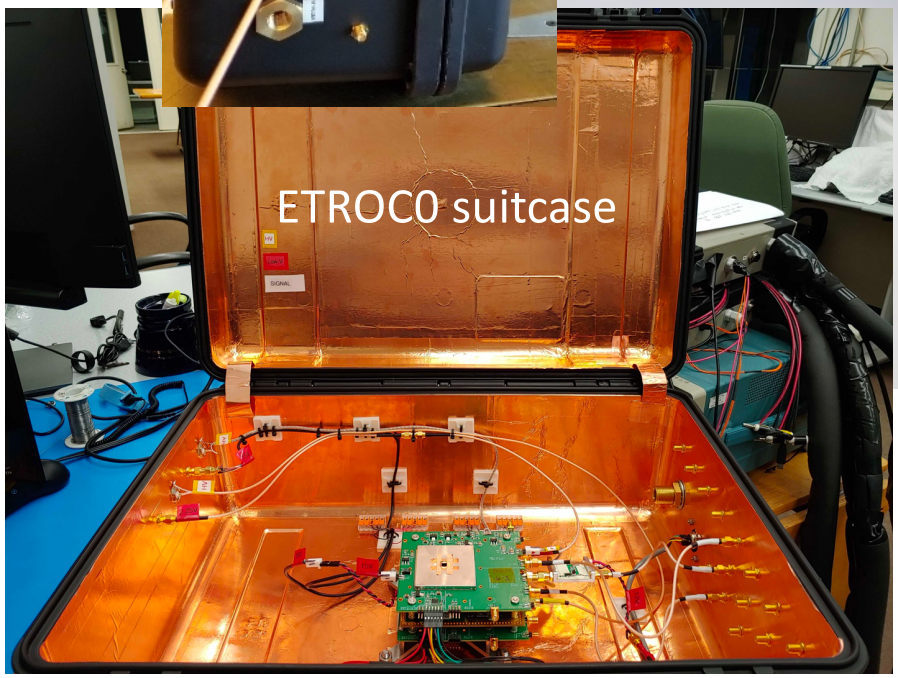
Saw values of 14ps-25ps depending on location of trigger and spot where jitter is measured. Will investigate this more in further testing.

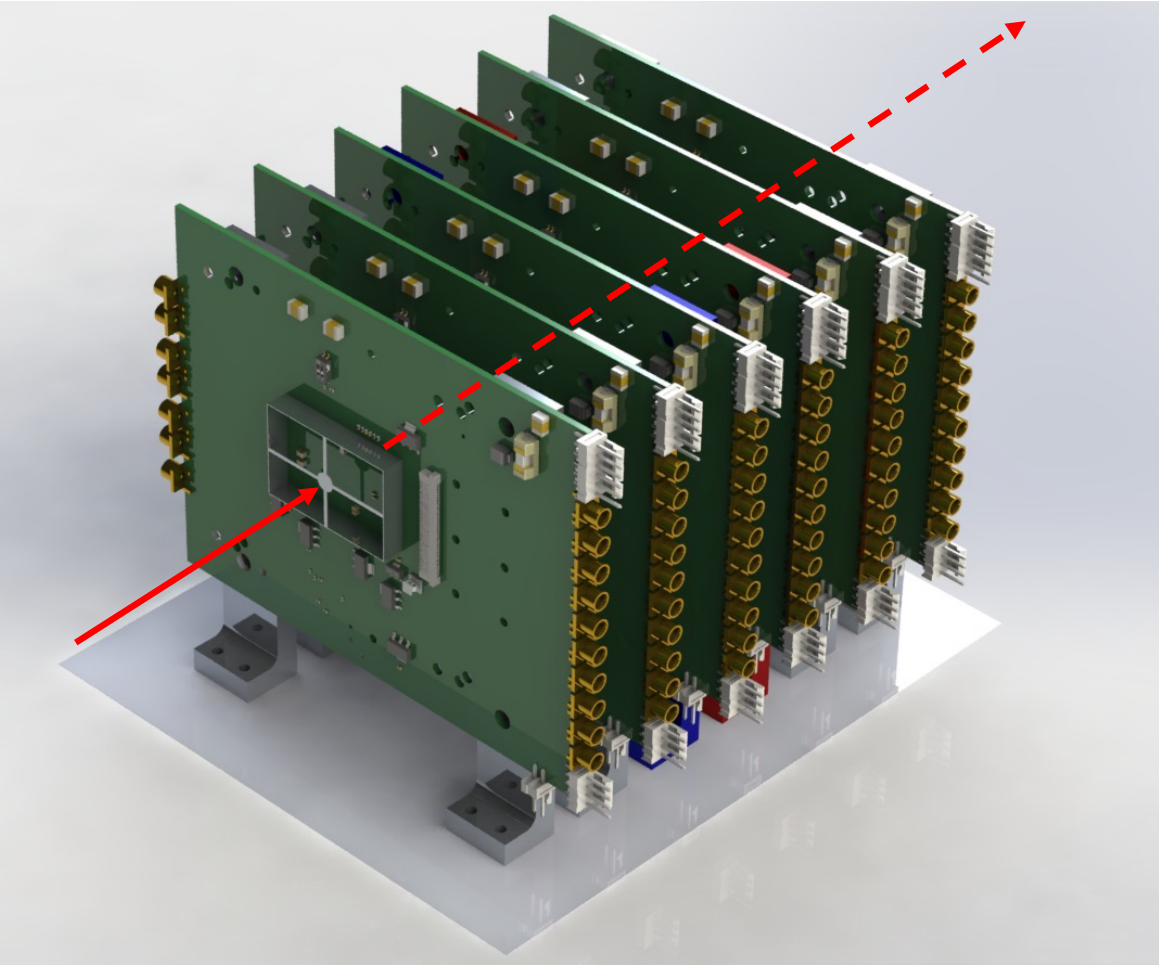
Next Steps

Going to test full chain readout with TDC data being output to the KC705 FPGA development board. This has previously been demonstrated so I'm very optimistic about this next phase of testing.

ETROC1 Beam Telescope design



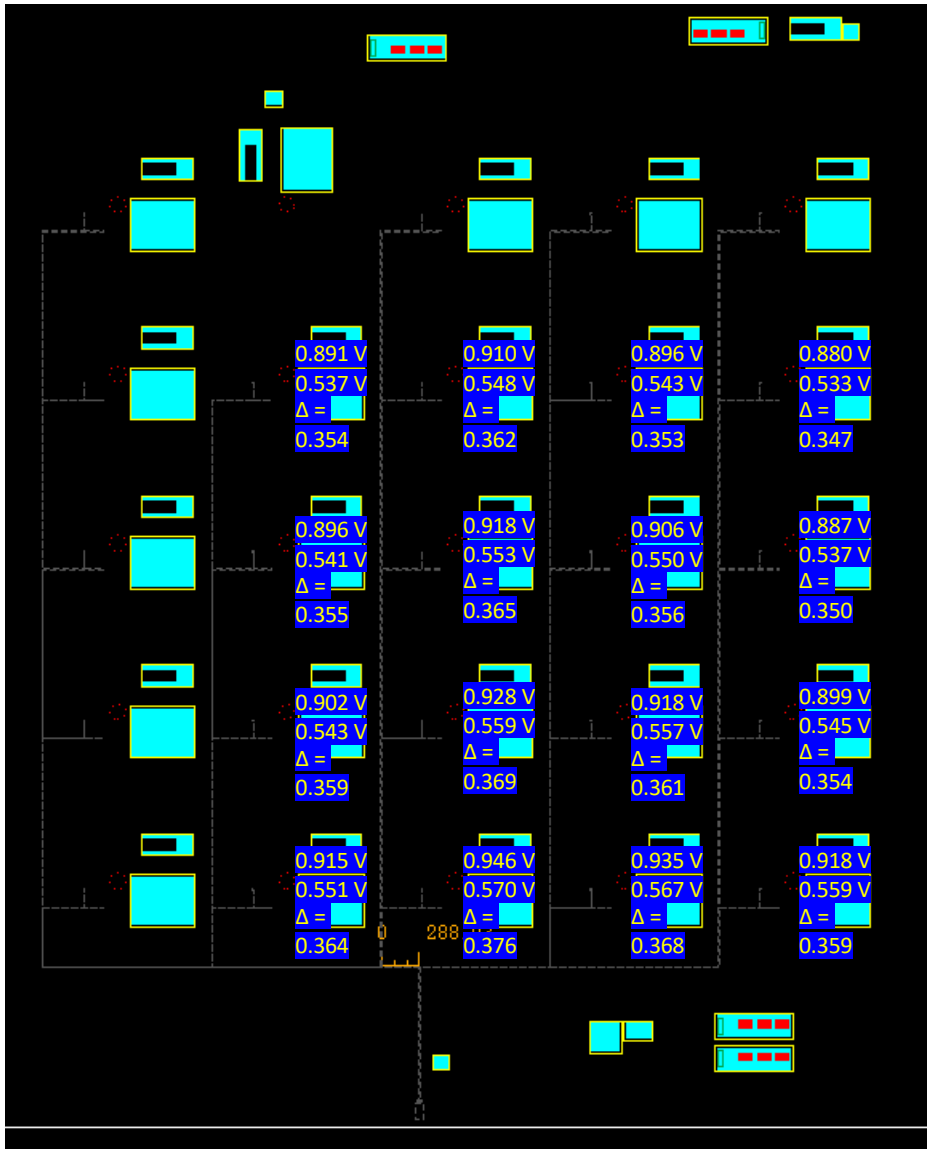




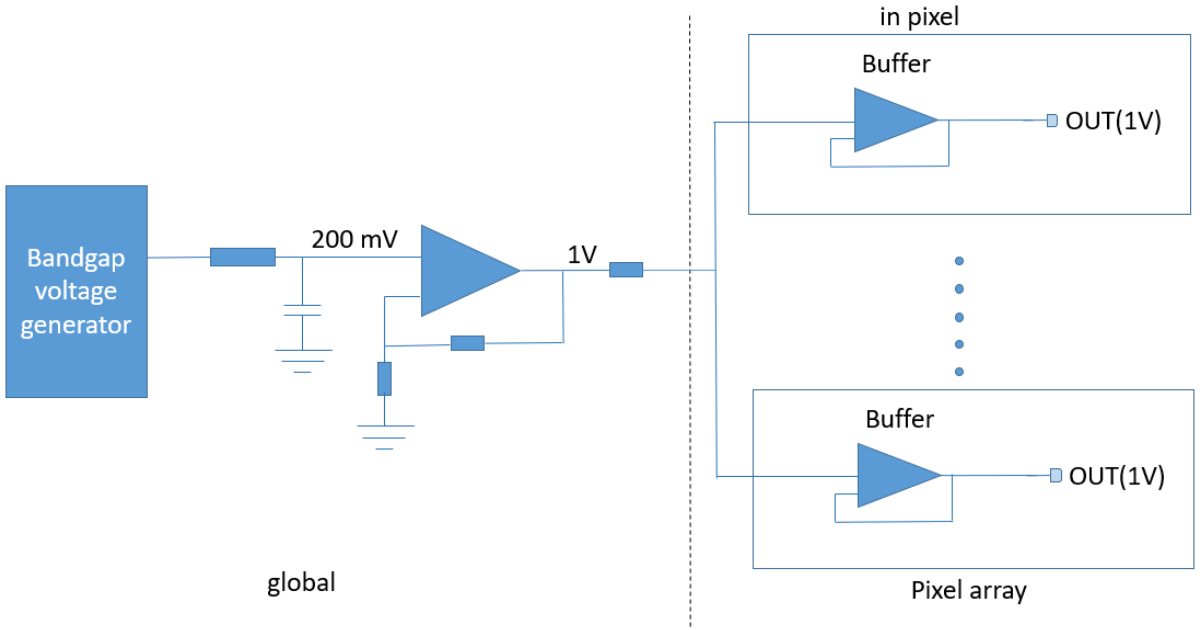
Designed by Chris Edwards (FNAL)

IR drop on VREF for ETROC1

- Pixel-dependent IR drop was observed on the voltage reference (VREF)
- The IR drop is observed because that the trace resistance is not negligible when the circuits draw current from VREF
- The IR drop does not affect ETROC1 testing much because DAC output still convers the range that is required
- This issue has been identified soon after the ETROC1 submission during ETROC2 full size floor planning and power distribution study.
- An improved design for VREF distribution has been prototyped in the PLL chip.

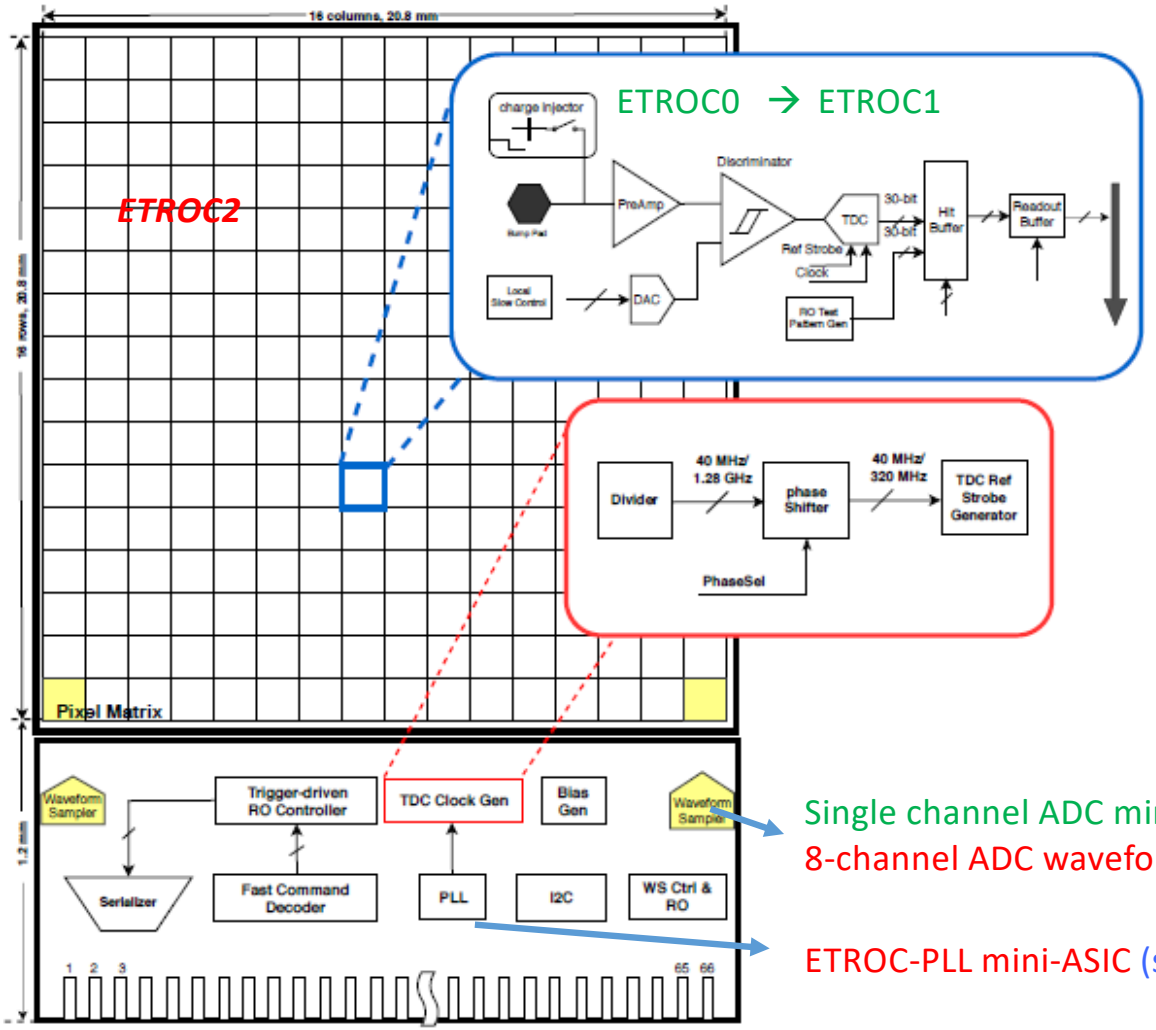


Reference voltage generator for ETROC2



- VREF generator is used to provide 1V reference voltage to the charge injection and the DAC in each pixel.
- A global bandgap voltage generator(from lpGBT) generates 200mV voltage.
- The RC filters are used to reduce noise and the Amplifiers generate 1 V voltage from bandgap.
- Buffer in each pixel provide stable 1V voltage
- This design block has been implemented in the PLL test chip, and we are ready to test it

From ETROC0 → ETROC1 → ETROC2



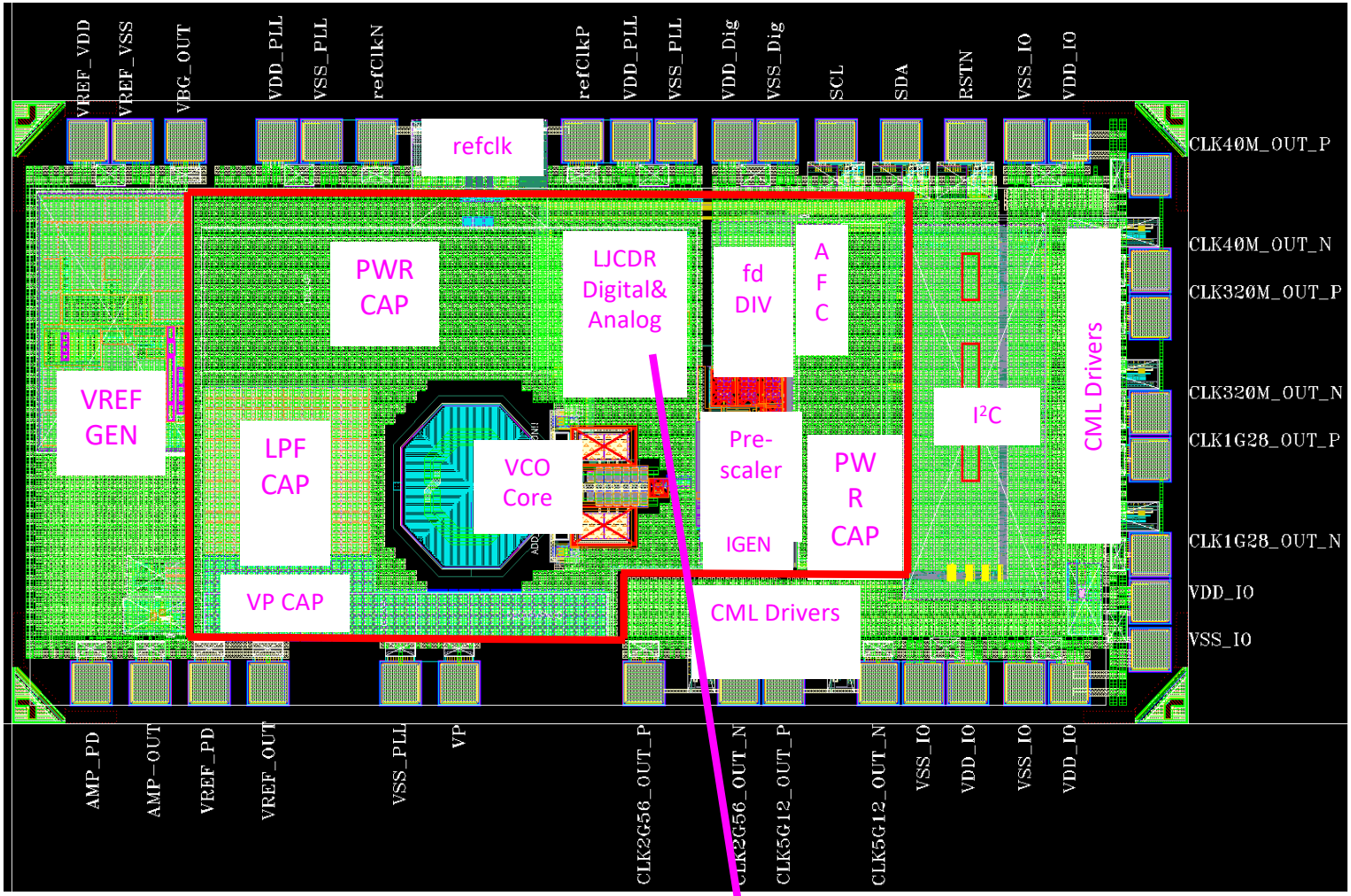
Single channel ADC mini-ASIC (submitted May 2019)
8-channel ADC waveform sampler (submitted March 2020)

ETROC-PLL mini-ASIC (submitted May 2020)

Fast command decoding, slow control (I2C), pixel readout, digital I/O, all being prototyped in ETROC emulator (FPGA)

(no time to cover the details)

The PLL mini-ASIC chip



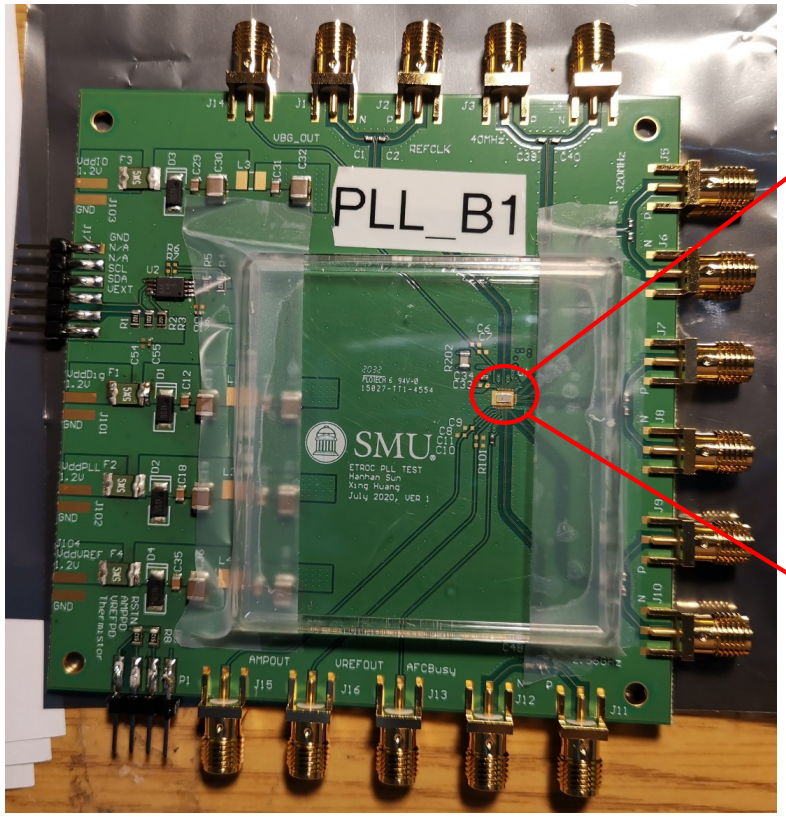
- Size of the chip: 2000 µm x 1000 µm
- Size of the ETROC PLL core : ~ 1170 µm x 685 µm

lpGBT's
Low-jitter Clock and Data Recovery (LJCDR)

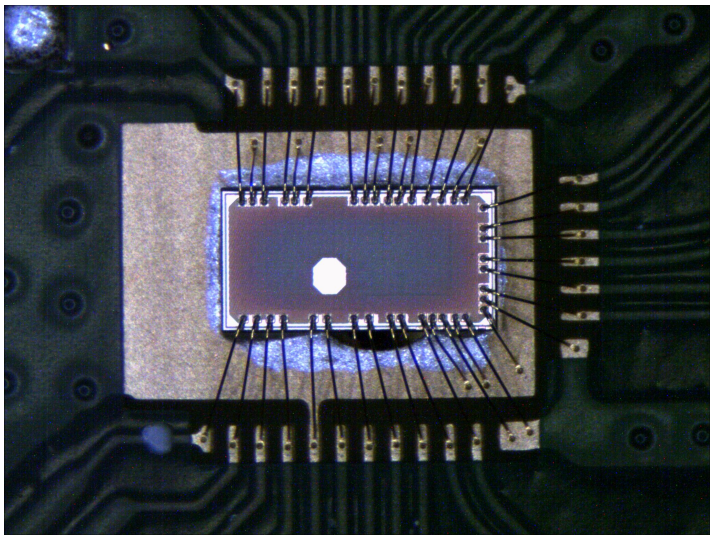
Extensively simulated. Reviewed by lpGBT experts.
Submitted on May 20th, 2020

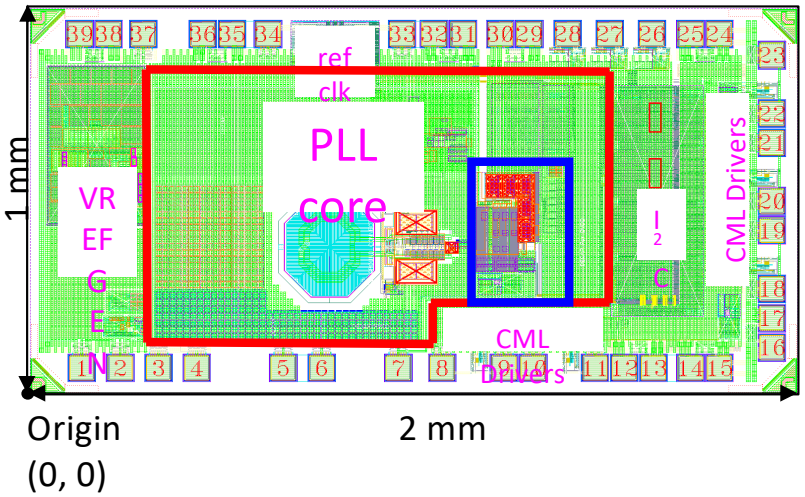
PLL core Power: 60mW
(to be verified with mini-ASIC)

ETROC PLL Testing preparation



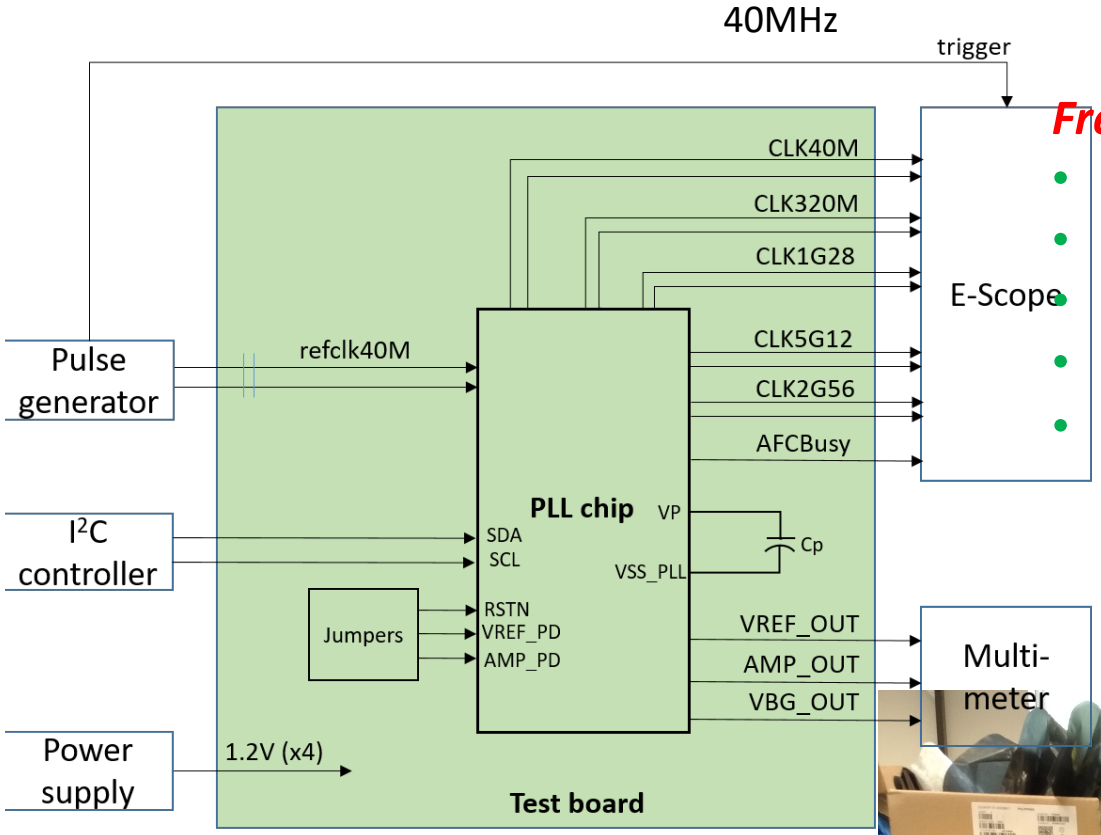
PLL mini-ASIC





- PLL chip submitted during COVID lockdown (May), arrived early Sept
- ***The PLL chip test started last Friday***
  - ***First day results very promising …***

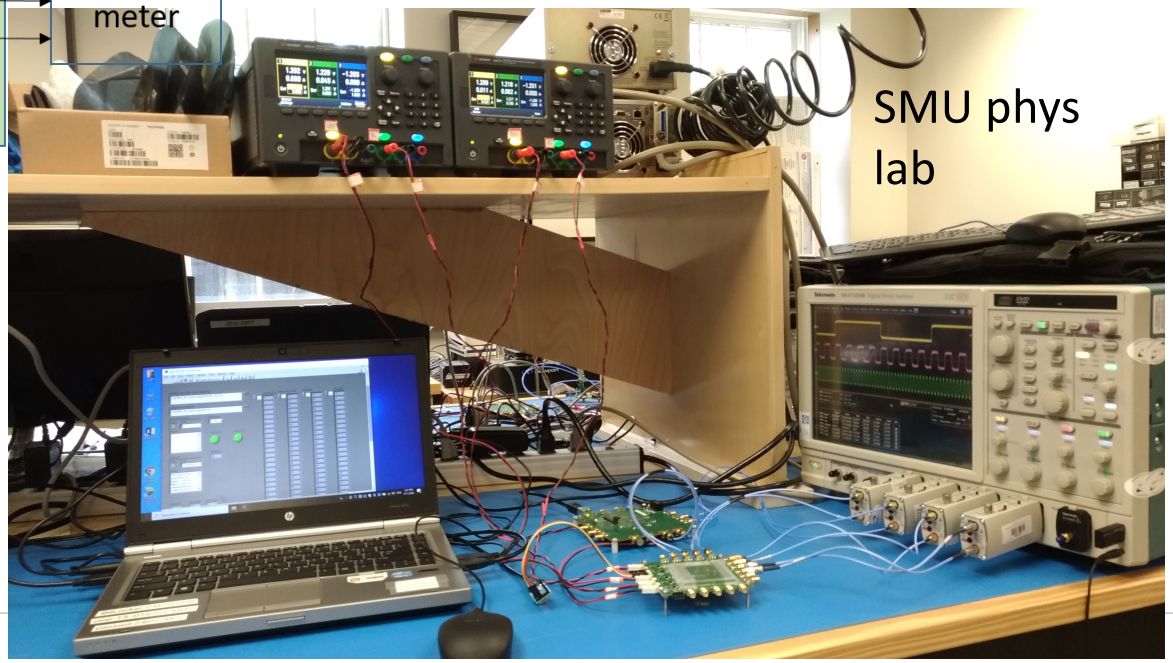
ETROC PLL Test results on day one :



Fresh results from the first day:

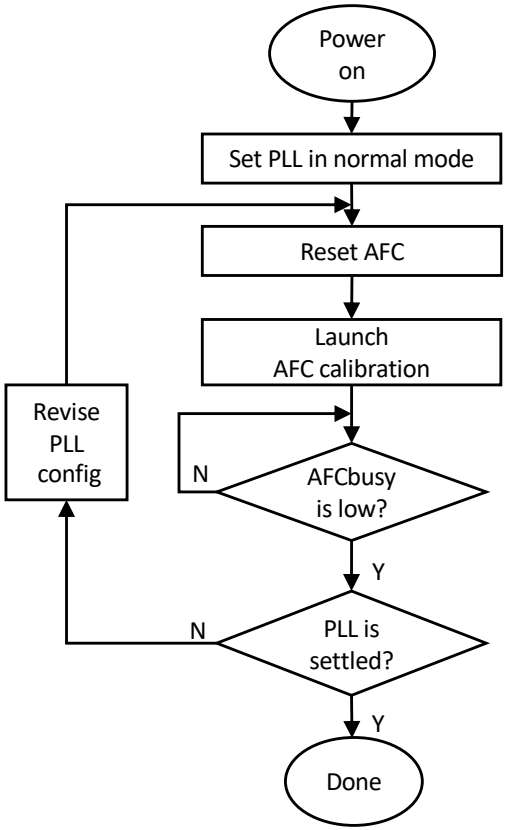
- Automatic frequency calibration (AFC) works
- PLL locks at 5.12 GHz after AFC
- All clocks rms jitter ~ 2ps
- Power consumption as expected
- All four boards fully consistent

Very good for the very first try



Four boards prepared
Passed smoke test on Sept 10
First results on Sept 11th shown here

AFC calibration



- Test procedure:
  - Apply 40-MHz reference clock to the test board.
  - Keep the default settings for PLL core.
  - Follow the fully automatic calibration flow (see left), launch the binary search for the optimal VCO capacitor DAC setting.
  - Check if the PLL is settled by:
    - Observing the output clocks on the oscilloscope.
    - Reading back the values of read-only register REGIn_20.

- **Test results:**
  - **PLL loop locks at 5.12 GHz.**
  - **The values of REGIn_20 are within expectation and shown below:**

REGIn_20	BIT							
	7	6	5	4	3	2	1	0
	INSTLOCK_PLL	AFCcalCap<5:0>						AFCBusy
Board1	1	0	1	0	1	0	0	0
Board2	1	0	1	0	1	0	0	0
Board3	1	0	1	0	1	0	0	0
Board4	1	0	1	0	1	0	0	0

The optimal VCO capacitor DAC setting of each test board is the same!

Four boards tested on day one, and all consistent

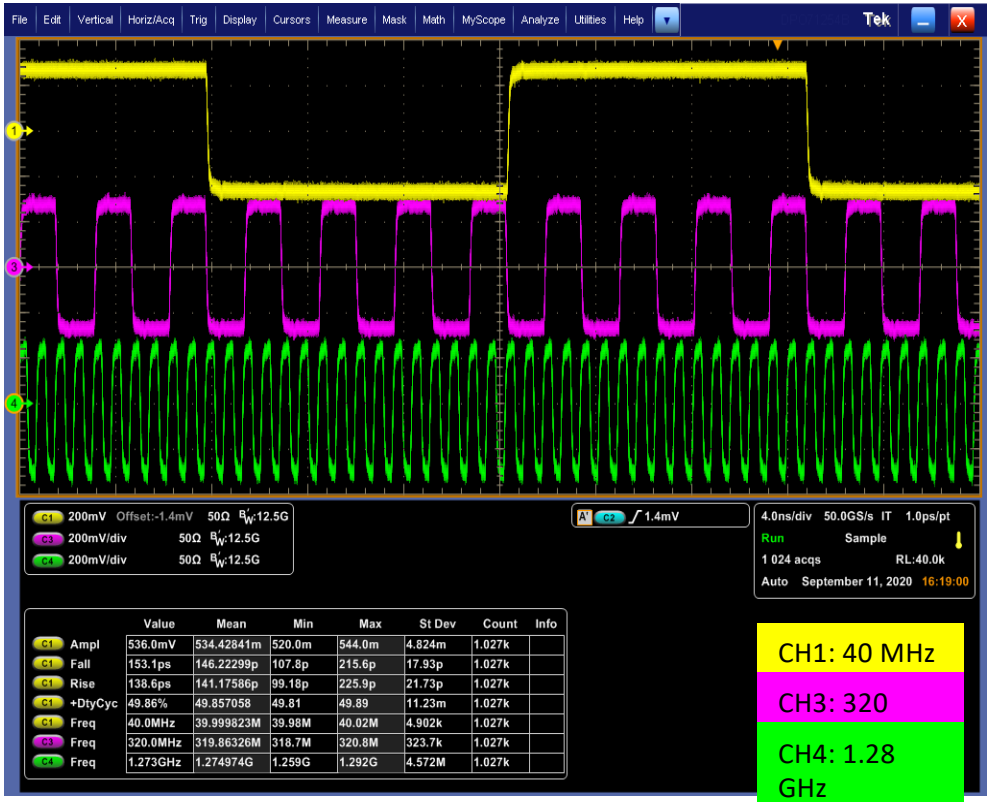
PLL power consumption

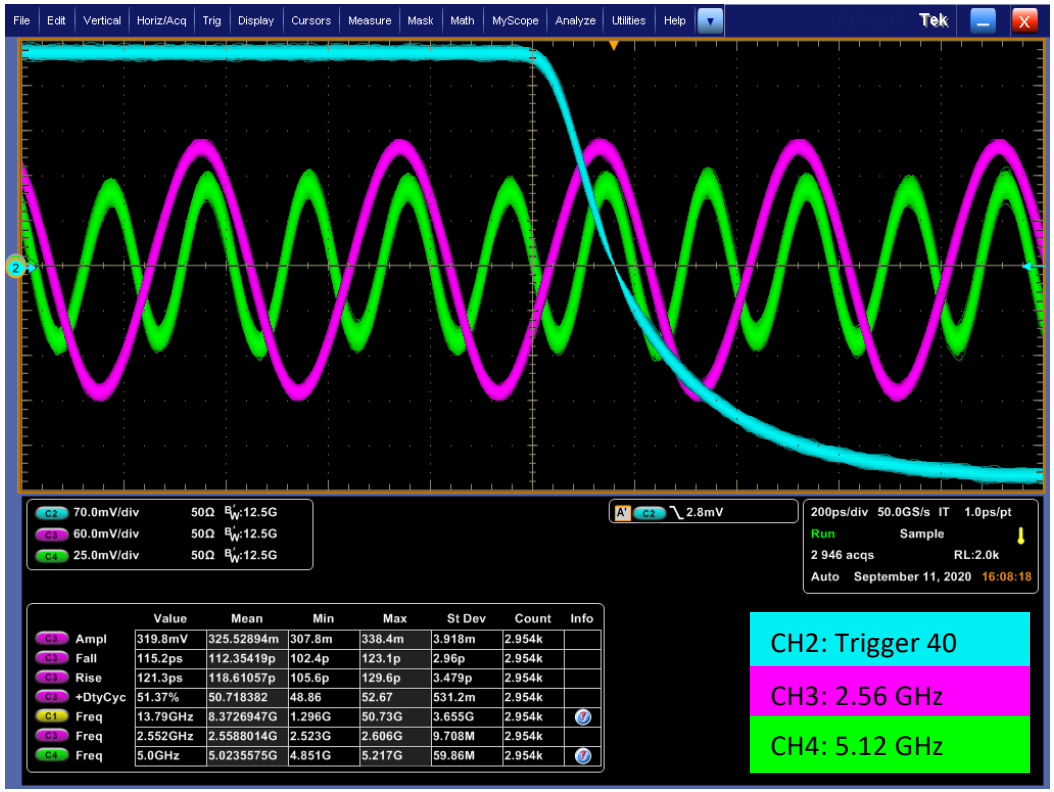
Operating current	Simulated values[1] (mW)	Test values when PLL locks at 5.12 GHz (mW)			
		B1	B2	B3	B4
Idd_IO[2]	78.0	74.4	73.2	73.2	74.4
Idd_Dig	10.4[3]	13.2	13.2	12.0	12.0
Idd_PLL	50.6 (PLL core: 47.2) (eRx: 3.4)	51.6	51.6	51.6	51.6

[1] The nominal pre-schematic simulation of power consumption is with tt corner, 1.2 V power supplies and room temperature of 27°C.
[2] All the output clocks are enabled and with the maximum output amplitudes.
[3] The power consumptions of AFC and I^2C are estimated to be 2 mW.

The total power consumption of PLL core is about 60 mW, which agrees with the simulations.

clock waveforms

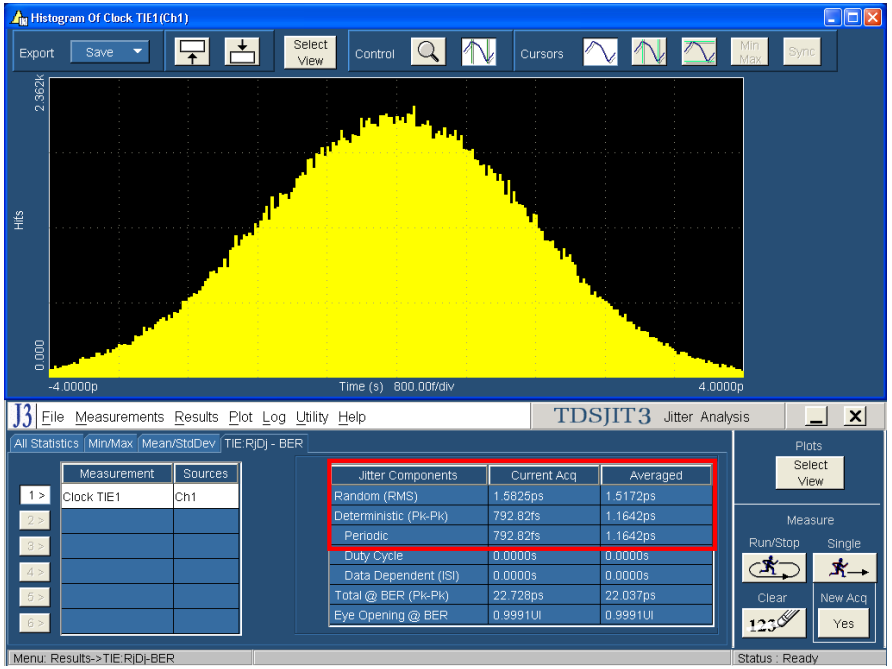




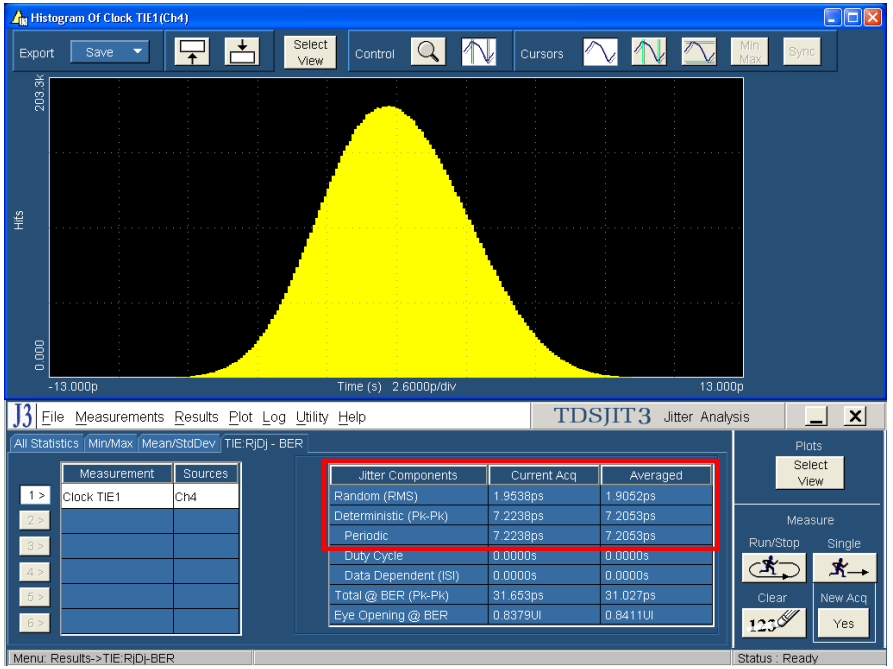
- All output clocks are captured with the trigger clock of 40 MHz from the clock builder.
- Note that the bandwidth of the CML drivers is not enough to drive the 2.56 GHz and 5.12 GHz output clock.

Jitter measurements (preliminary)

- 40 MHz



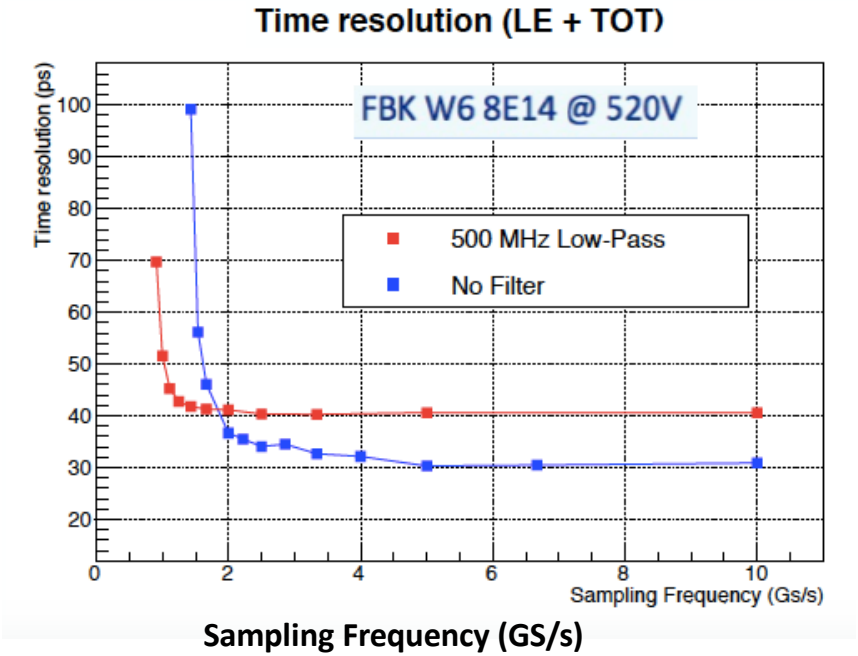
- 5.12 GHz

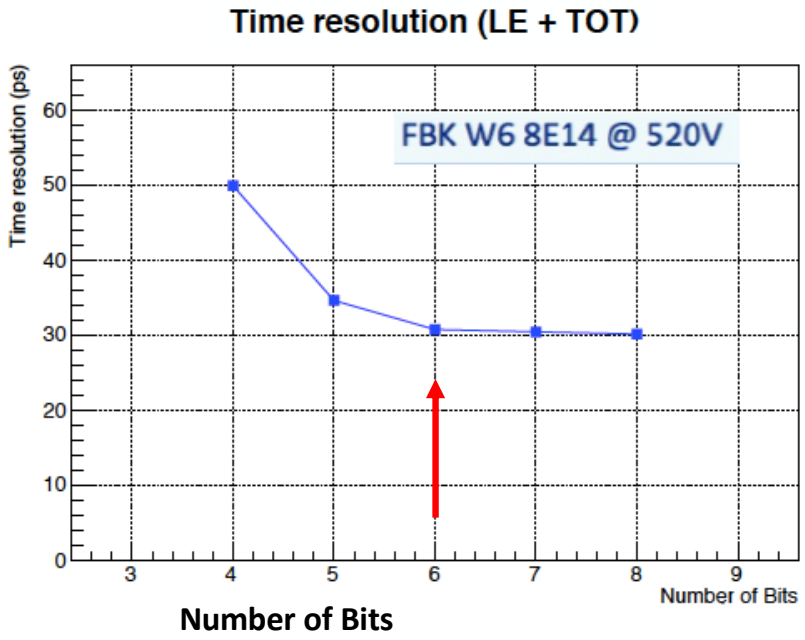


Frequency	40 MHz	320 MHz	1.28 GHz	2.56 GHz	5.12 GHz
Random jitter (ps)	1.5	1.6	1.5	1.6	1.9
Periodic jitter (ps)	1.2	11.1	8.2	2.2	7.2

The random (rms) jitter ~ 2 ps

Waveform Sampler Requirements for ETL (TDR)

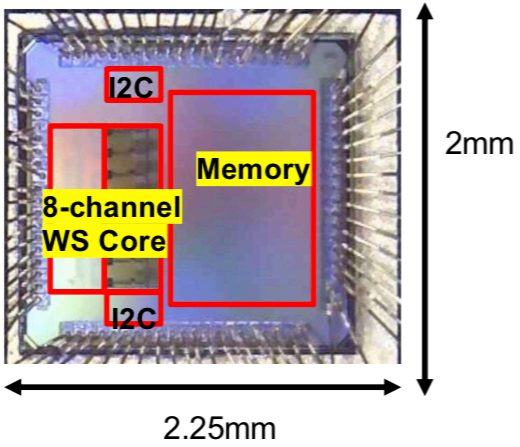


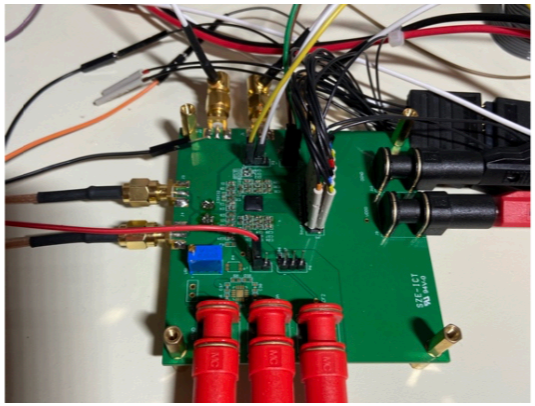


- Analysis based on beam test data sampled by a high-performance oscilloscope
- ≥ 2GS/s sampling rate and ~ 6 bits resolution good

(since preamp output signal is small, we will need a high performance waveform sampler in order to reach ~6 bits resolution)

Preliminary Measurement Results of 2.56GS/s 10-bit Waveform Sampler





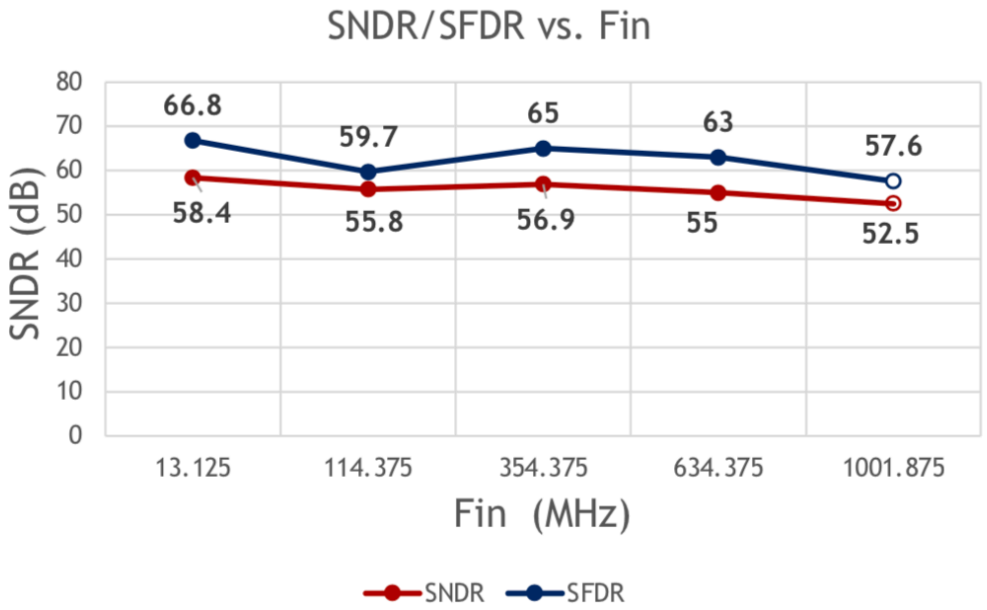
Specs	Measurement Results
Sampling Rate	Up to 2.56 GS/s
ENOB (Effective Number of Bits)	9.4 bits @ 13MHz and 8.4 bit at @1GHz input
Power Consumption	92 mW (when continuous operating)
Core area	1mm x 0.8mm
Topology	Pipelined-SAR
Technology	65nm CMOS

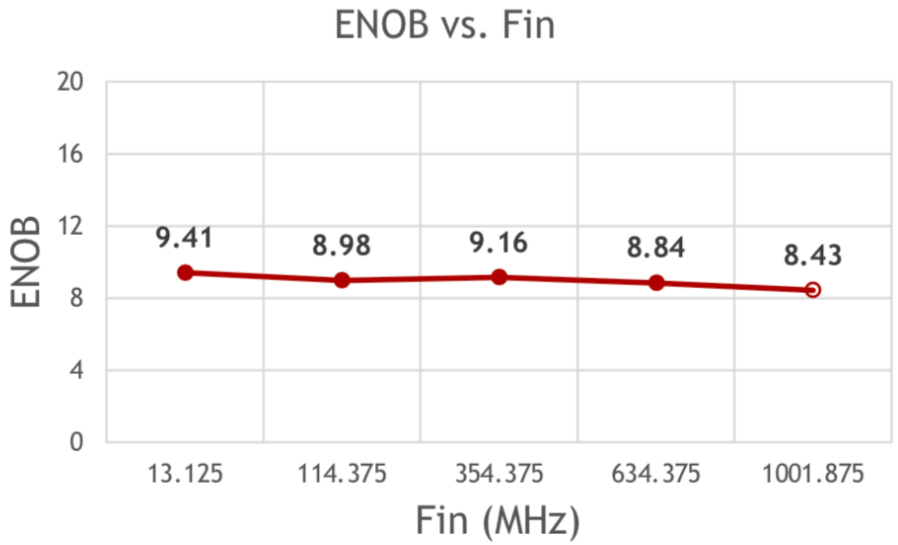
Chip design submitted in March 2020 right before COVID lockdown; More measurements are on-going

Measurement Results:
Dynamic Performance vs. Fin (Sampling Rate = 2.56GS/s)

Two main metrics:

- SNDR: Signal to Noise and Distortion Ratio
- SFDR: Spurious Free Dyanmic Range
- ENOB: Effective number of bits; ENOB = (SNDR-1.76dB) / 6.02



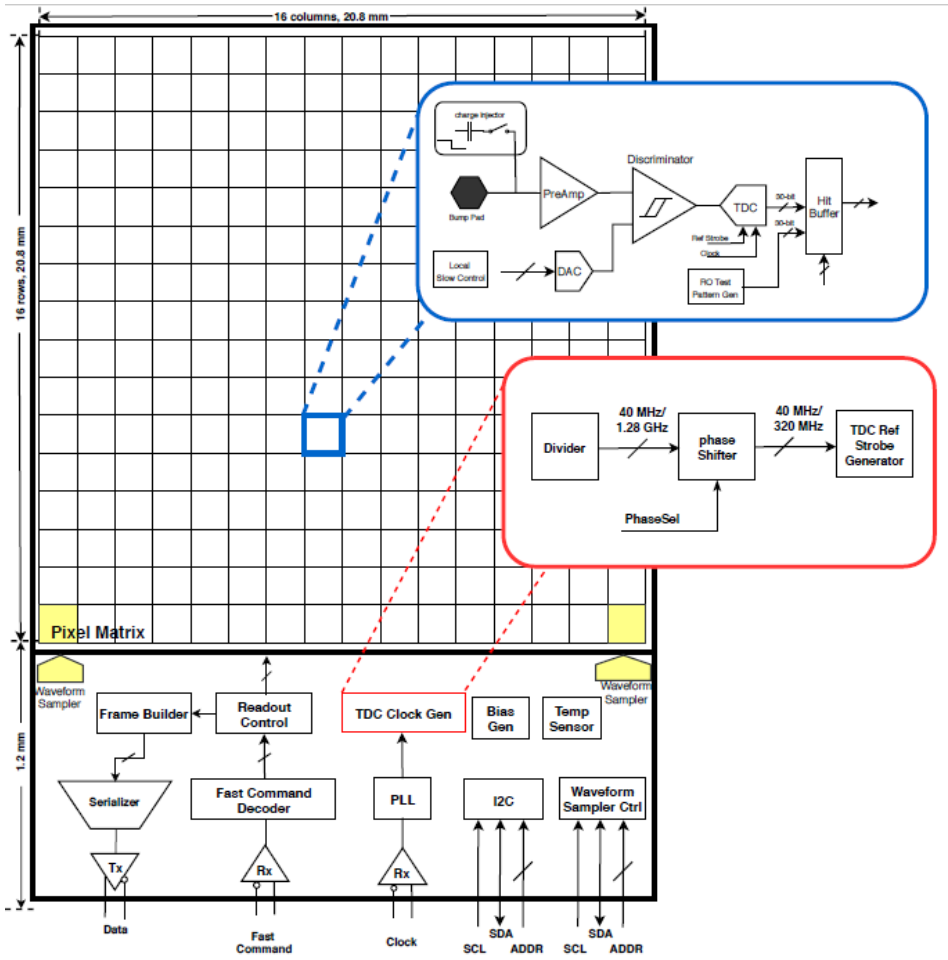


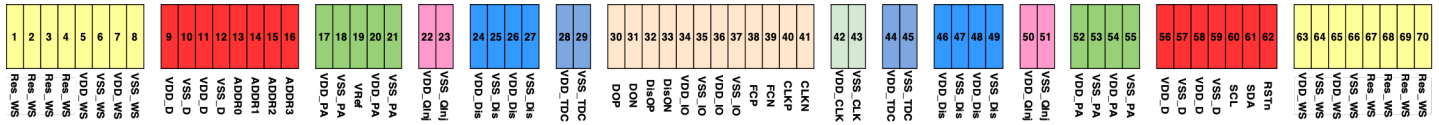
2.56GS/s 10-bit 8-channel Waveform Sampler – on-Chip Memory

- Consisting of 8 RAMs (8 x 512 depth x 13 width) that write in parallel and read in series.
- Speed: Write speed of each small RAM = 320MHz; Read speed = 30MHz
- Overall memory storage size: 4096(depth) x 13(width)
- Overall sampling rate: 2.56GS/s(one sample every ~391ps) → RAM working time frame: 4096x391ps = 1.6us (64 bunch crossings)
- 4096 points FFT: Noise floor is 36dB lower than SNR → Clear spectrum for waveform sampler analysis
- Memory size can be reduced to save area and power

ETROC2: all critical components prototyped

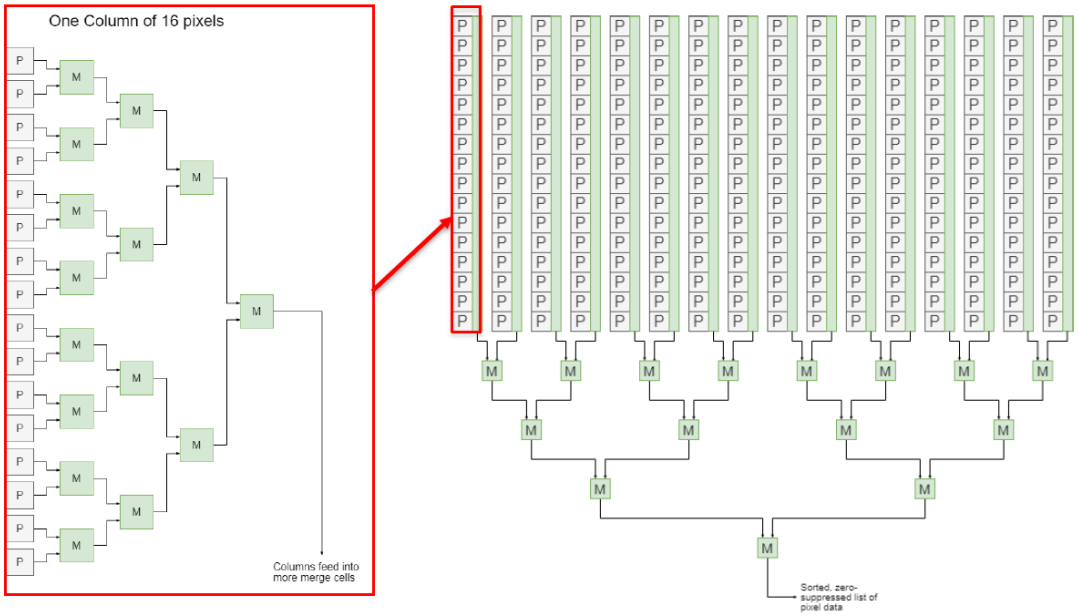
- Aim to submit in Aug 2021
- Full size with full mask engineering run
  - 16 X 16 pixel array
  - 20.8 mm X 22.0 mm
- Full frontend: PA + Discri + TDC
- L1 latency-matched hit buffer
- L1 trigger-driven readout with zero suppression
  - 320 Mbps Serial data to lpGBT
- 320 Mbps fast command from lpGBT
- 40 MHz reference from lpGBT
  - High performance PLL from lpGBT
- I2C slow control
- fast waveform sampling for some pixels
- On-chip temperature sensor



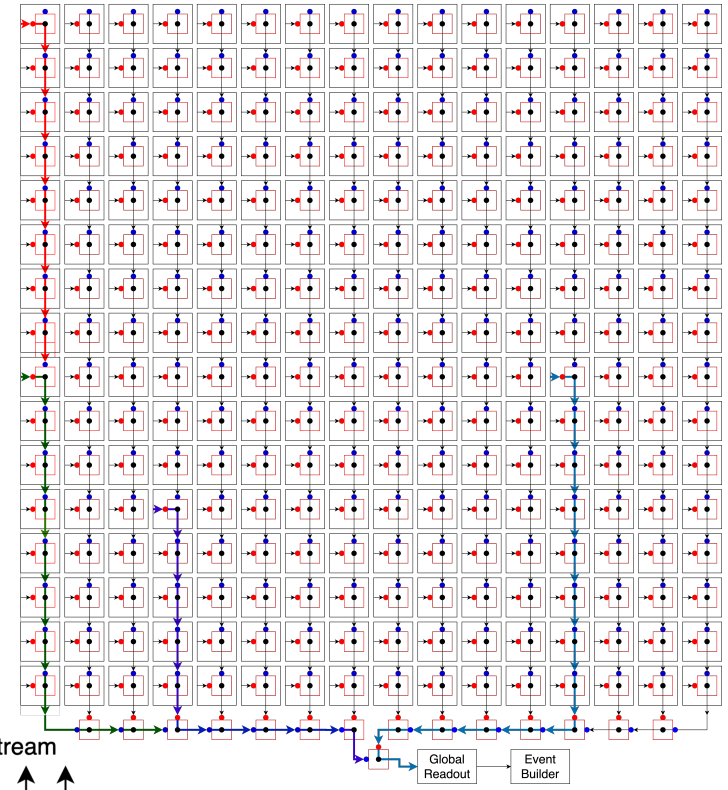


ETROC2 pixel readout design advanced (two approaches developed)

Merge cell approach

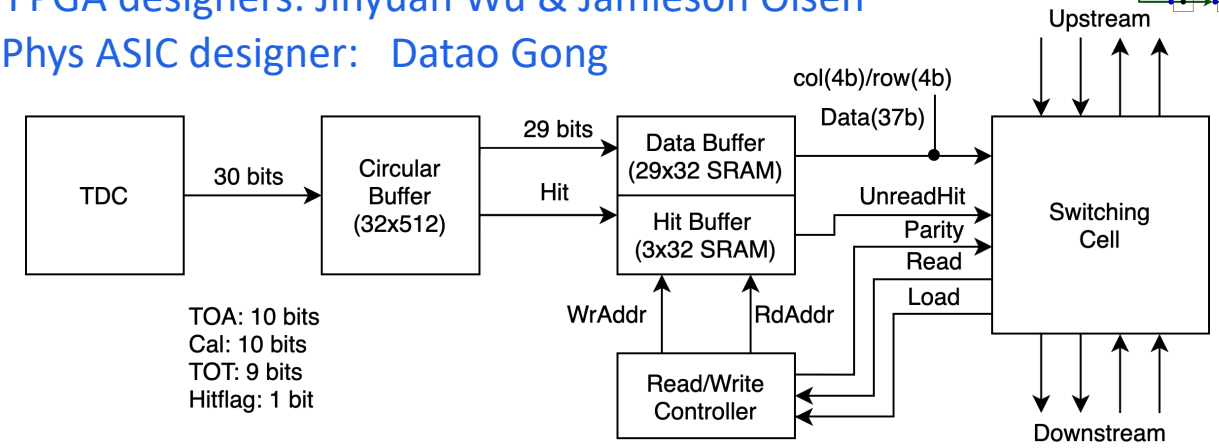


Switch network approach



FNAL FPGA designers: Jinyuan Wu & Jamieson Olsen

SMU Phys ASIC designer: Datao Gong



Both implemented in VHDL, Simulated/tested in FPGA, and will be used in ETROC2 emulator

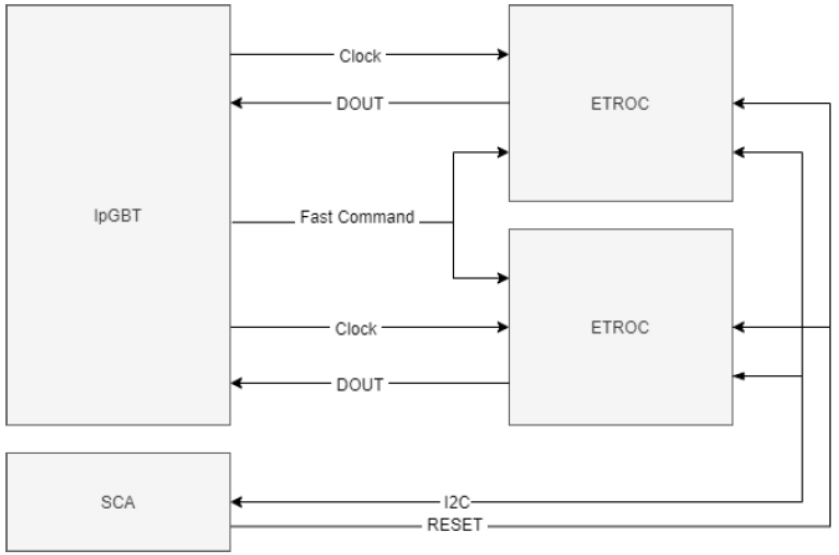
ETROC Fast Command Decoding

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	meaning
			Cal Req	Link Reset	L1A	BC0		
1	1	0	0	0	0	0	1	none
1	1	0	0	0	0	1	1	BC0
1	1	0	0	0	1	0	1	L1A
1	1	0	0	0	1	1	1	BC0 and L1A
1	1	0	0	1	0	0	1	Link reset
1	1	0	0	1	0	1	1	BC0 and link reset
1	1	0	0	1	1	0	1	L1A and link reset
1	1	0	0	1	1	1	1	BC0 and L1A and link reset
1	1	0	1	0	0	0	1	CalReq
1	1	0	1	0	0	1	1	BC0 and cal req
1	1	0	1	0	1	0	1	L1A and cal req
1	1	0	1	0	1	1	1	BC0 and L1A and cal req
1	1	0	1	1	0	0	1	Link reset and cal req
1	1	0	1	1	0	1	1	BC0 and link reset and cal req
1	1	0	1	1	1	0	1	L1A and link reset and cal req
1	1	0	1	1	1	1	1	BC0 and L1A and link reset and cal req

- Orbit Sync / Orbit Counter Reset : required for ETROC to maintain BCID counter
- L1ACC : drives/triggers ETROC readout
- Link-Reset : force the ETROC output link into known test/training pattern
- CalibrationReq : enable front end charge injection circuit
- CalibrationL1A : reserved/TBD

ETROC2 interface

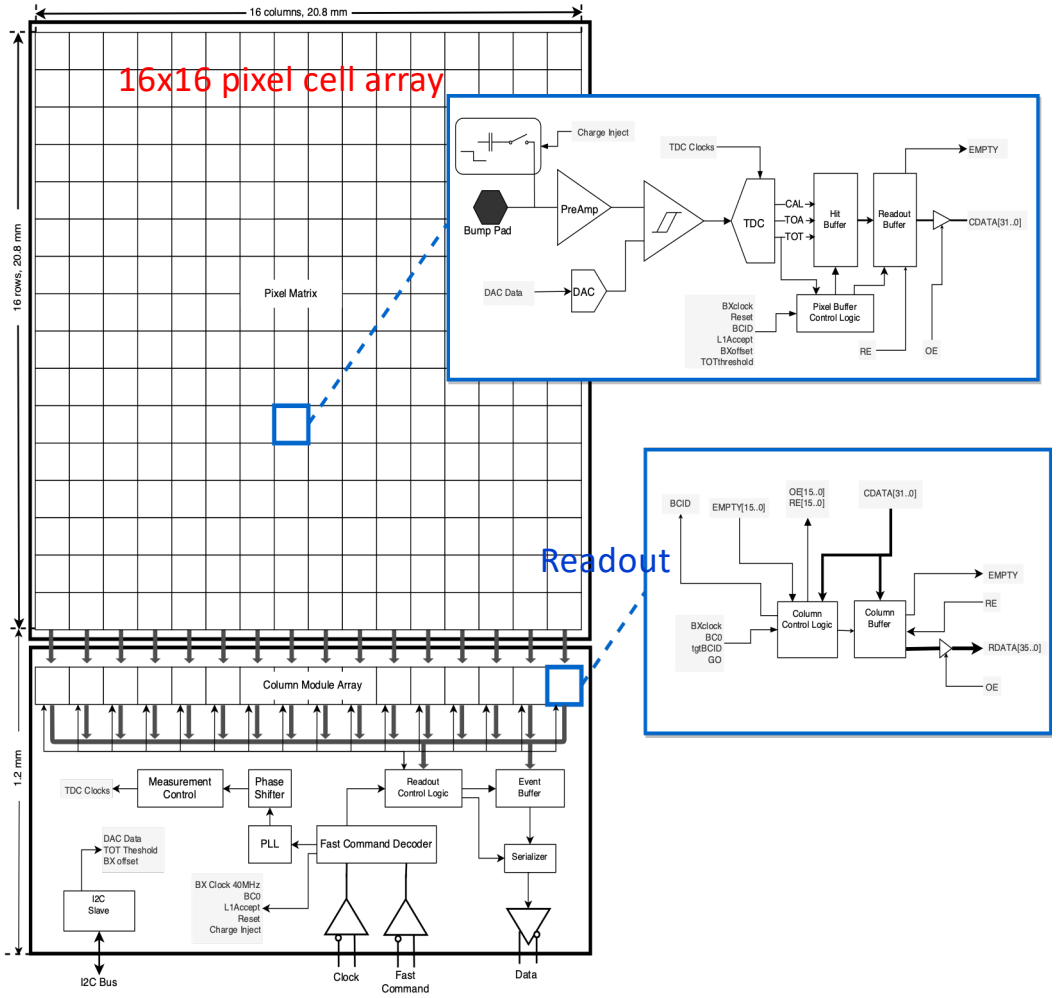
- 40 MHz clock
  - Low jitter clock from lpGBT
  - Point to point differential signaling, not shared
- Fast command
  - 320 Mbps, differential
  - 8 bits per BX
  - Multi-drop, shared by 2 ETROC2
- Data output
  - From 320 Mbps to 1.28 Gbps
  - Point to point link back to lpGBT
- Slow controls I2C & Reset
  - SCA or lpGBT
  - Address pins hardwired to the board
- Waveform sampler interface with dedicated I2C



ETROC2 emulator

ETROC system interfaces can be emulated by FPGA:

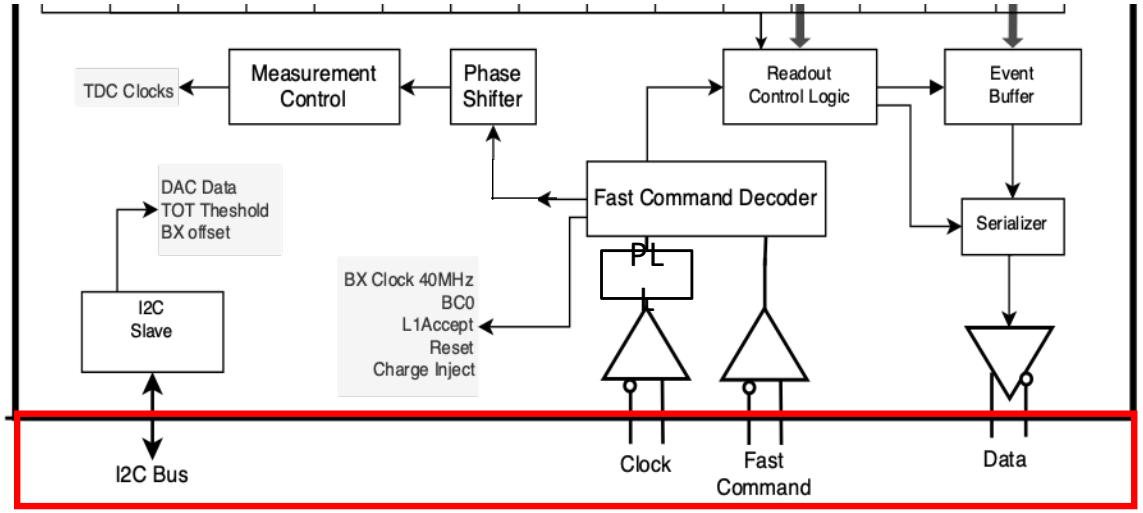
- I2C interface
- Data readout
- Clock input (40MHz distribution)
- Fast command interface
- …



The ETROC interface emulator would allow us to decouple the service hybrid /system development from the ETROC development: in other words, the service hybrid and system (front-end and backend) can be developed and tested before ETROC2 chips are available … and the ETROC interface emulator can help optimize the system interface as well …. To identify issues early.

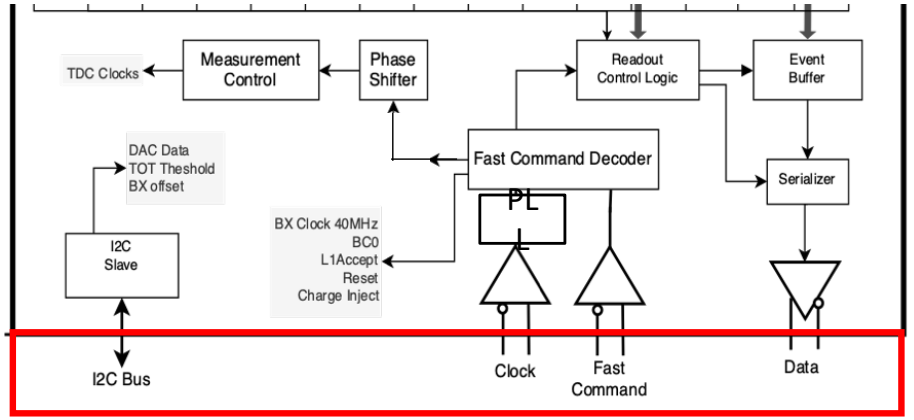
ETROC Interface

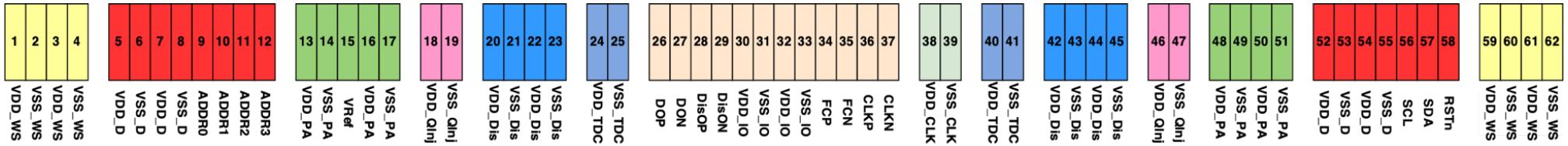
- ETROC is configured via an I2C interface from lpGBT/SCA.
- ETROC receives a differential 40-MHz clock from lpGBT.
- ETROC is controlled by a differential 320-Mbps fast command signal from the lpGBT.
- ETROC sends its data on a differential 320-Mbps (expandable to 640 Mbps or 1.28 Gbps) output to the lpGBT and the off-detector.

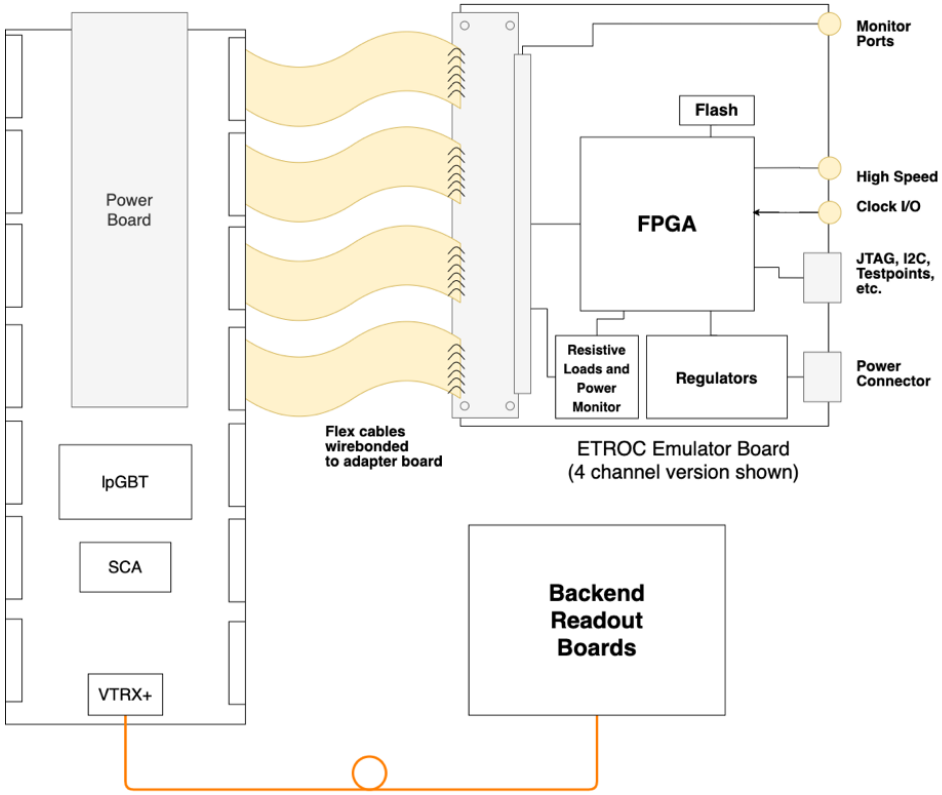


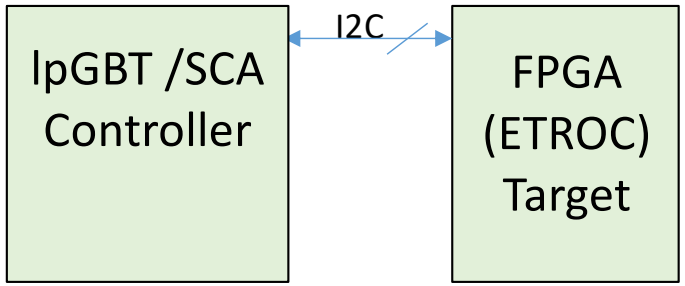
ETROC Interface

Power supply	VDD_QInj	VSS_QInj	1.2 V and ground The emulator may emulate the load of the ETROC power consumption for monitoring
	VDD_PA	VSS_PA	
	VDD_DIS	VSS_DIS	
	VDD_TDC	VSS_TDC	
	VDD_D	VSS_D	
	VDD_CLK	VSS_CLK	
	VDD_IO	VSS_IO	
	VDD_WS	VSS_WS	
Fast diff signals	CLK_P, CLK_N		Input 40M clock
	FCMD_P, FCMD_N		Input fast command at 320 Mbps
	DO_P, DO_N		Digital output at 320 Mbps, expendable to 640 Mbps and 1.28Gbps
slow control	SCL, SDA		I2C
	RESETb		Reset
Monitor	Vref		Output internal analog Vref for monitoring or receive external Vref





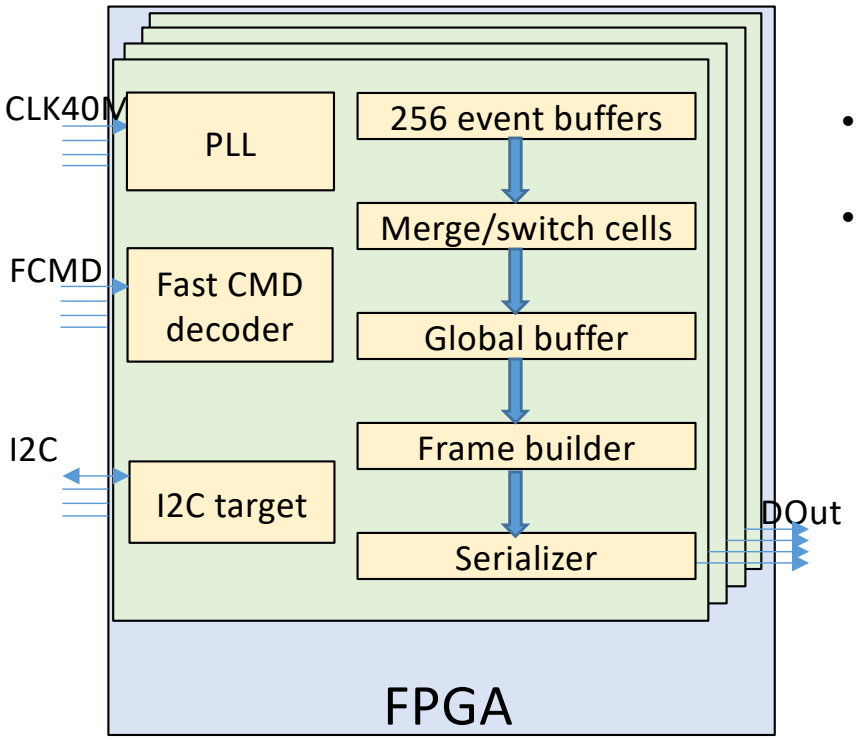




3. FPGA update (1)

- The emulator uses a single FPGA to emulate the functions of a few ETROCs.
- The FPGA interfaces with the lpGBT (or SCA for I2C) located on the readout board.
- The FPGA must be compatible with the lpGBT (or SCA for I2C) on the logic level.
- For I2C configuration, the lpGBT (or SCA) is the I2C controller, while the FPGA (ETROC) is the I2C target.
- The I2C signals (SCL, SDA, RESETb) are 1.2 V CMOS logic (1.5 V CMOS for SCA).
- It is not hard for the FPGA to be compatible with 1.2 V (1.5 V) CMOS logic.

ETROC Emulator Firmware



- The FPGA emulates the following functions of each ETROC: a PLL, a fast command decoder, an I2C target, and a readout logic.
- The PLL generates the internal 320 MHz and 40 MHz clocks.
- The fast command decoder uses the 40-MHz clock as the command boundary and the 320-MHz clock as the sampling clock to recover BC0, L1A, link reset, and other fast commands.
- The I2C target receives slow commands and stores the internal operational states.
- The readout logic fetches the data from the event buffer and transmits the data out of the FPGA. The readout logic implements:
  - 256 event buffers store triggered data (Data Valid flag, TOA, TOT, Calibration) of each pixel. The buffer depth, which depends on the readout algorithms, is to be decided later.
  - Merge cells or switch cells transfer the triggered data in proper order from 256 event buffers to a global output buffer.
  - A global buffer stores triggered data before framing.
  - A frame builder adds frame headers, frame trailers, and frame fillers (when no event is triggered).
  - A serializer converts parallel data to serial data.

The firmware development is in progress. Fast command decoder, I2C target, frame builder/aligner (constant word length option) have been implemented and verified. Readout logic has been simulated or implemented.
All the firmware blocks will be migrated and integrated to the new FPGA platform.

Overall expected ETROC performance

Time resolution

LGAD+ preamp/discriminator + TDC bin	35 ps	40/46
Time-walk correction residual	< 10 ps	
Internal clock distribution	< 10 ps	
System clock distribution	< 15 ps	
Per hit total time resolution	41 ps	45/50
Per track (2 hits) total time resolution	29 ps	32/35

→ ***To be verified with ETROC1***

With safety margin:
design specification is
~ 35ps per track (~50ps per hit),
< ~ 60ps per track at end of life
(~80 ps per hit)

Power consumption

Circuit component	Power per channel [mW]	Power per ASIC [mW]
Preamplifier (low-setting)	0.67	171.5
Preamplifier (high-setting)	1.25	320
Discriminator	0.71	181.8
TDC	0.2	51.2
SRAM	0.35	89.6
Supporting circuitry	0.2	51.2
Global circuitry		200
Total (low-setting)	2.13	745
Total (high-setting)	2.71	894

All confirmed

achieved 0.1mW

With some safety margin:
design specification is
~ 1W per chip

ETROC power consumption measurements

Final ETROC0/1 design simulation results

Circuit component	Power per channel [mW]		Power per ASIC [mW]
Preamplifier (low-setting)	0.67	0.76 0.74	171.5
Preamplifier (high-setting)	1.25	1.31 1.27	320
Discriminator	0.71	0.87 0.84	181.8
TDC	0.2	0.07 0.1	51.2
SRAM	0.35	0.25 (new)	89.6
Supporting circuitry	0.2	0.2 (reserve)	51.2
Global circuitry			200

226.5

- Measurements agree with simulation of ETROC0 and 1 design
  - TT corner numbers shown, mostly agree reasonably well
  - But should assume up to 20% variation with real production
  - Note: preamp highest setting (4th gear) power is 1.52mW (measured)
- The new 0.25mW SRAM is based on most recent estimate by expert
- The "supporting circuitry": reserved for circuitry hard to be separated clearly
- The "global circuitry" (a guess back then for TDR, with large uncertainty)
  - ***A lot is known now about global circuitry blocks (ETROC2 simulation)***
    - ***PLL: 60mW; Phase shifter: 2 mW; Clock distribution: 25mW;***
    - ***Tx: 16mW; Rx 1mW. Fast command decoder: 2mW***
    - ***Voltage reference generator: 0.5mW.***
    - ***Readout: 100mW (guess so far); other misc: 20mW (guess)***

106.5
+
120
= 226.5 mW

ETROC power consumption update

Final ETROC0/1 design simulation results vs measured

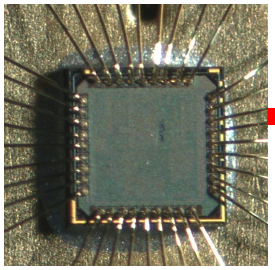
Circuit component	Power per channel [mW]		Power per ASIC [mW]	
Preamplifier (low-setting)	0.67	0.76 0.74	171.5	190
Preamplifier (high-setting)	1.25	1.31 1.27	320	325
Discriminator	0.71	0.87 0.84	181.8	215
TDC	0.2	0.07 0.1	51.2	26
SRAM	0.35	0.25 (new)	89.6	64
Supporting circuitry	0.2	0.2 (reserve)	51.2	51
Global circuitry			200	226.5
Total (low-setting)	2.13	2.13	745	773
Total (high-setting)	2.71	2.66	894	908
Total (highest setting)		2.91		972

We are still within 1W/chip spec!

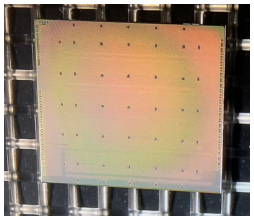
- Measurements agree with simulation of ETROC0 and 1 design
  - TT corner numbers shown, mostly agree reasonably well
  - ***But should assume up to 20% variation with real production***
  - Note: preamp highest setting power is 1.52mW x 256 = 389 mW
  - TDC power is assuming 1% occupancy…. (see next slide)
    - At 10% occupancy, from 0.1mW to 0.32mW (0.22mW x 256 = 56mW)
    - *Will need to add 56mW to the total power IF 10% TDC occupancy.*

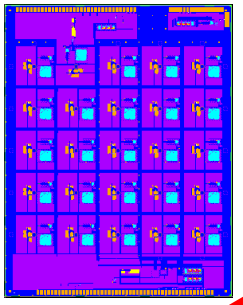
Towards ETROC2 and Front-end System Design

ETROC2 readout design is critical from system point of view

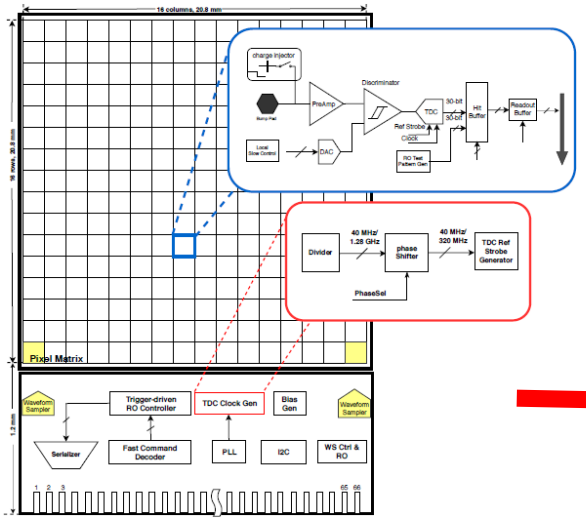


ETROC0





ETROC1



ETROC2

- Aim to submit in Q2 2021
- Designed to be compatible with 16 X 16 pixel array with full functionalities

ETROC3

Sensor design

Bump-bonding R&D

Module design

Readout board design

Power board design

ETROC2 emulator

Backend firmware/software

All designs have to be mature enough in order to finalize ETROC2 design

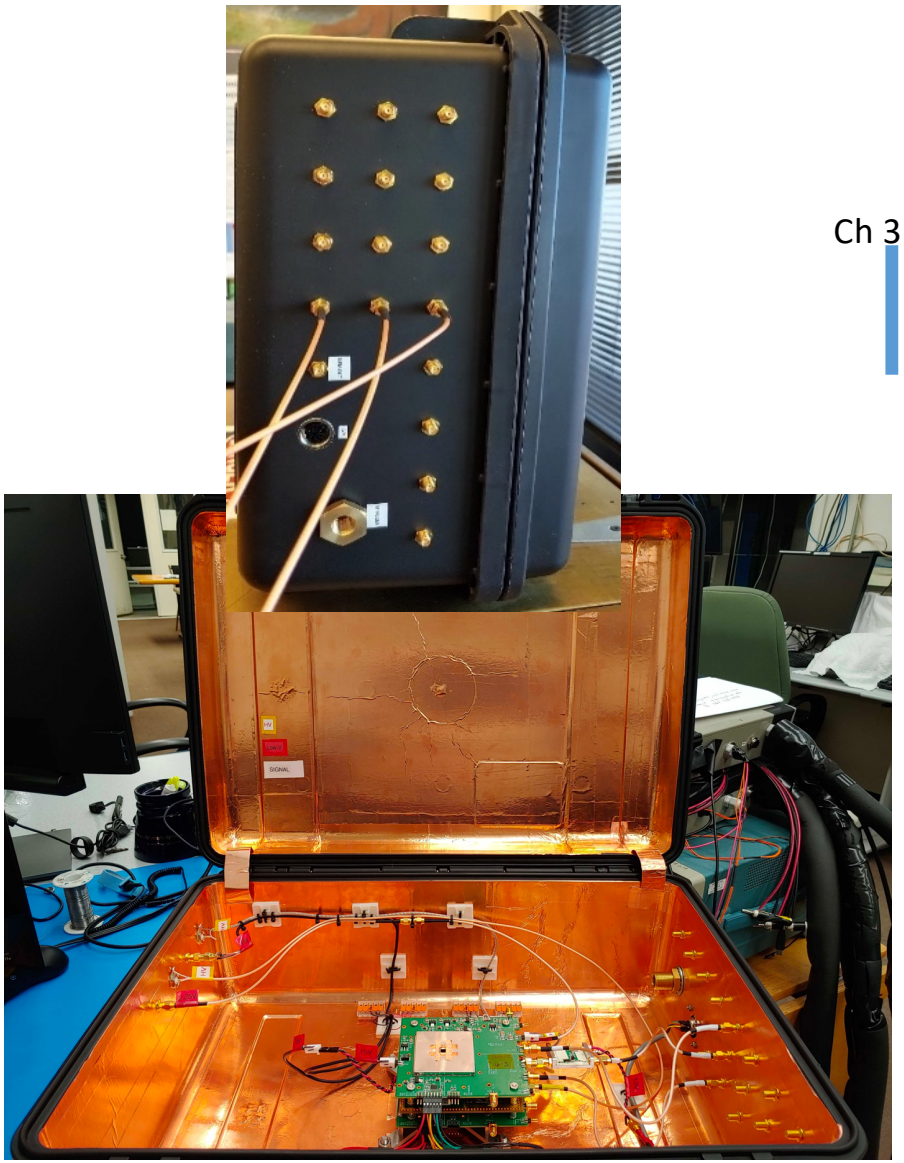
All prototypes have to be good enough in order to test ETROC2 at system level in time to move to ETROC3

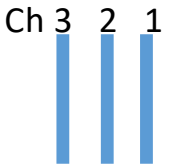
A simple ETROC0 Beam Telescope (3 boards)

Jan-Feb 2020

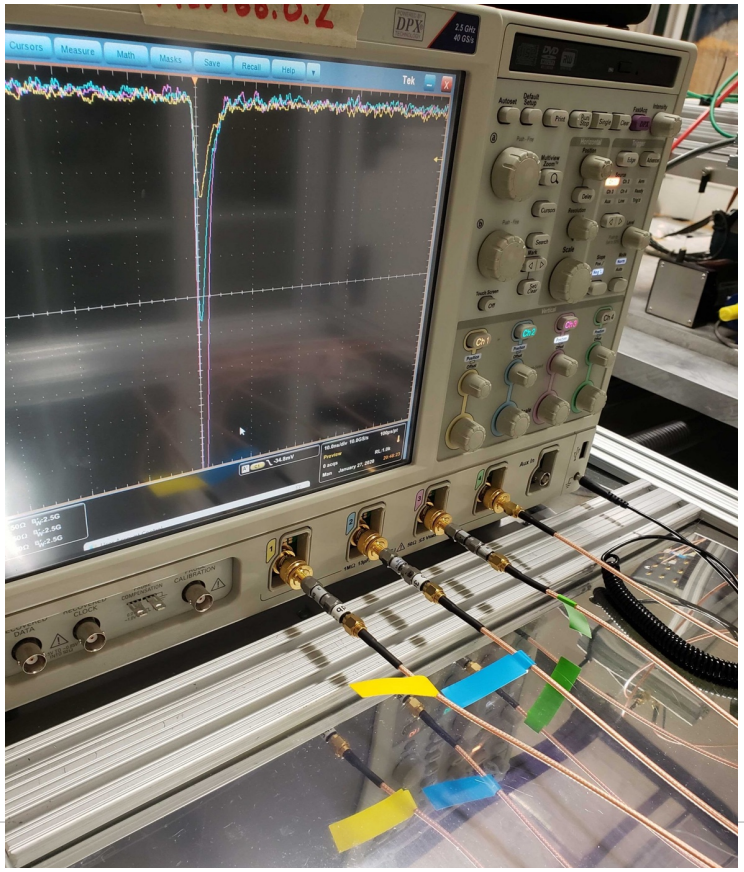
Simple "suitcase" setup in parasitic mode running at FNAL MTest

Designer: ***Chris Edwards***





120 GeV proton Beam

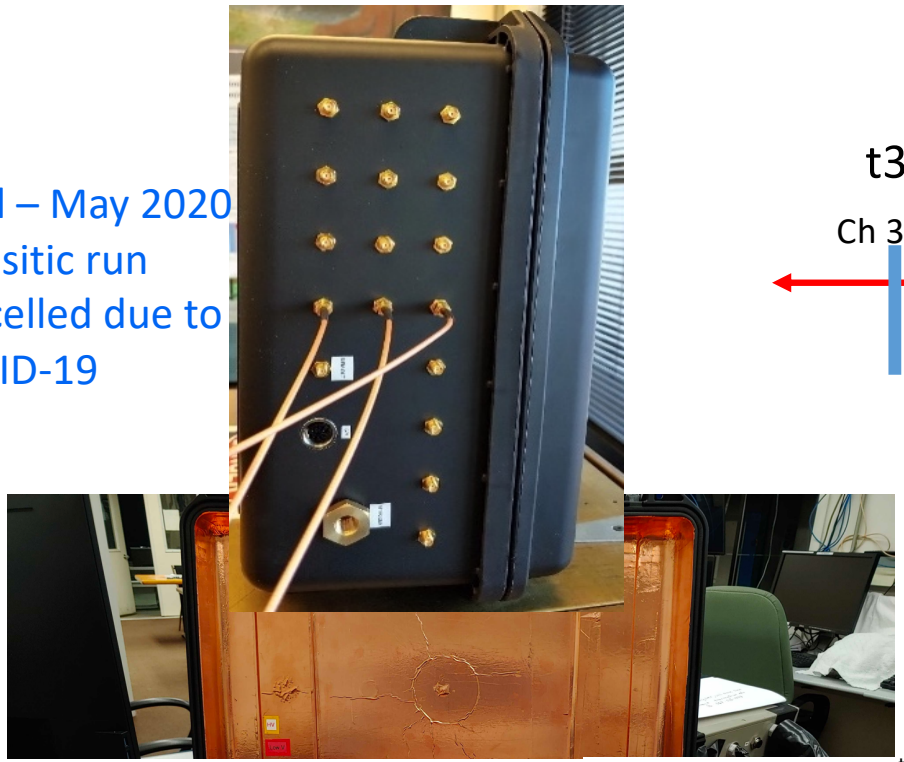


A simple Beam Telescope (with 3 HPK-ETROC0 boards)

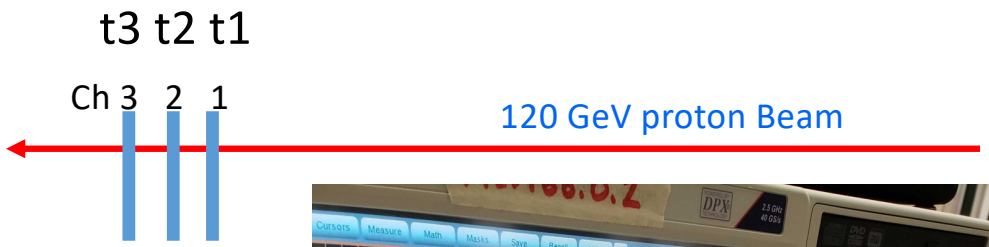
Jan-Feb 2020

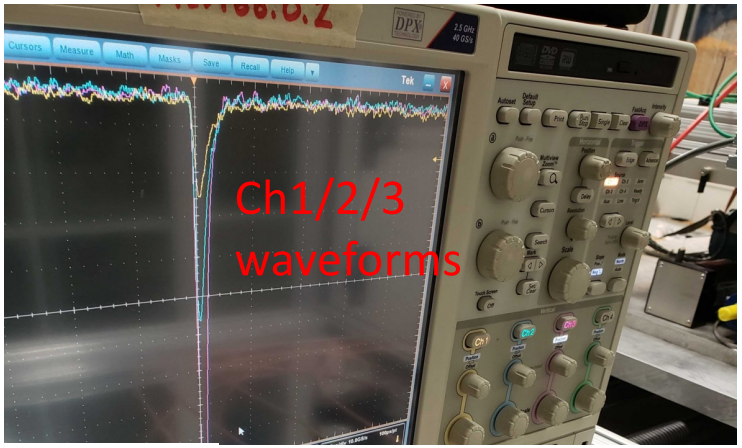
Simple "suitcase" setup in parasitic mode running at FNAL MTest

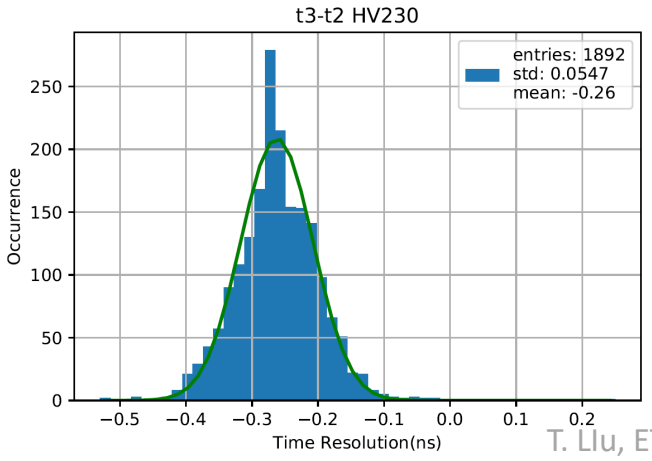
April – May 2020 parasitic run cancelled due to COVID-19

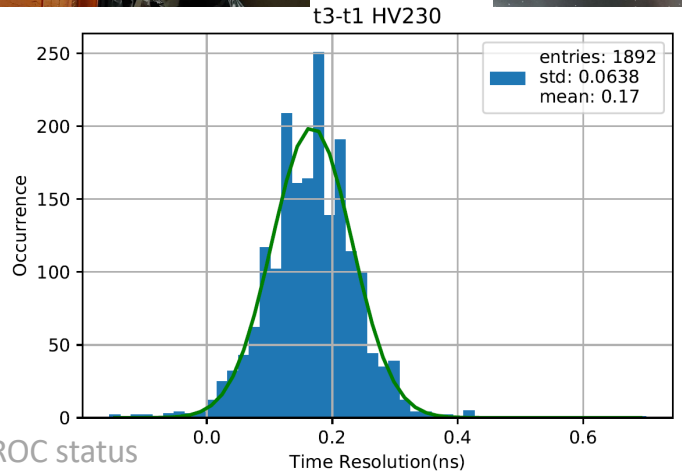


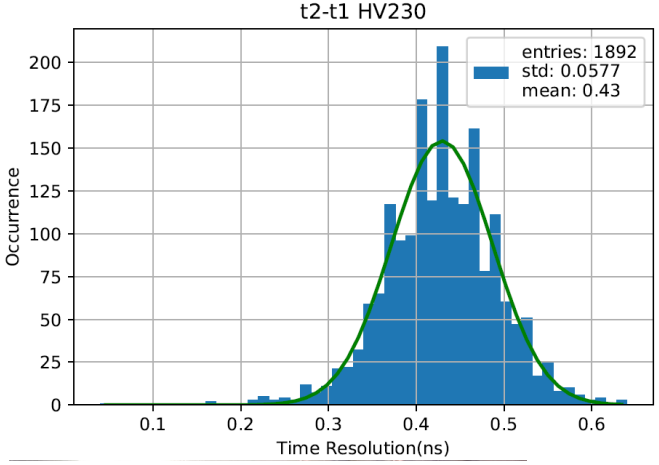
$$\sigma_2 = \sqrt{0.5 \cdot (\sigma_{21}^2 + \sigma_{32}^2 - \sigma_{31}^2)} \approx 33\ (ps)$$

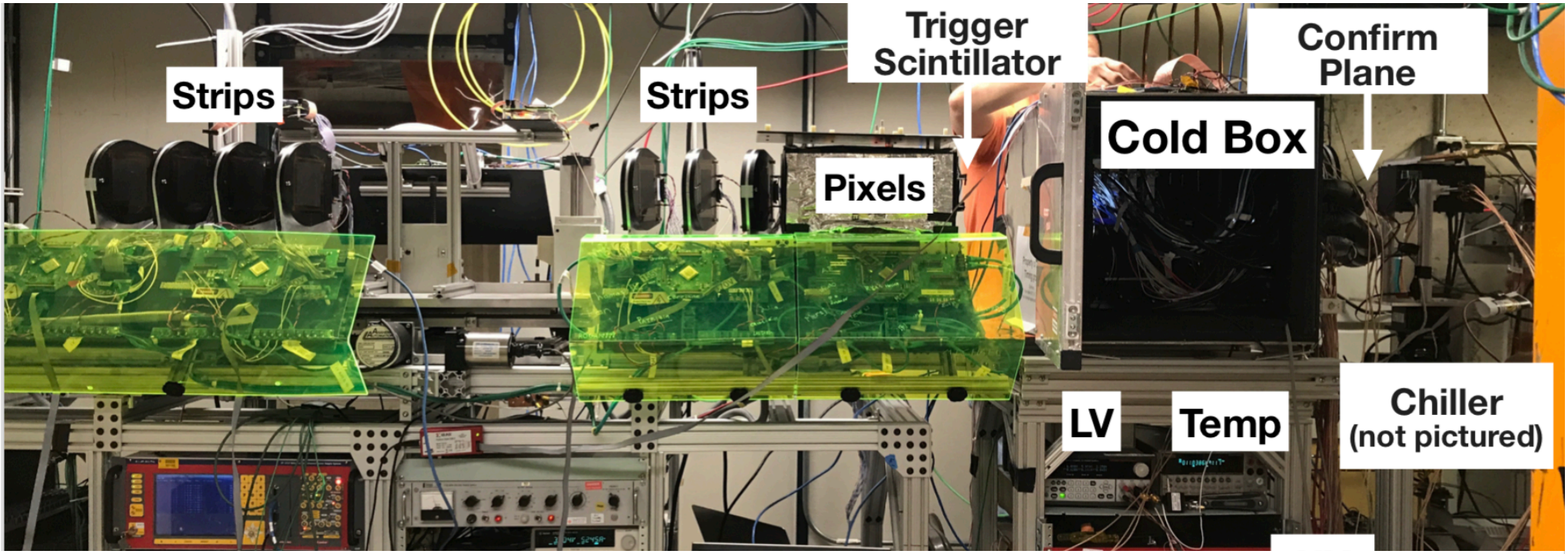




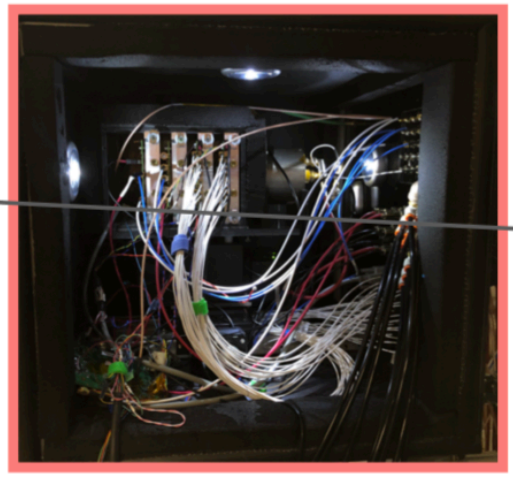








Strip and Pixel Telescope



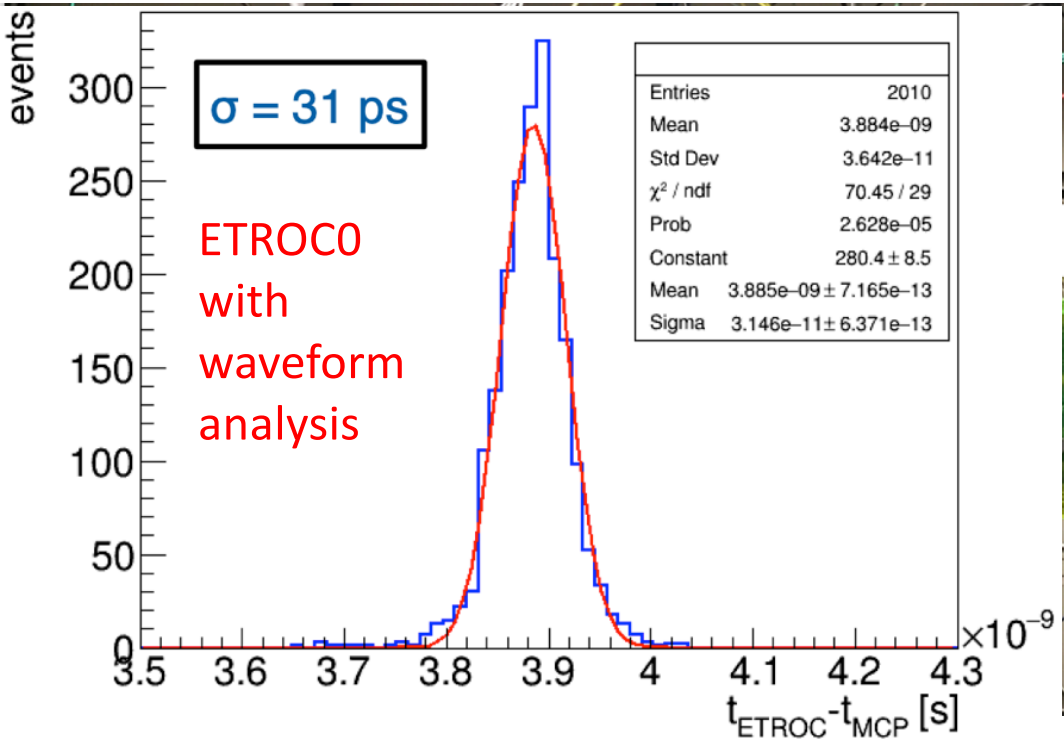
HPK-ETROC0 testing with ***full tracking***

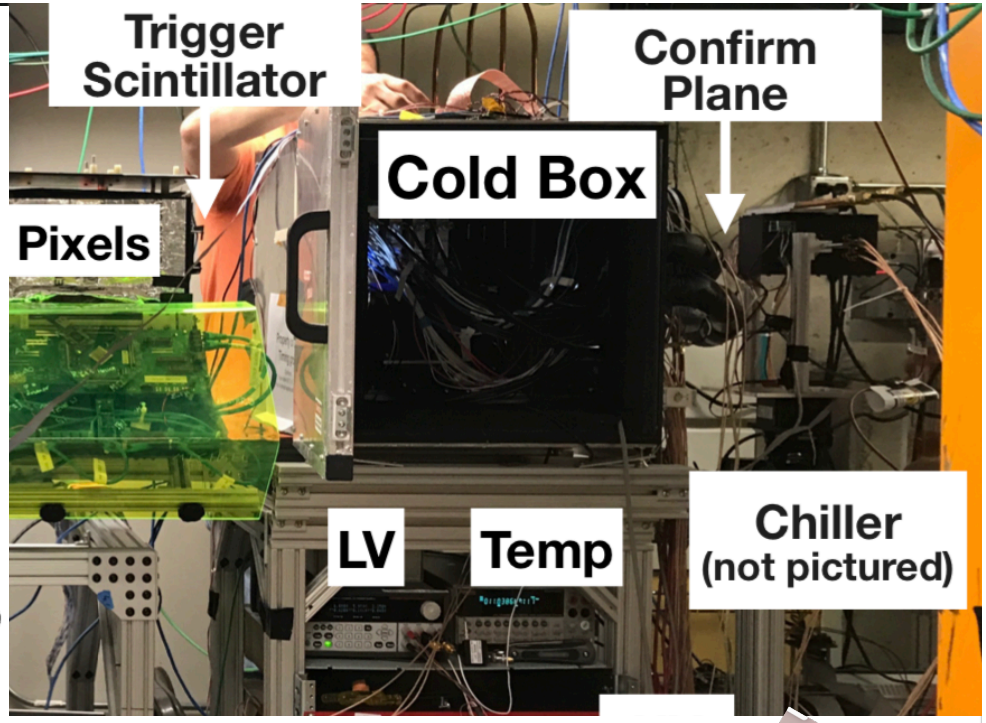
- MTD Beam Test Setup at FNAL MTest
  - Independent scintillator provides trigger
  - Telescope provides proton track
  - Oscilloscope saves waveforms
  - Study Δt(LGAD,MCP)

Cold box

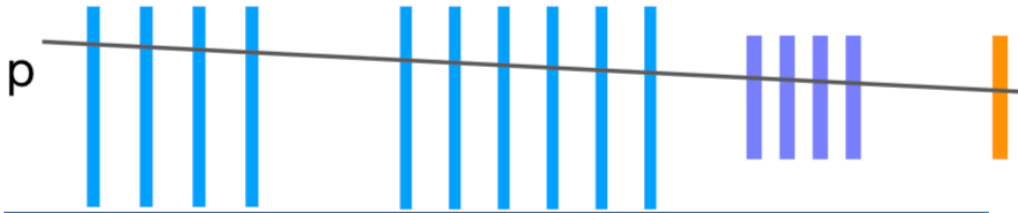
LGAD boards on cooling blocks

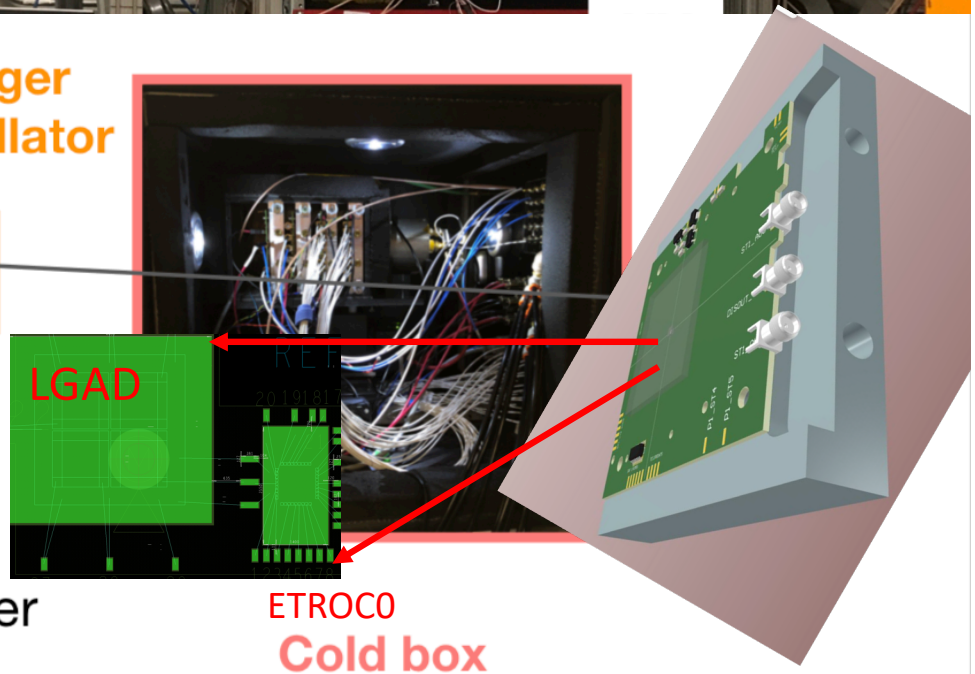
MCP (Photek) time reference





Strip and Pixel Telescope





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