ECON ASICs

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ASICs PMG
14 September 2020

ECON-T status

- Chinar working on layout with econt_top v74
  - Davide has helped with floor plan of periphery (I/O, power rings, eRx, eTx, serializer)

- Ralph recently provide econt_top v78 RTL
  - modifications to simplify the formatter place-and-route
  - mods to address small bugs discovered during block- and top-level verification

- Ralph now working on econt_top v79
  - small changes for interrupt signal affects two blocks

- Alpana has completed block synthesis and place-and-route for v78; waiting for econt_top v79

- Chinar working on layout with econt_top v74, but moving to v78 which is now available

- UVM : Cristian and Danny Noonan maintain progress despite **lack of Jim Hoff's availability since August 23**; Ralph says Jim's absence is relatively manageable.

- Xiaoran PLL schedule:
  - Aug 27 plan: PLL abstract due Sep 03, final PLL due Oct 01 (4 wks development)
  - Sep 10 plan : PLL abstract due Sep 17, final PLL due **Oct 22** (5 wks development b/c of DUNE sim)

DUNE delays for Xiaoran have already precluded October ECON-T submission, which was previous "drop dead date." Additional delays would threaten November ECON-T submission.

ECON Schedule with 2 prototype stages

	2020				2021												2022												2023							
	S	O	N	D	J	F	M	A	M	J	J	A	S	O	N	D	J	F	M	A	M	J	J	A	S	O	N	D	J	F	M	A	M	J	J	
ECON-T design	Design																																			
ECON-D design	Design																																			
ECON-T p1				Fab			Package		Test																											
ECON-D p1								Fab			Package		Test																							
V3 System Test									System Test																											
Design modifications											Design																									
Prototype 2																	Fab			Package		Test														
Prepare for production																								Design												
ECON-T/D Production																											Fab			Package		Test				**Total**
Ralph Wickwire	0.9	0.9	0.9	0.9	0.9	0.9	0.9				0.9	0.9	0.9	0.9	0.9	0.9								0.9	0.9	0.9										**14**
Chinar Syal	0.9	0.9	0.9	0.9	0.9	0.9	0.9				0.9	0.9	0.9	0.9	0.9	0.9								0.9	0.9	0.9										**14**
Alpana Shenai	0.7	0.7	0.7	0.7	0.7	0.7	0.7				0.7	0.7	0.7	0.7	0.7	0.7																				**9**
Jim Hoff	0.5	0.5	0.5	0.5	0.5	0.5	0.5				0.5	0.5	0.5	0.5	0.5	0.5								0.5	0.5	0.5										**8**
Cristian Gingu	0.8	0.8	0.8	0.8	0.8	0.8	0.8				0.8	0.8	0.8	0.8	0.8	0.8								0.8	0.8	0.8										**13**
Davide Braga	0.5																																				**1**
Xiaoran Wang	0.9	0.9	0.9																																		**3**
Test person (Scott?)		0.9	0.9	0.9	0.9	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5			0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5			0.5	0.5	0.5	0.5	0.5	0.5	0.5	**17**
Total	**5.2**	**5.6**	**5.6**	**4.7**	**4.7**	**4.3**	**4.3**	**0.5**	**0.5**	**0.5**	**4.3**	**4.3**	**4.3**	**4.3**	**4.3**	**4.3**	**0**	**0**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**3.6**	**3.6**	**3.6**	**0**	**0**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**79**

- 2nd prototype stage included in US project as risk with high probability
- Person power needs are (hopefully) high.
- Numbers for each name are FTE-months.

- Yellow FTE : associated with 2nd prototype stage
- Cyan FTE : associated with prototype and production

ECON Schedule with 1 prototype stage

	2020				2021												2022												
	S	O	N	D	J	F	M	A	M	J	J	A	S	O	N	D	J	F	M	A	M	J	J	A	S	O	N	D	
ECON-T design	Design																												
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V3 System Test									System Test																				
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ECON-T/D Production																			Fab			Package		Test					**Total**
Ralph Wickwire	0.9	0.9	0.9	0.9	0.9	0.9	0.9									0.9	0.9	0.9											**9**
Chinar Syal	0.9	0.9	0.9	0.9	0.9	0.9	0.9									0.9	0.9	0.9											**9**
Alpana	0.7	0.7	0.7	0.7	0.7	0.7	0.7																						**5**
Jim Hoff	0.5	0.5	0.5	0.5	0.5	0.5	0.5									0.5	0.5	0.5											**5**
Cristian Gingu	0.8	0.8	0.8	0.8	0.8	0.8	0.8									0.8	0.8	0.8											**8**
Davide Braga	0.5																												**1**
Xiaoran Wang	0.9	0.9	0.9																										**3**
Test person (Scott?)		0.9	0.9	0.9	0.9	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5			0.5	0.5	0.5	0.5	0.5	0.5	0.5		**14**
Total	**5.2**	**5.6**	**5.6**	**4.7**	**4.7**	**4.3**	**4.3**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**3.6**	**3.6**	**3.6**	**0**	**0**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**		**53**

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More details on ECON-T status

- Status of block level synthesis / place-and-route (S + PnR)
- Power+I/O floor plan & serializer
- Top-level S+PnR
- Verification
- PLL
- Other topics

Block synthesis + PnR dashboard : Top v74

- Synthesis + PnR redone for each block when RTL reaches ~stable point.
- **RTL designers now set up** to run synthesis flow developed by PnR team
  - catch bugs before passing to PnR team
  - confirm small RTL changes ➔ small netlist changes
  - adjust RTL to meet timing and area

Synthesis

CellName	RTL	Date	Cell Area	Net Area	Total Area	Square Root of area	Sequential Instance	Combinational Instance	Leakage Power(nW)	Dynamic Power(nW)	Total Power
algorithm_wrap	✓	4-Aug	523004	243818	766822	876	18150	125724	180921	32584670	32765592
channel_wrap	✓	5-Aug	58250	32211	90461	301	3189	13929	14956	1948562	1963519
common_aligner_wrap	✓	4-Aug	30800	12192	42992	207	2355	5758	8652	1523986	1532638
econt_buf	✓	5-Aug	431078	238154	669233	818	23070	105435	123542		
fast_control_v3_wrap	✓	3-Aug	4599	1581	6181	79	429	691	1224	181545	182770
formatter_wrap	✓	5-Aug	577816	260771	838588	916	2946	149172	229817		
i2c_v2	✓	10-Aug	47815	21705	69521	264	3331	9920	13217	462637	475854
mux_fix_calib_wrap	✓	3-Aug	295635	134623	430258	656	11547	63973	101162	16606722	430258
pll_control_wrap	✓	31-Jul	28173	11498	39671	199	2126	5465	7626	679800	687427

PnR

CellName	RTL	Date	Size	DRC/LVS	Not final= ✘	Path
algorithm_wrap	✓	19-Aug	650x1500	✓	✘	/asic/projects/E/ECON_T_P1/shenai/ECONT_P1_Digital/algorithm/algorithm_wrap
channel_wrap	✓	5-Aug	400x250	✓	✘	/asic/projects/E/ECON_T_P1/shenai/ECONT_P1_Digital/aligner/channel_wrap
common_aligner_wrap	✓	20-Aug	350x150	✓	✘	/asic/projects/E/ECON_T_P1/shenai/ECONT_P1_Digital/aligner/common_aligner_wrap
econt_buf	✓	7-Aug	1000x1500	✓	✘	/asic/projects/E/ECON_T_P1/shenai/ECONT_P1_Digital/formatter_buffer/econt_buf/
fast_control_v3_wrap	✓	3-Aug	250x30	✓	✘	/asic/projects/E/ECON_T_P1/shenai/ECONT_P1_Digital/fast_ctrl/fast_control_v3_wrap
formatter_wrap	✓		350x1200		✘	/asic/projects/E/ECON_T_P1/shenai/ECONT_P1_Digital/formatter_buffer/formatter_wrap
i2c_v2	✓	12-Aug	300x250	✓	✘	/asic/projects/E/ECON_T_P1/shenai/ECONT_P1_Digital/i2c/i2c_v2
mux_fix_calib_wrap	✓	5-Aug	450x1000	✓	✘	/asic/projects/E/ECON_T_P1/shenai/ECONT_P1_Digital/mux_fix_calib/mux_fix_calib_wrap
pll_control_wrap	✓	3-Aug	200x200	✓	✘	/asic/projects/E/ECON_T_P1/shenai/ECONT_P1_Digital/pll_clocks_reset

Block synthesis + PnR dashboard : Top v78

Expected RTL changes after v78

- **formatter_wrap** : adjust RTL to optimize size
- **common_aligner_wrap** : add interrupt signals
- **aligner, mux-fix-calib, algorithms, formatter, buffer** : potential to add functionality for debugging registers

Synthesis

CellName	RTL	Date	Time (min)	Cell Area	Net Area	Total Area	sqrt(Area)	Sequential Instance	Combinational Instance	Leakage Power (nW)	Dynamic Power (nW)	Total Power (nW)
algorithm_wrap	✓	2-Sep	221	523004	243818	766822	876	18150	125724	180921	32584670	32765592
channel_wrap	✓	3-Sep	10	58153	32276	90429	301	3189	13914	14860	1223547	1238408
common_aligner_wrap	✓	3-Sep	3	30800	12266	43066	208	2355	5763	8627	1280111	1288739
econt_buf	✓	3-Sep	121	410037	226614	636652	798	23070	94385	111804	8149000	22505800
fast_control_v3_wrap	✓	30-Aug	1	5929	1964	7894	89	582	836	1524	210199	211723
formatter_wrap	✓	2-Sep	462	634366	279184	913550	956	4464	159606	245859	202040000	35671800
i2c_v2	✓	30-Aug	5	47912	21746	69658	264	3349	9931	13255	2258579	2271834
mux_fix_calib_wrap	✓	3-Sep	21	294214	134263	428478	655	11547	63627	100660	16617292	16717953
pll_control_wrap	✓	28-Aug	3	28045	11530	39575	199	2117	5504	7790	1288192	1295982

PnR

CellName	RTL	Date	Size	DRC/LVS	Not final= ✘	Path
algorithm_wrap	✓		650x1500		✘	/asic/projects/E/ECON_T_P1/shenai/ECONT_P1_Digital/algorithm/algorithm_wrap
channel_wrap	✓		400x250		✘	/asic/projects/E/ECON_T_P1/shenai/ECONT_P1_Digital/aligner/channel_wrap
common_aligner_wrap	✓		350x150		✘	/asic/projects/E/ECON_T_P1/shenai/ECONT_P1_Digital/aligner/common_aligner_wrap
econt_buf	✓		1000x1500		✘	/asic/projects/E/ECON_T_P1/shenai/ECONT_P1_Digital/formatter_buffer/econt_buf/
fast_control_v3_wrap	✓	3-Sep	250x30	✓	✘	/asic/projects/E/ECON_T_P1/shenai/ECONT_P1_Digital/fast_ctrl/fast_control_v3_wrap/fast_control_v3_78
formatter_wrap	✓		350x1200		✘	/asic/projects/E/ECON_T_P1/shenai/ECONT_P1_Digital/formatter_buffer/formatter_wrap
i2c_v2	✓	2-Sep	300x250	✓	✘	/asic/projects/E/ECON_T_P1/shenai/ECONT_P1_Digital/i2c/i2c_v2
mux_fix_calib_wrap	✓		450x1000		✘	/asic/projects/E/ECON_T_P1/shenai/ECONT_P1_Digital/mux_fix_calib/mux_fix_calib_wrap
pll_control_wrap	✓	1-Sep	200x200	✓	✘	/asic/projects/E/ECON_T_P1/shenai/ECONT_P1_Digital/pll_clocks_reset/pll_control_wrap/pll_control_wrap_78

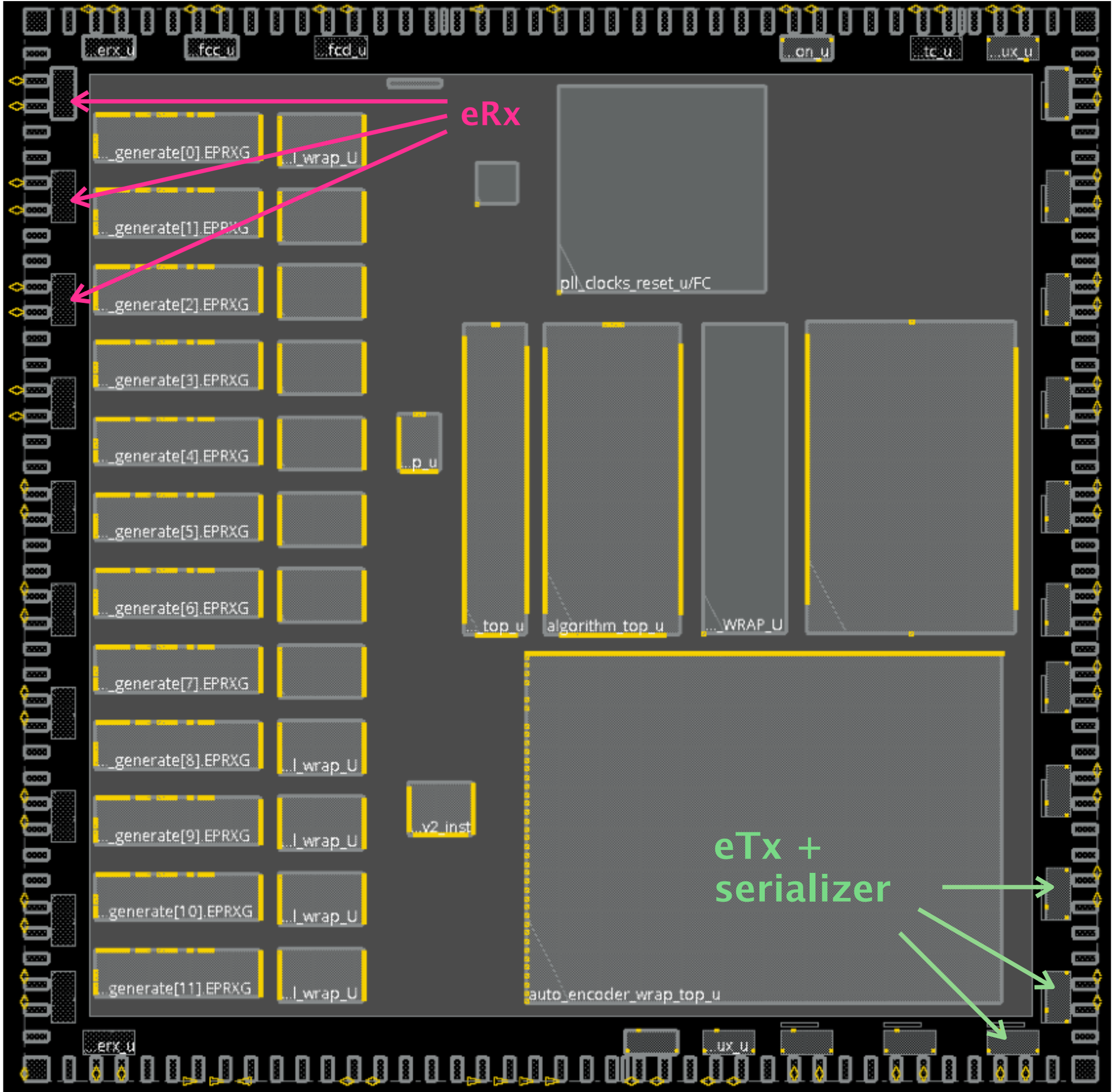
Power, I/O, serializer

Significant effort nearly complete to optimize

- pin out and pads
- power rings
- power domains
- I/O placement and incorporation into top-level RTL
- serializer layout

Remaining work

- serializer analog sim after layout update
- move serializer into core to simplify powering
- final clean up of connections



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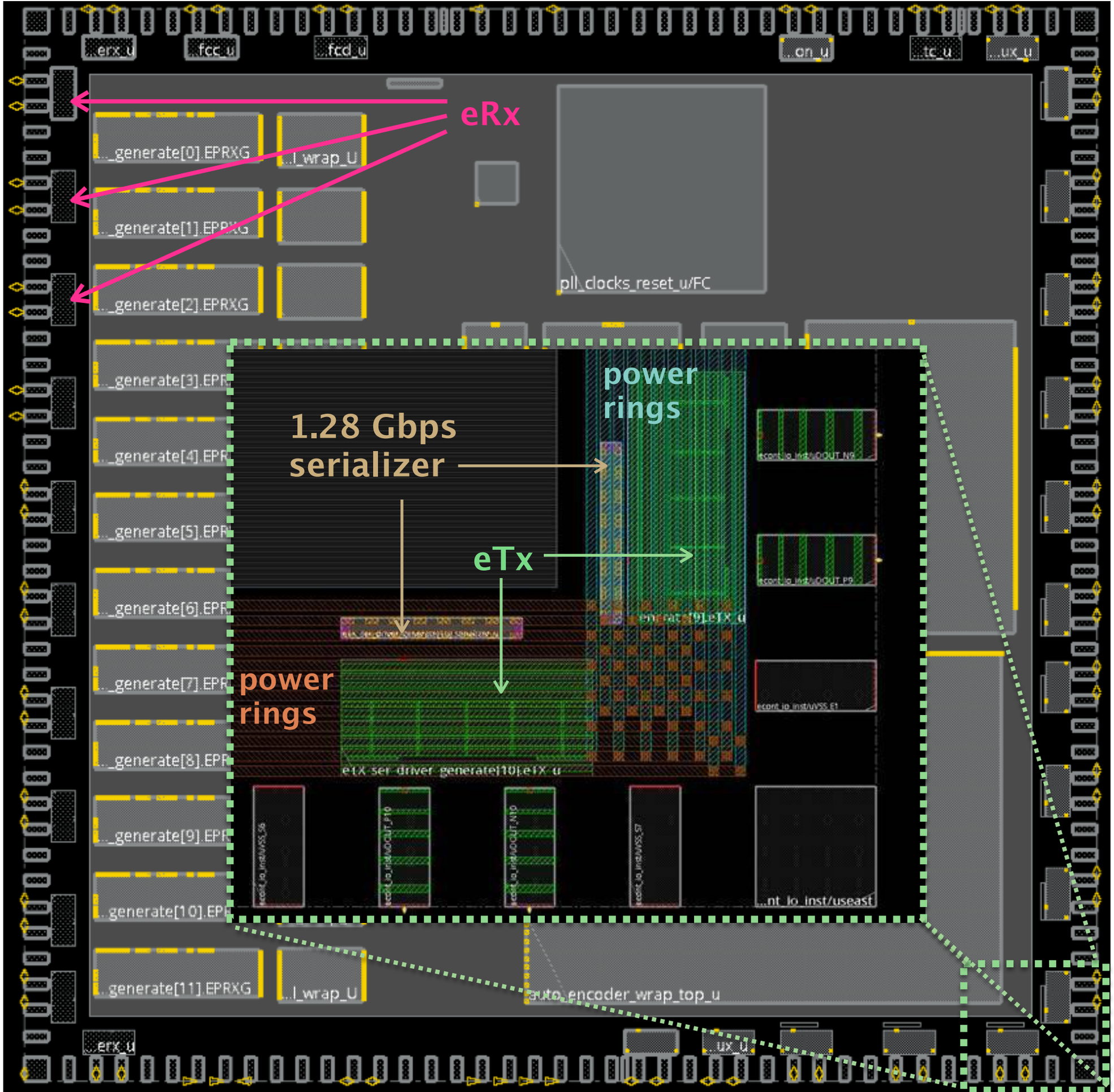


Top-level PnR

Working with top v74

- move to v78 next week when block S+PnR is complete

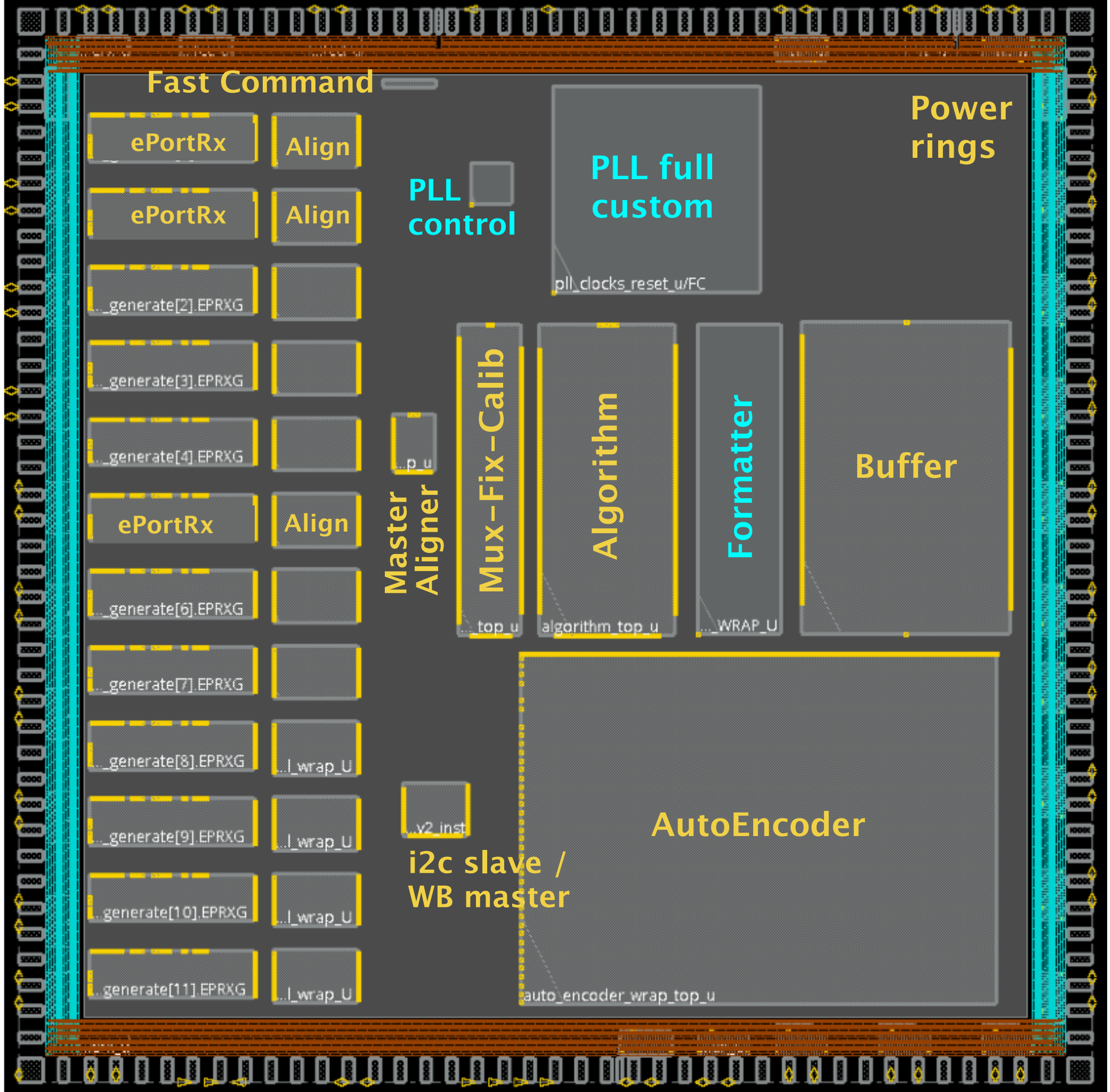
Most blocks pulled in at top level

In progress blocks

- PLL design work on going – abstract ready this week.
- Formatter – RTL adjustment in progress to reduce size.

Buffer PnR was challenging

- 13 eTx, 20 BX max latency
- Bug in tool (confirmed by Cadence) worked around by removing 14th eTx



PLL

- Challenge is moving full custom design from 6-layer lpGBT to 9-layer stack ECON.

lpGBT 6-layers

M6	***inductor + power mesh***
M5	***MIM caps + power mesh***
M4	***routing***
M3	***routing***
M2	***routing***
M1	***routing***

ECON 9-layers

M9	***inductor + power mesh***
M8	***MIM caps + power mesh***
M7	***power mesh***
M6	***power mesh***
M5	***power mesh***
M4	***routing***
M3	***routing***
M2	***routing***
M1	***routing***

- some V4M5V5M6 lpGBT components moved automatically to ECON V7M8V8M9
  - inductor in M9, MIM caps in M4V4M5
  - need to connect down to M4 by hand
- components remaining in V4M5V5M6
  - need adjustment for changing design rules
  - verification of performance for changing resistivity ➔ move to V7M8V8M9 manually, if problem
- add power mesh in M5M6M7 in addition to existing mesh in M5M6
- consultation with others reveals no deficiency with approach
  - Tom Zimmerman (FNAL), Szymon Kulis / Paulo Moreira (CERN)
  - adapting SKILL scripts for 6➔7 layer port from Xavi Llopart (CERN)
  - Cadence consultants
- Top-level PnR can continue based on full PLL abstract

Verification with UVM

- **Block-level UVM** in place for most blocks since early 2020.
  - i2c and hierarchy changes to RTL had significant impact on UVM, but are now ~complete
- **Top-level UVM** first flowing data in early August
  - revealed small bugs in RTL, many of which are already fixed

- UVM framework can **operate in two paradigms**
  1. **input** : random / corner case test vectors ➔ **compare output** to custom UVM-based verilog predictors
  2. **input** : physics / random / corner case test vectors ➔ **compare output** to result of python emulation
  - Paradigm 2 is simpler to implement and **allows efficient use of physicist effort**

- **Random test vector example**: compare RTL output to emulator output:
  - observe **difference** in last frame with non-IDLE data for certain values
  - investigation shows difference is in zero padding but RTL is OK : difference occurs only at block-level b/c zero padding modified in subsequent step.

Python emulation output

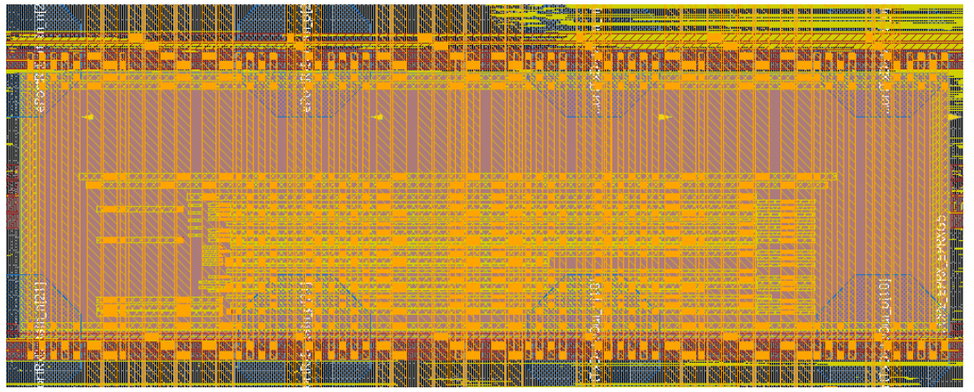
	FRAMEQ_11	FRAMEQ_12	FRAMEQ_13	FRAMEQ_14	FRAMEQ_15	FRAMEQ_16	FRAMEQ_17
0	15656	**41344**	43023	43023	43023	43023	43023
1	35808	27819	630	44514	**17528**	18447	18447
2	9043	62165	**45056**	32783	32783	32783	32783
3	48546	4810	16371	**38656**	34831	34831	34831
4	14938	22666	53126	51358	**19888**	51215	51215

UVM RTL output

	FRAMEQ_11	FRAMEQ_12	FRAMEQ_13	FRAMEQ_14	FRAMEQ_15	FRAMEQ_16	FRAMEQ_17
0	15656	**41349**	43023	43023	43023	43023	43023
1	35808	27819	630	44514	**17528**	18447	18447
2	9043	62165	**45114**	32783	32783	32783	32783
3	48546	4810	16371	**38720**	34831	34831	34831
4	14938	22666	53126	51358	**19895**	51215	51215

Other topics

- **Updated ePortRxGroupTMR IP** received on 16-July-2020
  - incorporated into ECON-T
  - should maintain 1.28 Gbps performance @ 200 Mrad
  - new power distribution verified with Voltus



- **Cadence consultants**
  - Fermilab PO open since early August
  - Cadence will perform Voltus simulation when design reaches appropriate point
  - Also discussing assistance with PLL