Monolithic Active Pixel Sensors for High Performance Tracking

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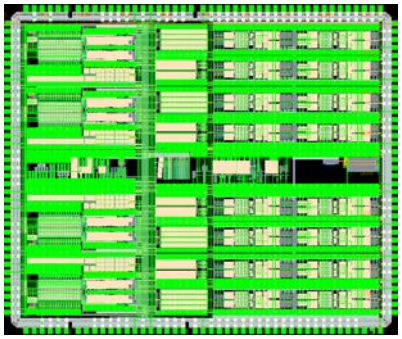
Technology for monolithic tracking and timing devices

BROOKHAVEN NATIONAL LABORATORY

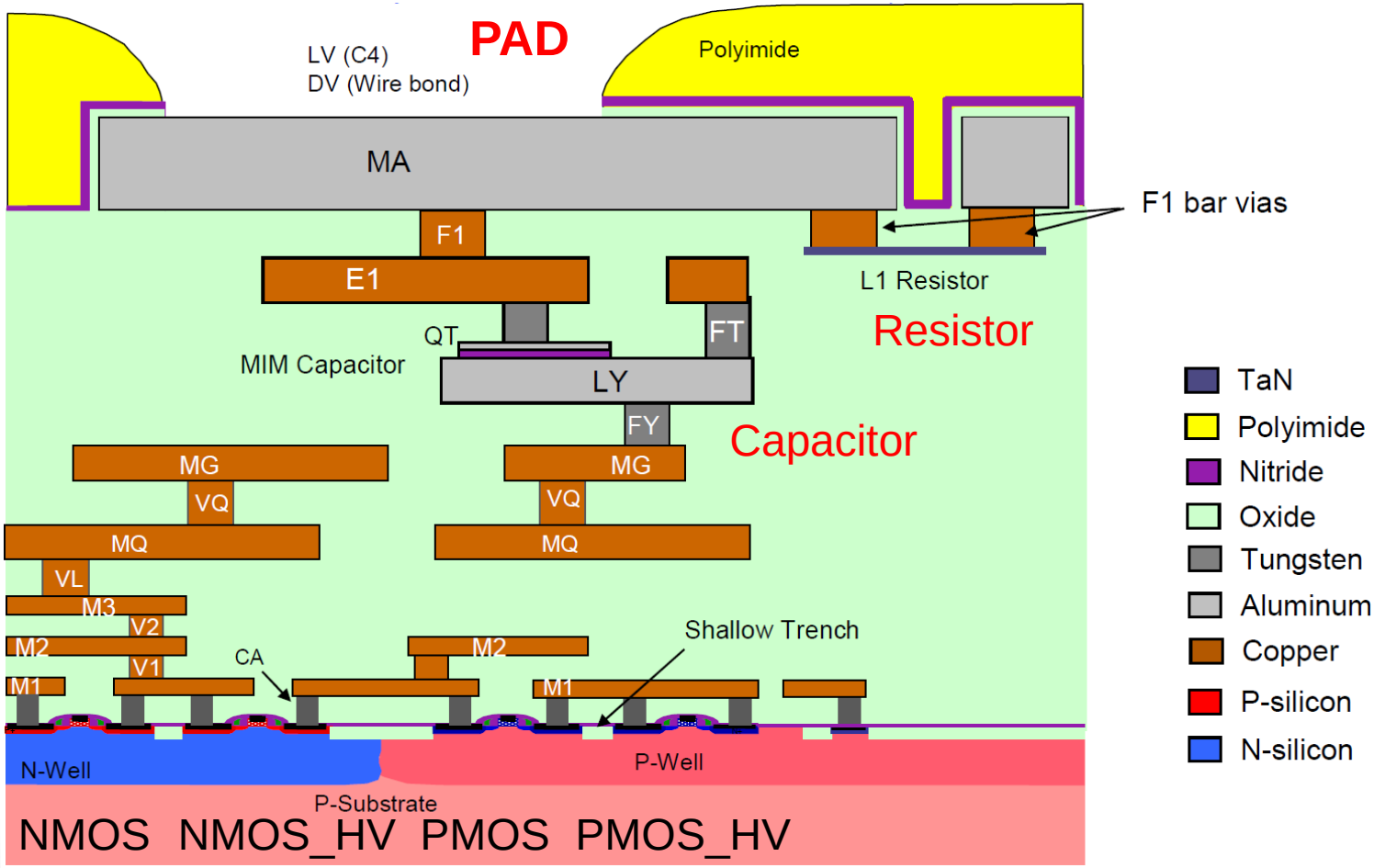
U.S. DEPARTMENT OF ENERGY

Typical bulk CMOS process



Q: What is inside of an integrated circuit?

A: active and passive devices and interconnects

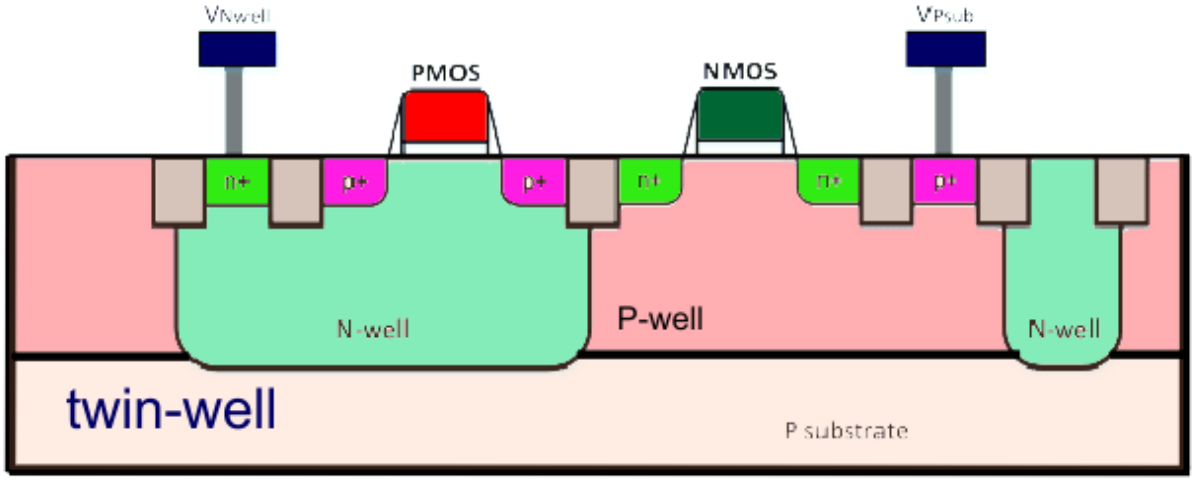


Cross-section of layers in 130 nm bulk CMOS mixed-mode (analog-digital) integrated circuit

Typical bulk CMOS process

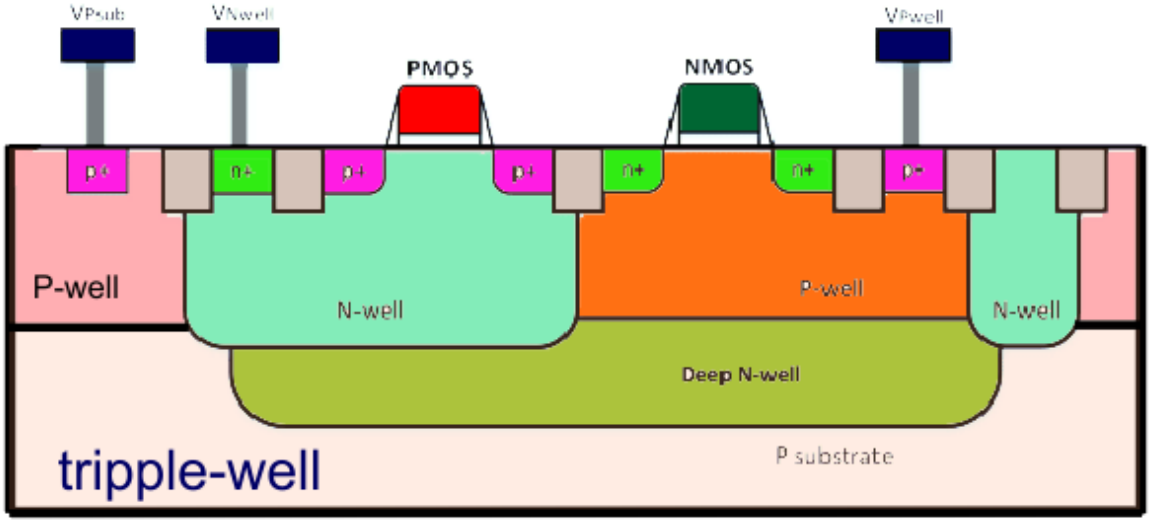
Q: How transistors are built and how the are isolated?

A: transistors “sit” in wells and wells are implanted in substrate; substrate is typically p-type



Twin-well:

nMOSFETs share common substrate (pwell)



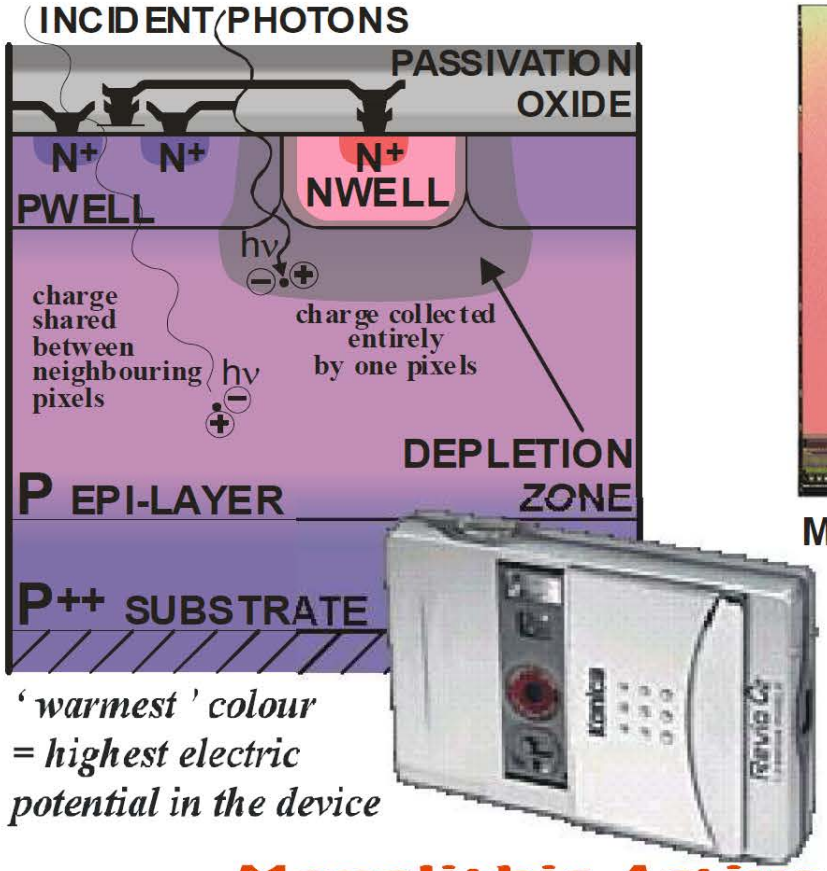
Tripple-well:

nMOSFET do not share substrate between them (extra pwell inside nwell-deep_nwell)

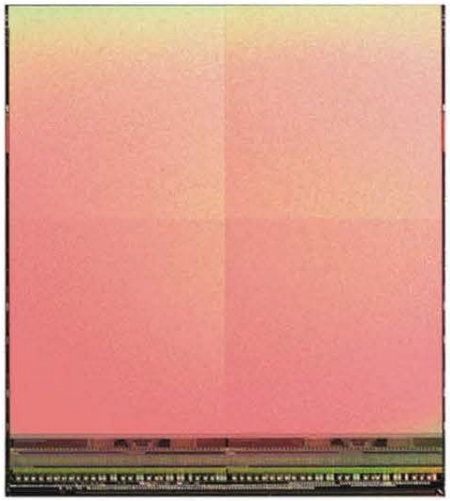
Implanted wells create diodes with other doped areas, so these structures can act as sensors

MAPS in 2000+

From digital photography

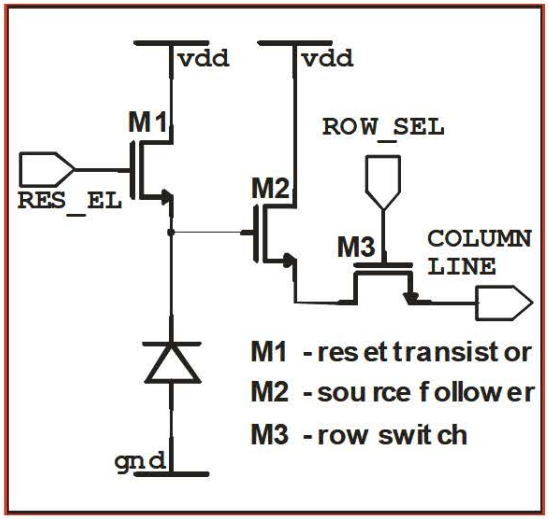


'warmest' colour = highest electric potential in the device



MIMOSA V 1×10^6 pixels micro-photograph

classical 3T pixel schematics



to charged particle detection

Monolithic Active Pixel Sensors (MAPS)

advantages:

- decoupled charge sensing and signal transfer (compared with CCDs)
- small pitch (high tracking precision),
- low amount of material,
- fast readout,
- moderate price, SoC, etc.

MAPS in 2000+ =>PXL MAPS sensor

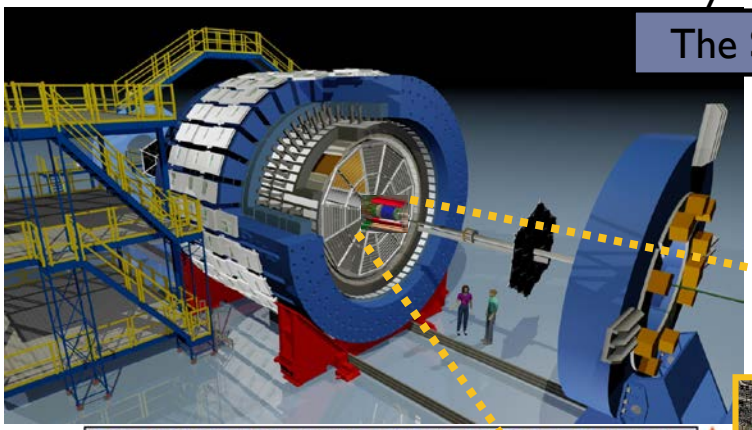
- *This early MAPS made to STAR HFT: Ultimate-2:* 3rd rev. sensor for PXL by PICSEL of IPHC, Strasbourg
- AMS OPTO 0.35 process
- Binary readout of hit pixels
- Increased resistivity p-epi layer
  - Reduced charge collection time
  - Improved radiation hardness
- S/N ~ 30
- MIP Signal ~ 1000 e-
- 185.6 µs integration time
- ~170 mW/cm² power

Rolling-shutter readout

1. A row is selected
2. For each column, a pixel is connected to discriminator
3. Discriminator detects possible hit
4. Move to next row

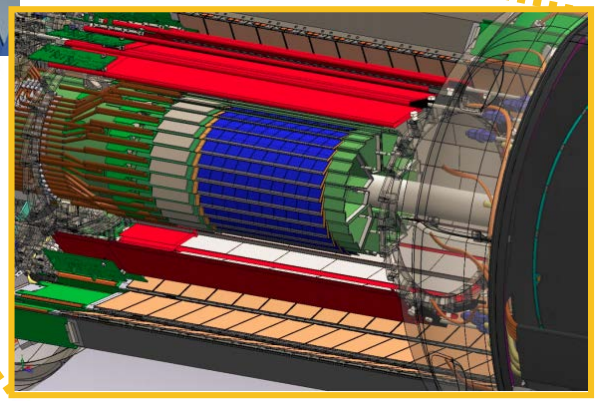
Pixel matrix

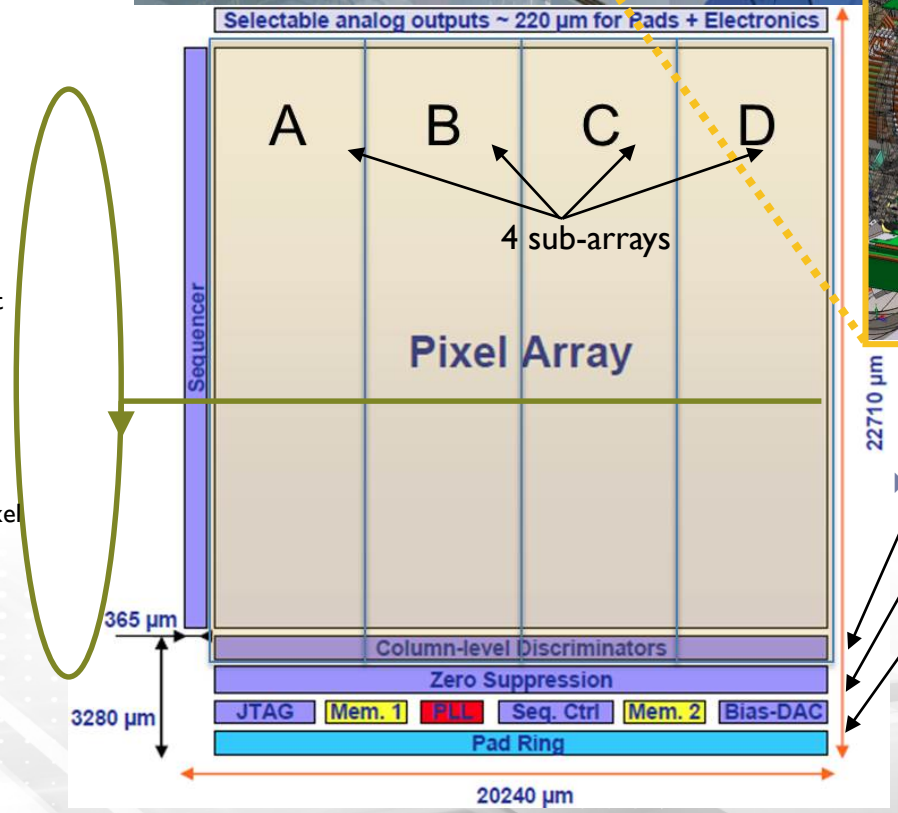
- 20.7 µm x 20.7 µm pixels
- 928 rows x 960 columns = ~1M pixel
- In-pixel amplifier
- In- pixel CDS



HFT – Heavy Flavor Tracker

- SSD – Silicon Strip Detector
- IST – Intermediate Silicon Tracker
- PXL – Pixel Detector

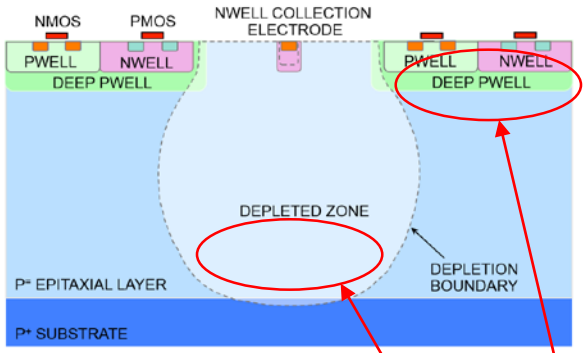




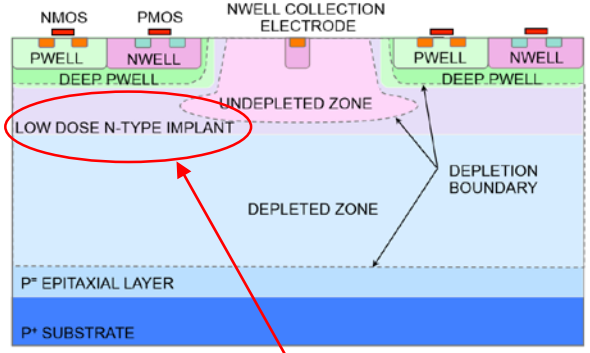
Digital section

- End-of-column discriminators
- Zero suppression (up to 9 hits/row)
- Ping-pong memory frame readout (~1500 W)
- 2 LVDS data outputs @ 160 MHz

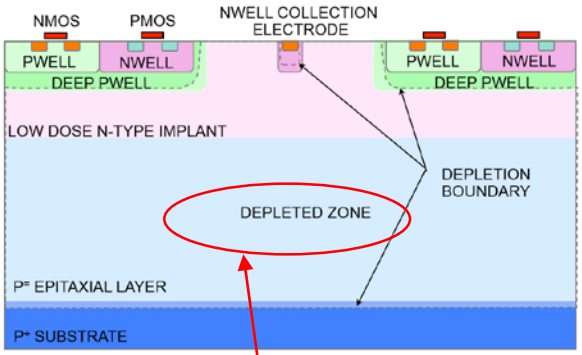
Evolution of MAPS



Standard, not fully depleted



Not fully depleted at low reverse bias



Depletion at higher reverse bias

Q: what features help operating as good detector?

A: several…
- full depletion of sensing volume
- uniform Efield in sensitive volume
- smallest achievable capacitance in sensitive node

added pwell (does not isolate nMOSFETs)

increased resistivity (typically: 10Ωcm Increased to to ~1kΩcm)

added uniform n-implant to:
- vertical Efield under wells
- no extra capacitance if depleted
- nevertheless no lateral E field

applied stronger voltage for more depletion, but watch out breakdowns

Foundry accepted process additions to TJ 180nm and good results were obtained

https://dx.doi.org/10.1016/j.nima.2017.07.046

(PWELL + HR)=ITS

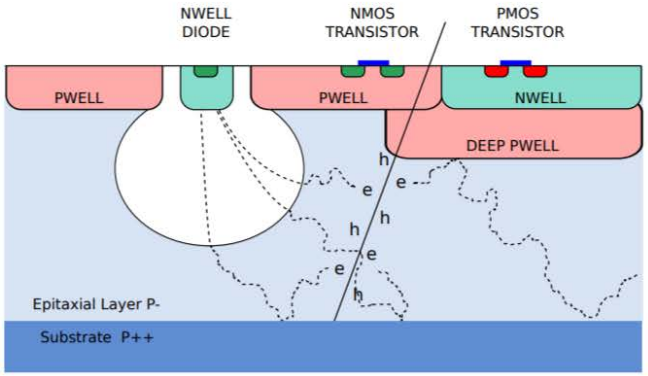
A Large Ion Collider Experiment

ALICE

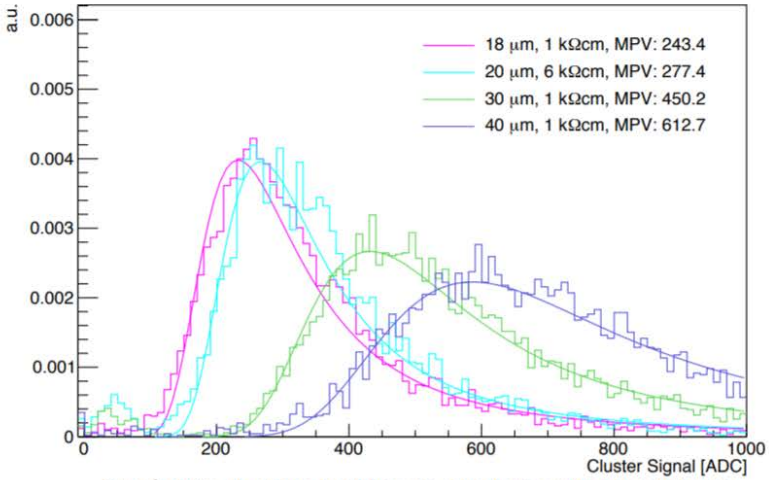
ALICE ITS pixel technology

MAPS produced in CMOS 0.18 µm process by TowerJazz

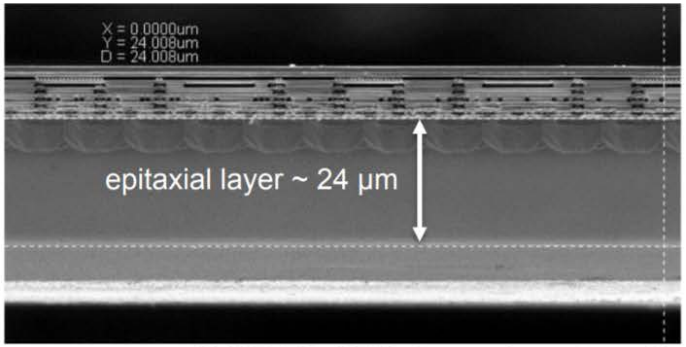
- Deep p-well allows to have PMOS and NMOS inside the pixel cell
- High resistivity epi layer
- Chip size: 15 mm x 30 mm, thinned to 50 µm
- Pixel pitch ~ 30 µm
- Spatial resolution < 5 µm



Cluster Signal (5x5), Explorer-1, A1-E2, Sector 5

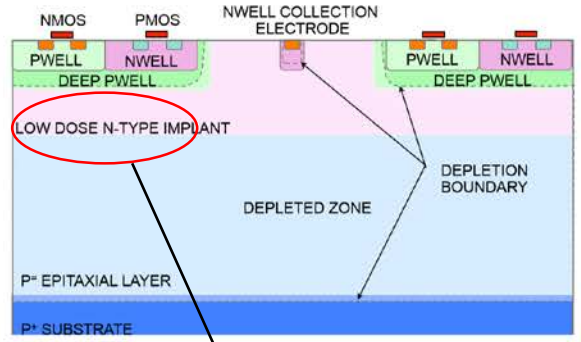


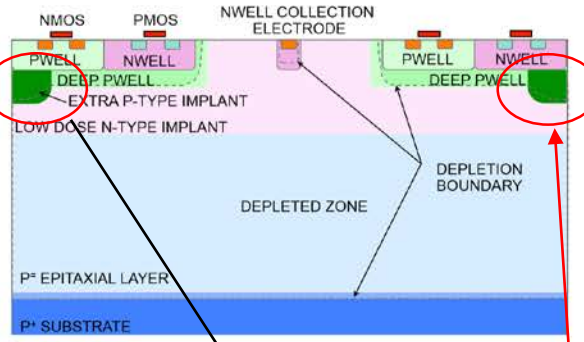
3.2 GeV/c electron test beam, pixel size 20 µm x 20 µm
J. Van Hoorne, PoS (TIPP2014) 125

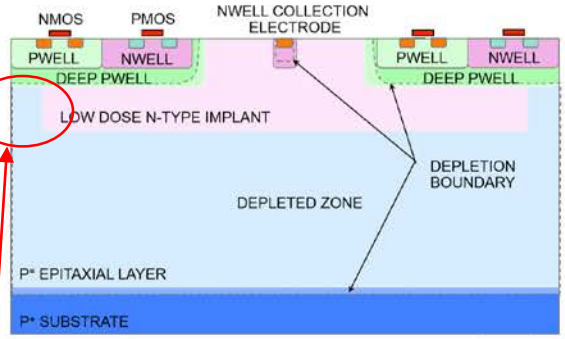


ALICE ITS, SEM picture of prototype chip

Further evolution of MAPS







charge stacks here

charge pushed sideways

Extra pwell implant or break in blanket deep implant creates later push for carriers

Q: what is not enough?

A: charge drifting upwards get stack under wells with electronics; there is no lateral push to collection nwell

improvement of collection speed, CCE => radiation hardness

Further improvements accepted to TJ 180nm and good results were obtained but 180nm has density limitation => 10 μm pixels difficult

E. Schioppa, et al, VCI 2019
M.Munker, et al. PIXEL2018

Use of process features

- Adding features to existing volume production CMOS process is extremely difficult and only possible if foundry sees economical benefits:
  - Even using wafers from outside of qualified supplier is out of question,
  - Adding or modified doping layers is even more difficult.

- MAPS have been detectors demonstrated assuitable for tracking in some limited areas, but with TJ 180 / TJ 65 for ALICE ITS MAPS gain 100x in performance (bandwidth, TID, NIEL, processing, timing).

- MAPS combined combine diode as sensitive detection volume.
- Other structures, e.g. avalanche charge multiplying devices (DC / AC-LGAD) can be explored should process features available (implants) allow construction of such a device – needs to be investigated.

MAPS technology LOI

Snowmass 2021 Letter of Interest: Monolithic Active Pixel Sensors for High Performance Tracking

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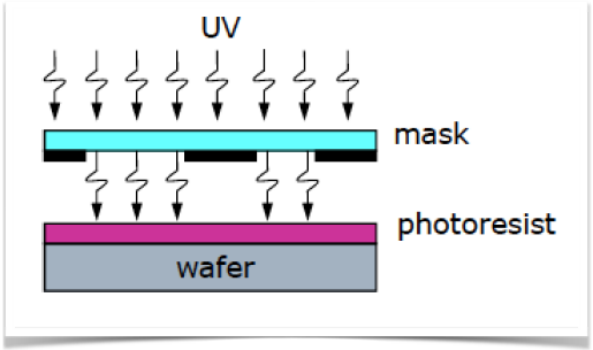
Thematic Areas: IF7: Electronics/ASICs
IF3: Solid State Detectors and Tracking

Monolithic Active Pixel Sensors (MAPS) detectors have been postulated for charged particle tracking in the early 2000s [1] stimulated by a growing interest at that time in developing lepton colliders with an aim on the International Linear Collider (ILC). The MAPS detectors can be built rather inexpensively, even in large sizes of megapixel arrays, thinned as needed, offer high blooming threshold, individual pixel readout, radiation hardness, while operating at high speed with low power consumption, from a single and low voltage supply. Older-generation MAPS, such as those postulated early for the ILC and practically used in the Heavy Flavor Tracker (HFT) at STAR [2] are built on a low-resistivity substrate, forming the active sensitive volume (ASV) and in-situ signal/data processing is limited. This limitation results from the technological restriction of fabrication processes used for these early MAPS detectors. Simply, a lack of nested n-inside-p doping wells disallows complementary transistors in in-pixel processing circuit networks.Therefore, these early MAPS detectors, although able to offer high granularity and small material budget, are not suited for implementation of the systems requiring advanced timing, fast readout and resistance to radiation needed in the LHC experiments or for Electron Ion Collider.

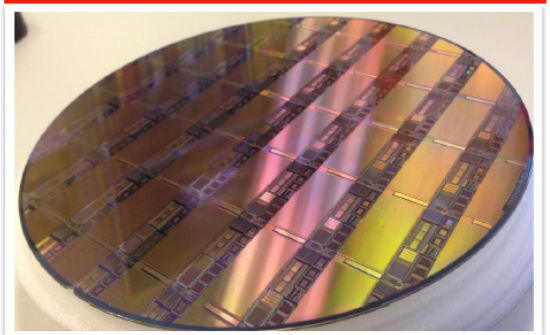
TJ 65 for tracking

- TJ 180nm process used with modifications – fabricated in Israel
  - deep-wells, EPI ρ=~500Ωcm (HR option), EPI thickness limited to 8-10 μm,
- New efforts TJ 65nm process – fabricated in Japan (joint venture w. Panasonic
- Two main technology flavors(both available with HR epi<10 μm thick):
  - Imaging technology (ISC) and high-density CMOS (logic, rf…),
- Switch to TowerJazz 65 nm CMOS process (ITS2/ALPIDE: TowerJazz 180 nm)
  - needed mainly because of larger wafers: ⌀=300 mm (180 nm process only available on ⌀=200 mm wafers)
- Stitching, i.e. producing chips as big as the wafer
- More details about the sensor development in the ***next talk by Iain Sedgwick***

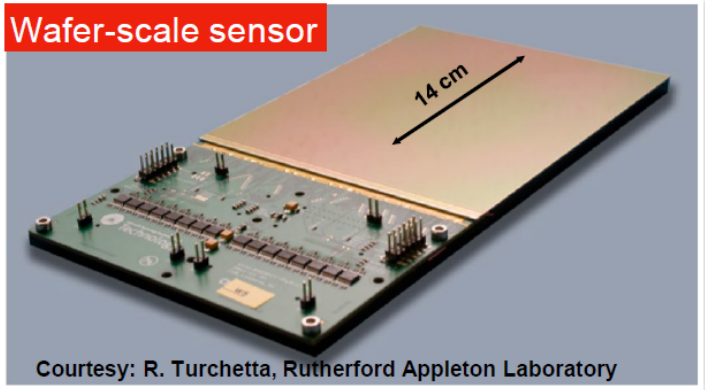
Principle of photolithography



200 mm ALPIDE prototype wafer



Wafer-scale sensor



TJ 65 for tracking
EOI – EIC Silicon Consortium

Please indicate the name of the contact person for this submission:

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Please indicate all institutions collectively involved in this submission of interest:

LBNL, BNL Instrumentation Division, University of Birmingham, Rutheford Appleton Laboratory, CCNU (Wuhan), JLAB.
We expect others to be joining soon.

Please indicate the items of interest for potential equipment cooperation:

The goal of this consortium is to develop a MAPS sensor and associated powering, support structures, control and ancillary parts as necessary to produce a detector solution for silicon tracking for the central tracking parts of an EIC detector. The consensus of opinion in the consortium is that the optimum path to realize this goal is to join the ITS3 effort at CERN and work to develop both the proposed ITS3 sensor technology that could be used for the vertexing layers at the EIC, and a very similar sensor optimized for deployment in the outer barrel and disc layers.

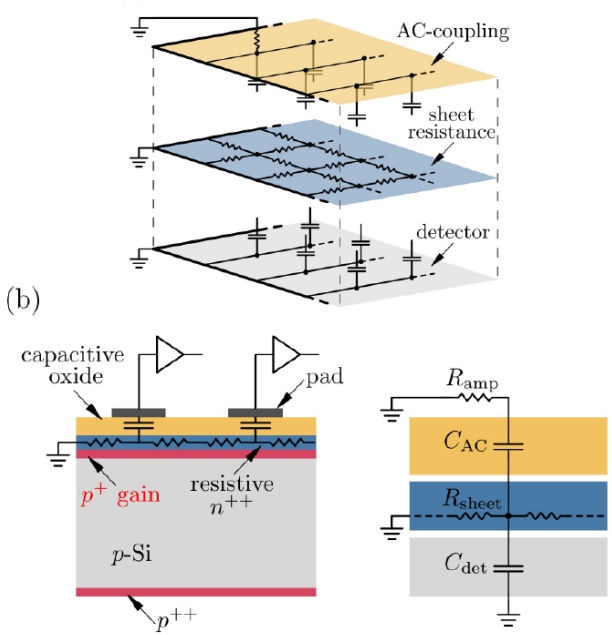
Timing

- **Novel development: AC-coupling allows fine segmentation**
  - ➔ **Time & Space measurements**
  - ➔ **100% fill factor**

Main differences wrt LGADs:

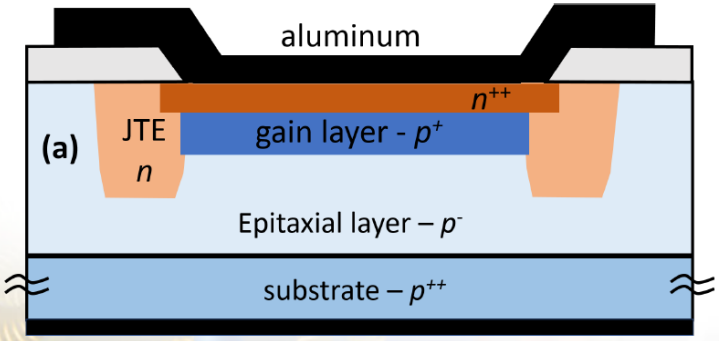
1. one large low-doped / high-ρ n^+ implant running overall the active area, instead of a high-doped low-ρ n^{++}
1. A thin **insulator** over the n^+, where fine-pitch electrodes are placed.

- ➢ Signal is still generated by drift of multiplied holes into the substrate and AC-coupled through dielectric
- ➢ Electrons collect at the resistive n^+ and then slowly flow to ohmic contact at the edge.
- ➢ **100% Fill Factor and fast timing information at a per-pixel level both achieved!!!**

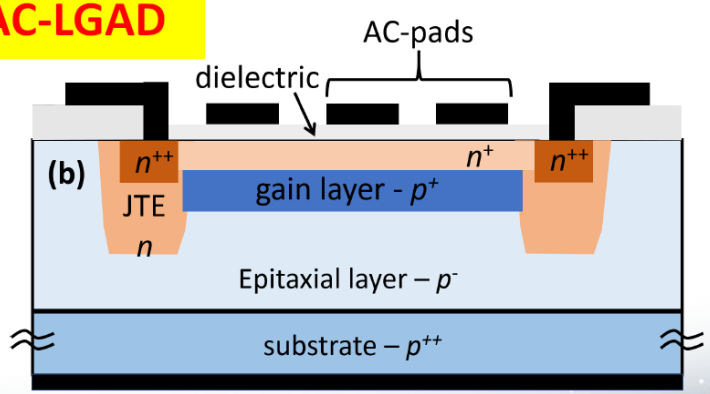


BNL designs:

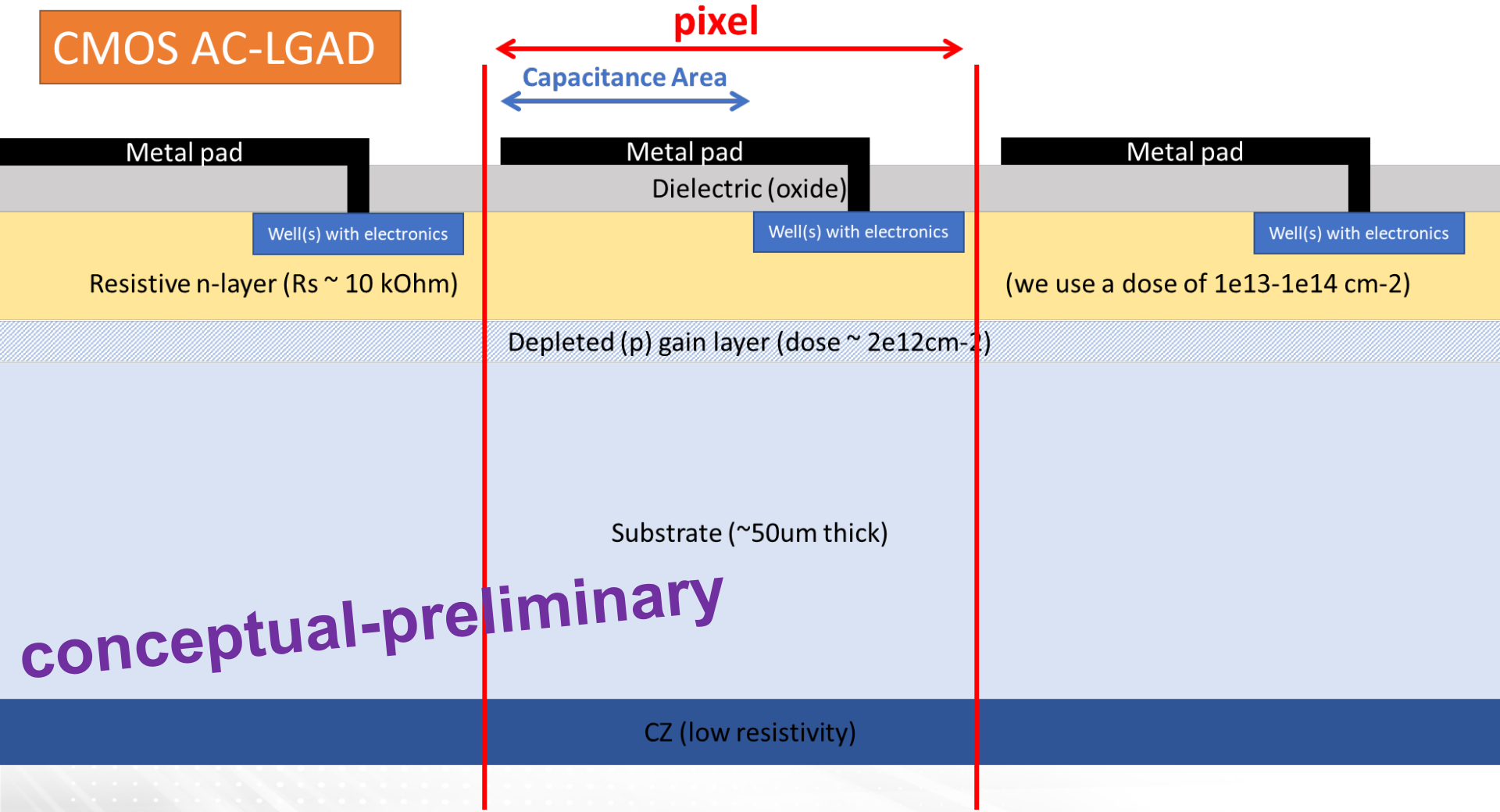
LGAD



AC-LGAD

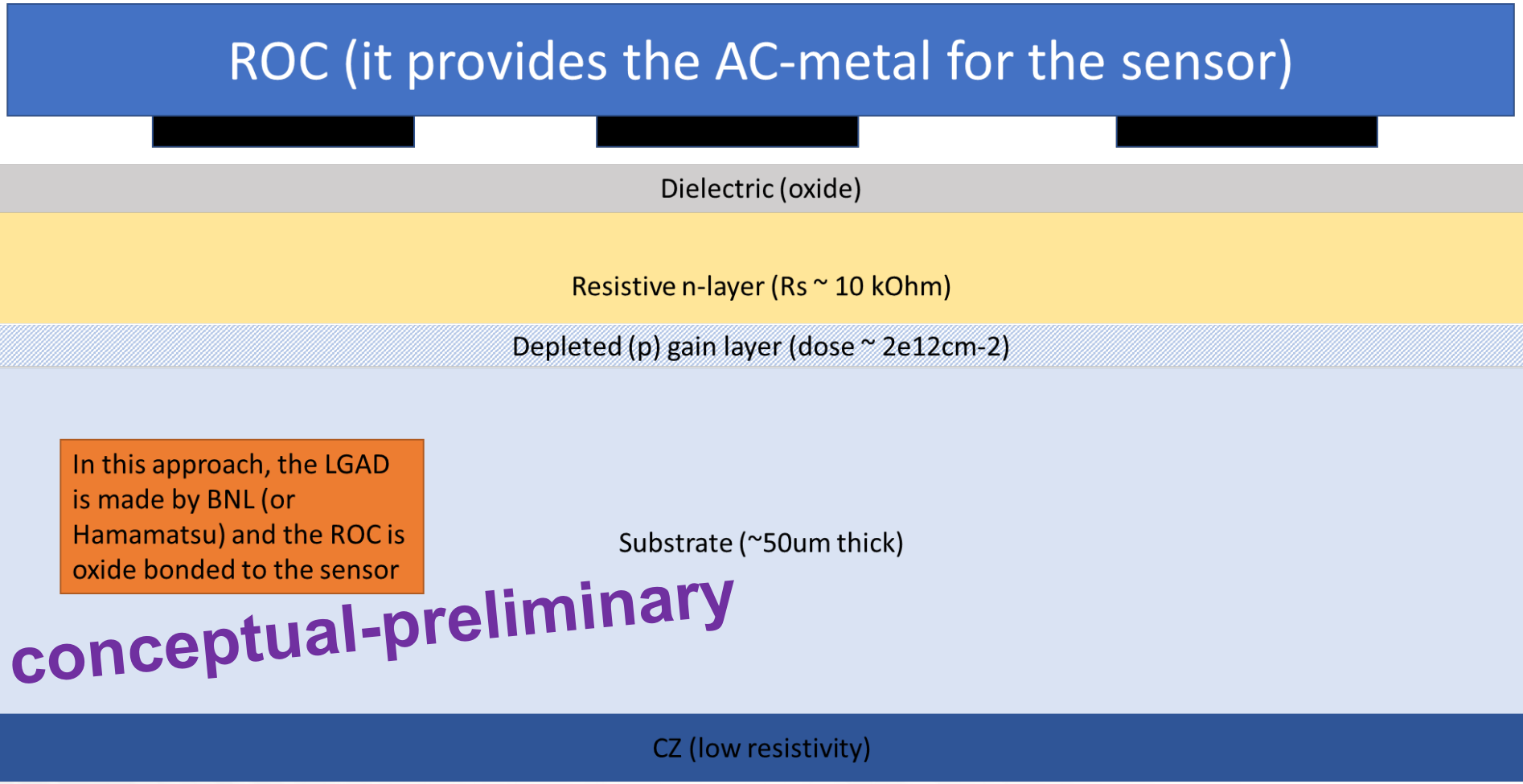


TJ 65 for: monolithic AC LGADs



timing detectors

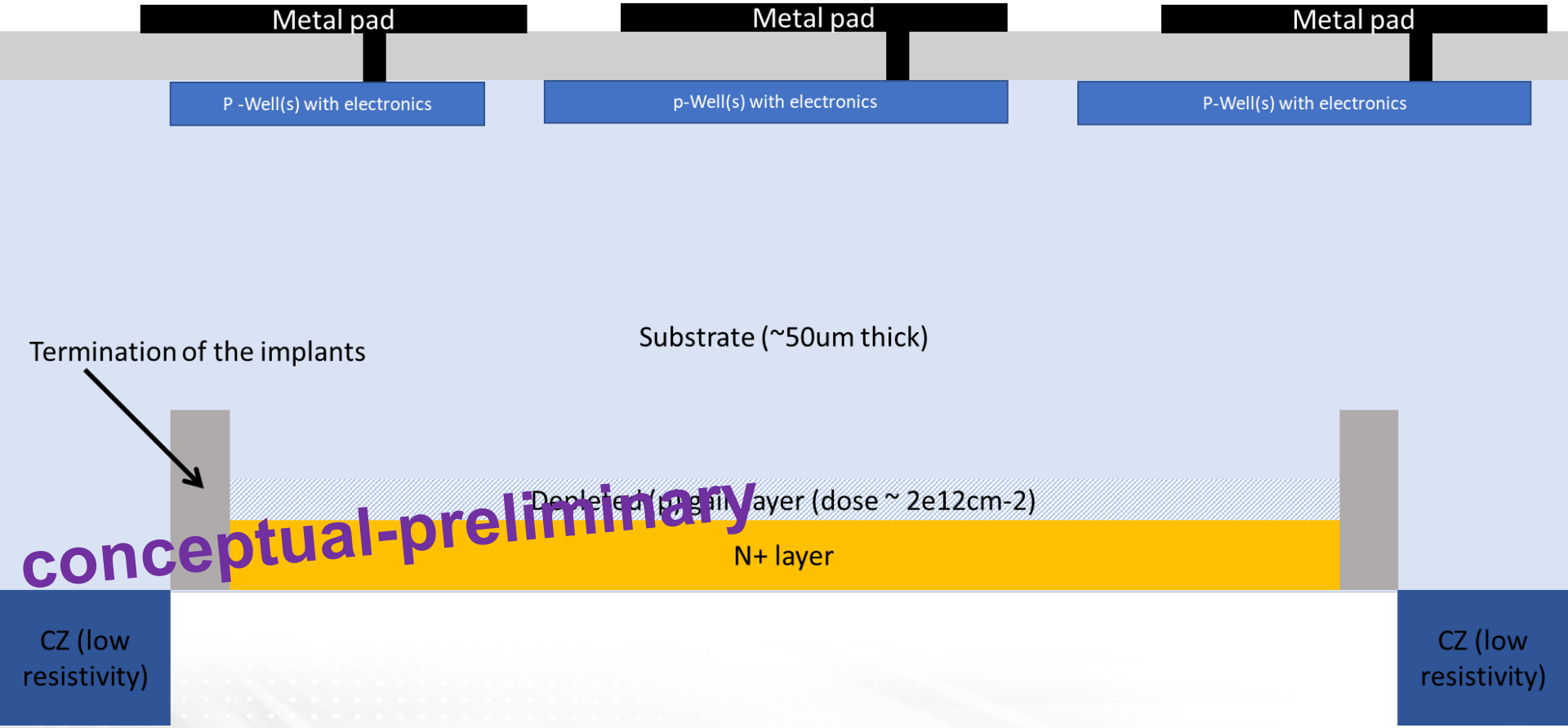
Timing: monolithic AC LGADs



May still combine hybridization

Timing: monolithic AC LGADs

CMOS LGAD



conceptual-preliminary

or double side processing

Conclusions

- MAPS as initially developed in early 2000s showed their limitations,
- Recently, an effort is emerging to develop new generation MAPS in TJ 65 nm CMOS imaging technology

- Improvements for making good monolithic (sensors + readout) has been known, simulated and sometimes demonstrated – inefficient is to get the adaptations to a mainstream CMOS process due to no market for foundries,

- MAPS built in adapted TJ process for ALICE ITS3, CERN Experimental Physics department R&D programme (WP1.2 MAPS)
  and are is technological platform for:
  - EIC tracking (options are under consideration) and pixel for direct detection of electrons and X-ray photons.
  - Timing detectors using built-in gain structures; this is under feasibility consideration if process features are suitable.

bent but functional ALPIDE