DE LA RECHERCHE À L'INDUSTRIE

Round table workshop PIP-II

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DEVELOPMENT

- Development environment: VSCODE
- Source code: GIT (CEA-Saclay repository)
- Issues: GITLAB
- Documentation: Confluence
- EPICS Base and support defined
- Programming rules

NAMING CONVENTION, PLC

- Naming convention is often under estimate but impact on project can be significant
  - Naming software (EPICS) vs cabling
  - Changing variable name in EPICS database is long and not fun
  - Same thing for wiring scheme
  - Naming tool is good. ESS tool is generating communication code for example

- PLC
  - We are working on Siemens product
  - Cryogenic plants can have a lot of variables
    - S7 from PSI for reading
    - Modbus/TCP writing one variable (Boolean)

SARAF PROCESS VARIABLE NAMING

Close to ESS naming
No tool
Rules already used for Spiral2 and IFMIF

Section-Subsection	:	Dis-Device-Index	:	Signal
Sec-Sub(x)	:	**Dis-Dev-Idx**	:	**Signal**
Up to 8 alphabetic characters, upper-case Sec is for the Section. Sub has to be chosen following the context and up to 3 characters.		Up to 15 alphabetic characters Dis: Discipline from 2 to 5 characters Dev: component name of the device, from 2 up to 5 alphabetic characters Idx: device index, 1 to 5 numeric characters. Even if only one of this device is planned, give it index 1.		Up to 20 alphabetic characters. Camel case is used. Should be chosen as short as possible.

Signal = Command//Property
Ex: IMes, UCmd, ThrSet

SARAF CABLING NAMING: RDS USED

mem_Pbs	RDS2	Connector A	Terminal A	Connector B	Terminal B
Turbo pump venting valve control cable	-SL-MBT-RBN1-C1-PSG1-PS1-WG3		-SL-MBT-RBN1-C1-PSG1-PS1-GQ1		-SL-MBT-RBN1-C1-PSG1-PS1-KF1
Pump control cable	-SL-MBT-SVC-PSA4-PSG1-PS1-WG1		-SL-MBT-SVC-PSA4-PSG1-PS1-GQ1		-SL-MBT-SVC-PSA4-PSG1-PS1-KF1
Fan control cable	-SL-MBT-SVC-PSA4-PSG1-PS1-WG2		-SL-MBT-SVC-PSA4-PSG1-PS1-GQ1		-SL-MBT-SVC-PSA4-PSG1-PS1-KF1
Turbo pump venting valve control cable	-SL-MBT-SVC-PSA4-PSG1-PS1-WG3		-SL-MBT-SVC-PSA4-PSG1-PS1-GQ1		-SL-MBT-SVC-PSA4-PSG1-PS1-KF1
Pump control cable	-SL-MBT-SVC-PSA2-PSG1-PS1-WG1		-SL-MBT-SVC-PSA2-PSG1-PS1-GQ1		-SL-MBT-SVC-PSA2-PSG1-PS1-KF1
Fan control cable	-SL-MBT-SVC-PSA2-PSG1-PS1-WG2		-SL-MBT-SVC-PSA2-PSG1-PS1-GQ1		-SL-MBT-SVC-PSA2-PSG1-PS1-KF1
Turbo pump venting valve control cable	-SL-MBT-SVC-PSA2-PSG1-PS1-WG3		-SL-MBT-SVC-PSA2-PSG1-PS1-GQ1		-SL-MBT-SVC-PSA2-PSG1-PS1-KF1
Pump control cable	-SL-MBT-RBN3-C1-PSG1-PS1-WG1		-SL-MBT-RBN3-C1-PSG1-PS1-GQ1		-SL-MBT-RBN3-C1-PSG1-PS1-KF1
Fan control cable	-SL-MBT-RBN3-C1-PSG1-PS1-WG2		-SL-MBT-RBN3-C1-PSG1-PS1-GQ1		-SL-MBT-RBN3-C1-PSG1-PS1-KF1
Turbo pump venting valve control cable	-SL-MBT-RBN3-C1-PSG1-PS1-WG3		-SL-MBT-RBN3-C1-PSG1-PS1-GQ1		-SL-MBT-RBN3-C1-PSG1-PS1-KF1
Pump control cable	-SL-MBT-RBN2-C1-PSG1-PS1-WG1		-SL-MBT-RBN2-C1-PSG1-PS1-GQ1		-SL-MBT-RBN2-C1-PSG1-PS1-KF1
Fan control cable	-SL-MBT-RBN2-C1-PSG1-PS1-WG2		-SL-MBT-RBN2-C1-PSG1-PS1-GQ1		-SL-MBT-RBN2-C1-PSG1-PS1-KF1
Turbo pump venting valve control cable	-SL-MBT-RBN2-C1-PSG1-PS1-WG3		-SL-MBT-RBN2-C1-PSG1-PS1-GQ1		-SL-MBT-RBN2-C1-PSG1-PS1-KF1

-SL-MBT-RBN3-C1-PSG1-PS1-WG1
-SL-MBT-RBN3-C1-PSG1-PS1-WG2
-SL-MBT-RBN3-C1-PSG1-PS1-WG3
-SL-MBT-RBN2-C1-PSG1-PS1-WG1
-SL-MBT-RBN2-C1-PSG1-PS1-WG2
-SL-MBT-RBN2-C1-PSG1-PS1-WG3

Only the first 2 fields are identical to the EPICS PV naming

NETWORK, TEST

- Separating network
  - PLC (Profinet)
  - PLC supervision (IOC)
  - Device (Power supply, …)
  - Timing
  - EPICS (CA or PVA)

- Test : automatic test with WeTest based on yaml description

MAIN CONTROL SYSTEM APPLICATIONS

- Applications are in Java based solution

- GUI: CSS, Phoebus in progress. Phoebus is much more easier if you need to add new functionalities
  - CSS based on Eclipse RCP makes plugin development more complex
  - Phoebus not deployed for the moment

- Archive: Archive Appliance but for small accelerator
  - Trouble are mainly administration ones with var/messages full or disk out of order
  - Or IOC not on time (NTP issues)

- Alarm: BEAST, Kafka solution in progress with development on dayshift

REQUIREMENTS

- Need **naming convention** really early for detailed specification
- In the project schedule, we have requirements for IOC **late** because instrumentation (vacuum, cryogenic, diagnostic,…) has to make choices first
- Have instrumentation involving **less control work** (TCP vs serial,…) from the instrumentation team, especially when serial products are less expensive
- **Outsourcing** the code development is challenging in term of **maintenance**
  - Define programming rules
  - Define tests

MTCA

- New technology so the products are not always completely operational
- Mastering compilation chains involves specific skills, not as easy as TIA Portal, LabVIEW,…
- Very modular backplane and so more time to configure and understand why it is not working (power supply, data bus, timing)
  - Ex: Timing card will be installed at the same slot
- AMC can have 2 FMC, modular but needs time for developing code, so we are freezing configuration

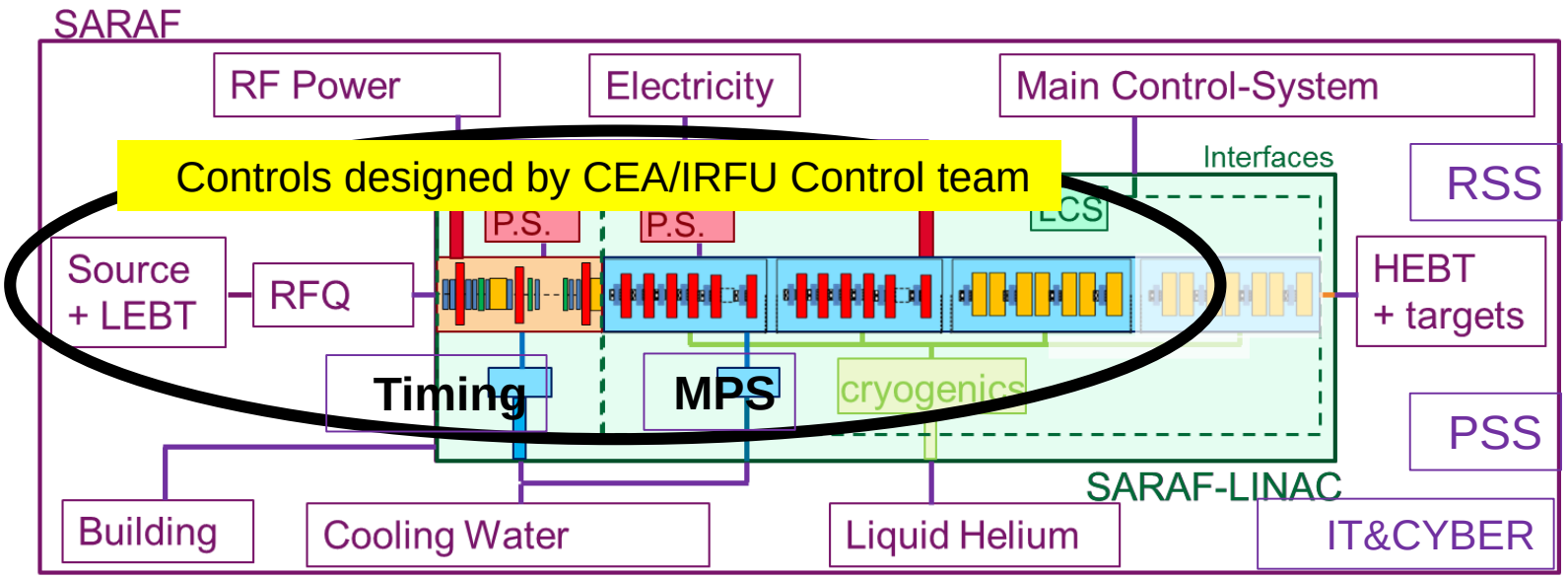
LABVIEW EPICS

- No pure LabVIEW EPICS solution
  - Driver EPICS from NI is a Channel Access server but not an IOC (no alarm)
  - One interesting solution for LabVIEW developer based on Shared Variables is NetShrVar but fast data? https://github.com/ISISComputingGroup/EPICS-NetShrVar

- Several solutions but depend on the target (PC, cRIO)
  - CALab (version 1.7 2020, compatible EPICSv7): https://www.helmholtz-berlin.de/zentrum/locations/it/software/exsteuer/calab/index_en.html
  - LabIOC (Observatory Science): http://observatorysciences.co.uk/labview.php
  - lvPortDriver (Los Alamos): https://github.com/lanl/lvPortDriver
  - Nheengatu (FPGA only): https://github.com/lnls-sol/project-nheengatu

- Be careful of the timestamp
- Slow : Modbus/TCP

SARAF LINAC IN BRIEF

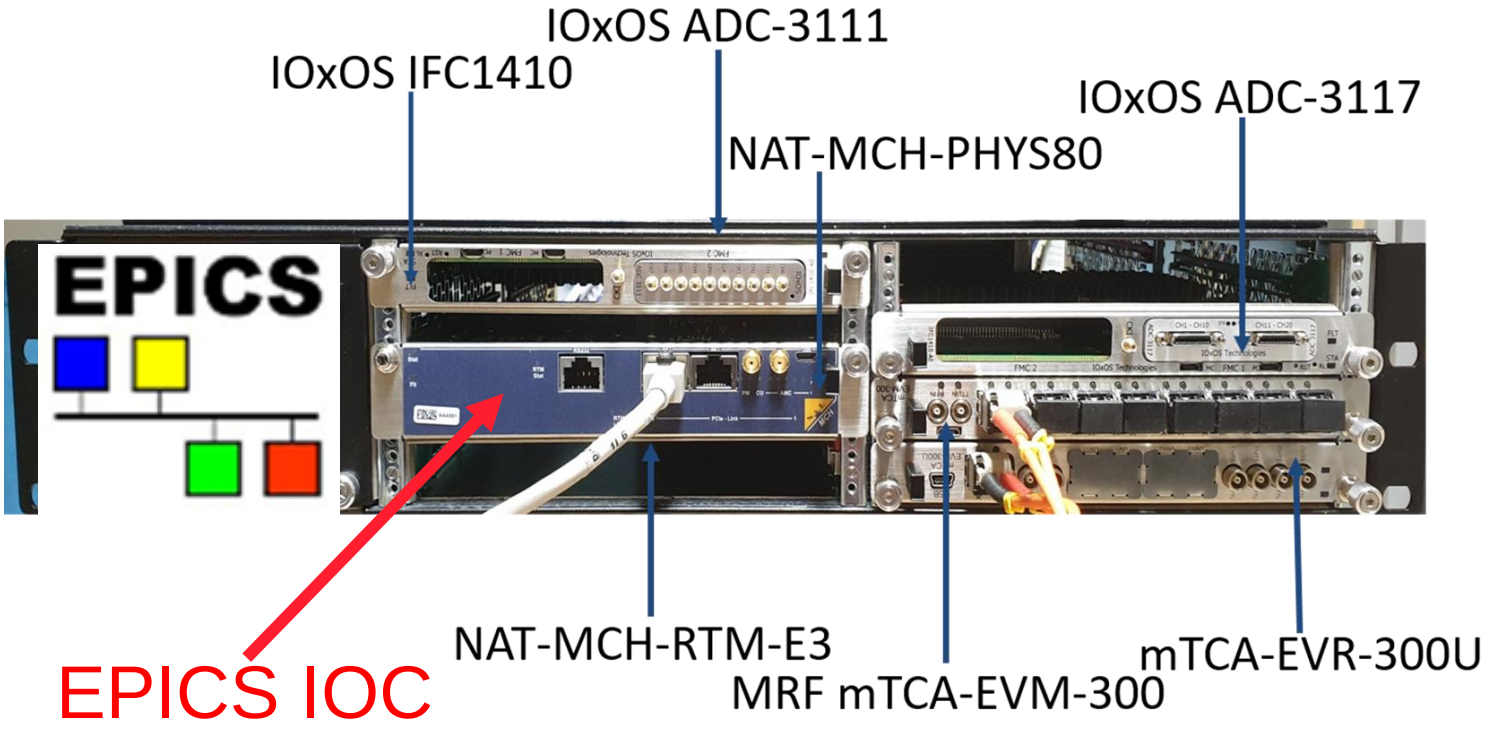


- CEA takes over controls of:
  - Source & LEBT & RFQ already existing and control delivered in Q2 2020
  - MEBT delivered in Q3 2020 with its control
  - 4 Cryomodules CM1, CM2, CM3 and CM4
  - Each Cryomodule CM2-4 includes 7 cavities, CM1: 6 cavities
    - To be delivered in 2022
  - Diagnostics: BPMs, nBLMs, Harps, Faraday cups, ACCTs, …

MTCA.4 STANDARDIZED PLATFORM IN BRIEF

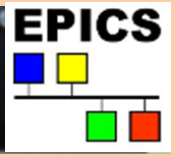
- Migration to MTCA.4 for SARAF control system in summer 2018
- CEA team updated and standardized the IRFU EPICS Environment with MTCA.4 solutions based on:
  - **NAT solution NAT-MCH-RTM-COMexE3 (CPU) & MCH-PHYS80 (MCH)**
  - **IOxOS boards** (ADC-3117, ADC-3111, DIO-3118)
  - **MRF** boards
  - ESS ICS EPICS drivers in 2018
- In 2019 we developed our own CEA EPICS drivers for IOxOS boards
- **We are using EPICS 3.15.5 & ASYN R4.33**
- Our purpose: use COTS as much as possible

STANDARDIZED PLATFORM IN A NATIVE-R2 CRATE

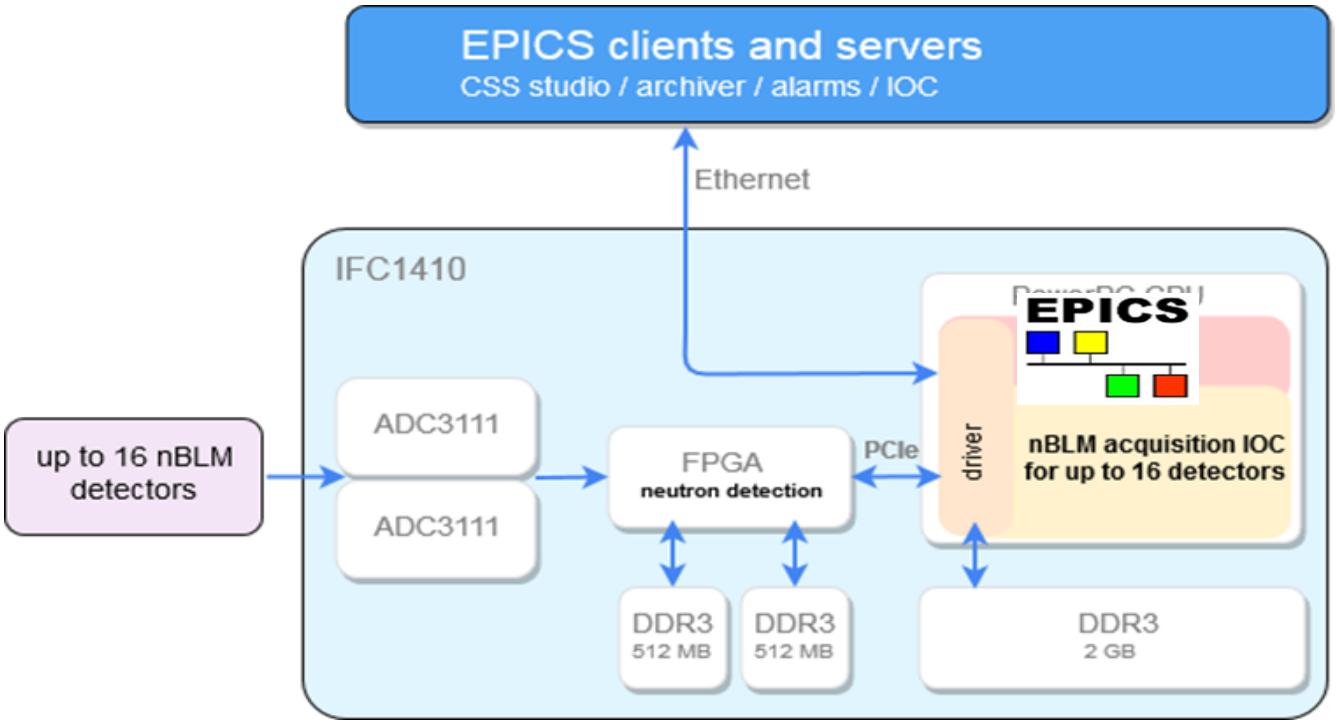


NAT NATIVE-R2 crate

STANDARDIZED COTS SOLUTIONS

Requirements	Sampling/monitoring	COTS solutions
MTCA.4 MCH & CPU  		NAT-MCH-PHYS80 (MCH)& NAT-MCH-RTM-COMex-E3 (CPU)
Fast acquisition  Sem—fast acq Digital I/O -TTL	5 MS/s up to 250 MS/s 50 KS/s up to 5 MS/s	CPU carrier **IOxOS IFC 1410** & IOxOS FMC ADC-3111 FMC ADC-3117 FMC DIO-3118 
Remote I/Os control LAN or serial	100 ms up to 1s	Industrial PC & Beckhoff (Modbus/TCP) 
Process for vacuum and cryogenics & Interlock	100 ms up to 1s	Siemens 1500 PLC & I/O boards Profinet/ Profibus Fieldbuses & remote I/Os 
Timing System		MRF mTCA-EVM-300, mTCA-EVR-300U

EXAMPLE: SARAF NEUTRON BEAM LOSS MONITOR



- The **IOxOS IFC1410 board** provides an FPGA and a PPC processor running Linux
- The neutron detection is managed in this FPGA
- The IOC (running in the PPC) manages data from the FPGA through PCIe
- The IOC analyses and takes over the formatting of FPGA data
- The IOC makes calculations and provides data through Channel Access
- The IOC also provides acquisition files on demand

SARAF: LLRF & BPMS OUTSOURCED

LLRF & BPM boards outsourced by Seven Solutions
System of Chip architecture
Boards will be delivered in January 2021

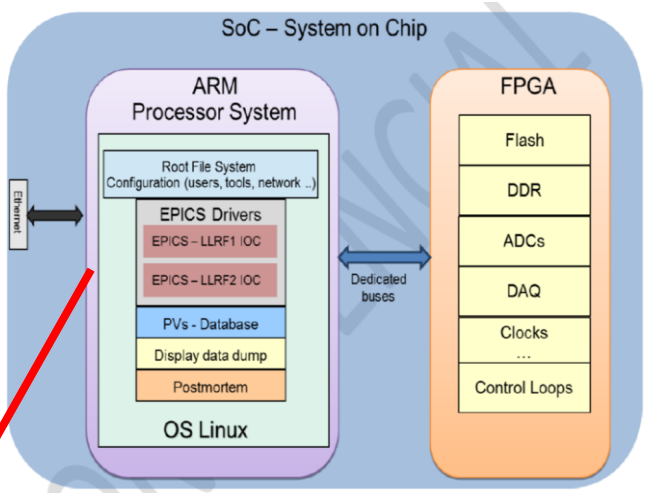
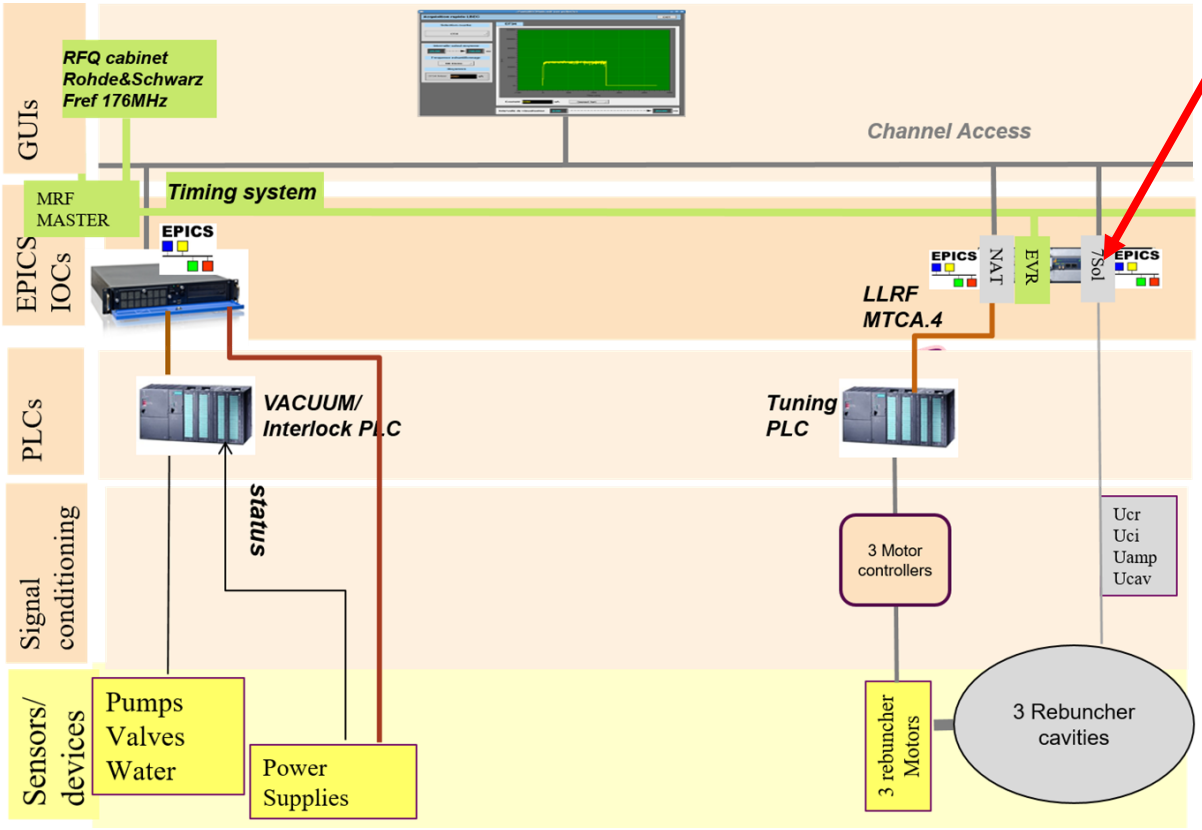
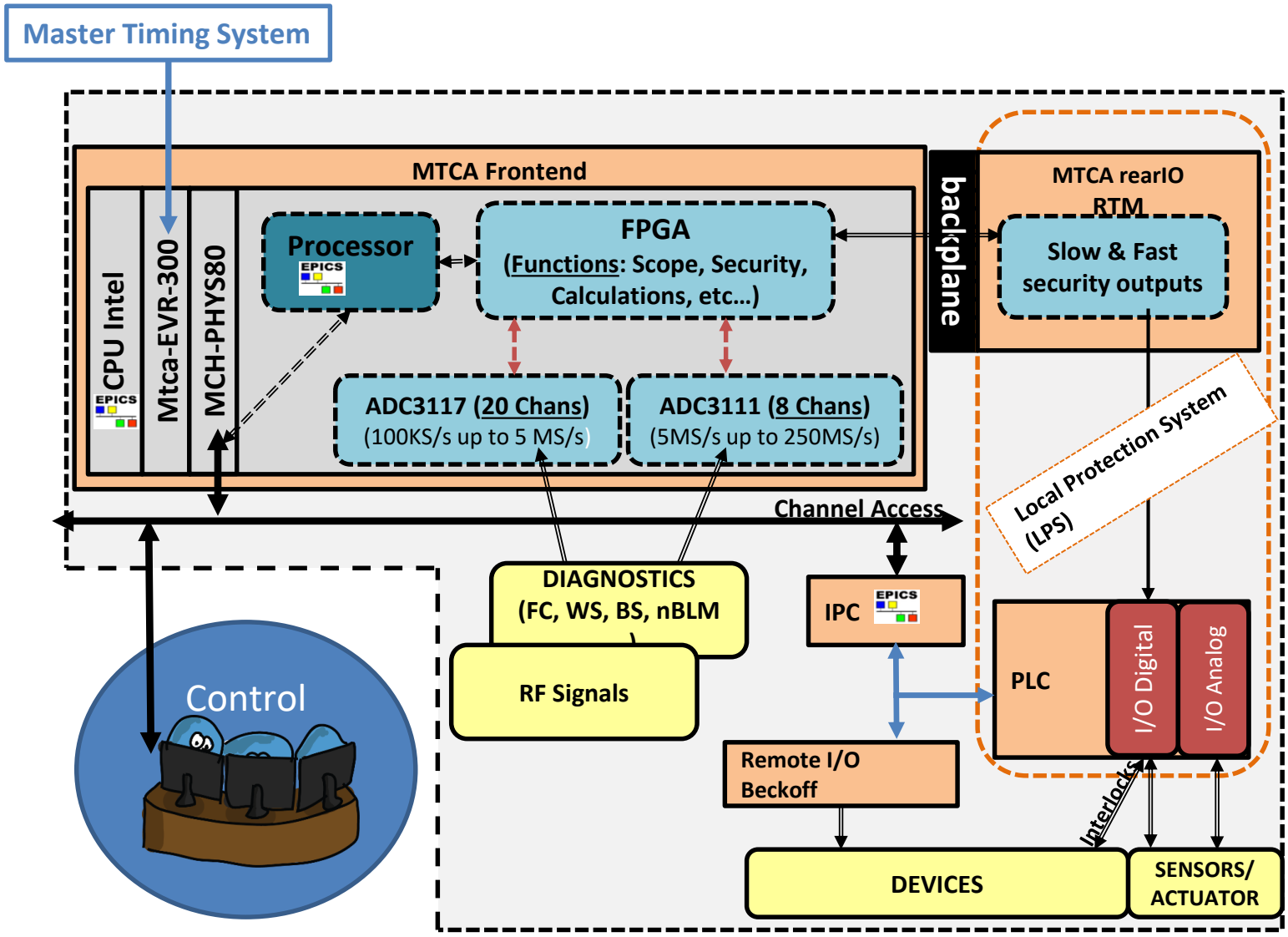


Figure 12 - LLRF SoC architecture



EPICS STANDARD PLATFORM BASED ON COTS



Local Control System (LCS)