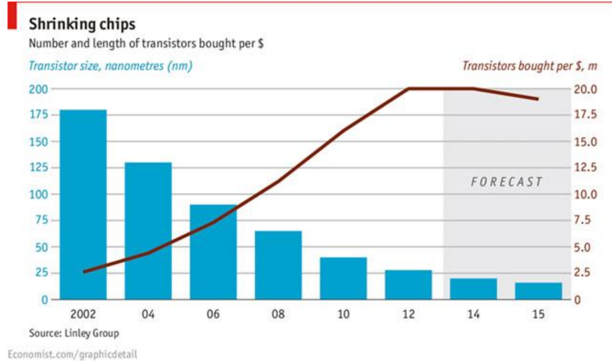
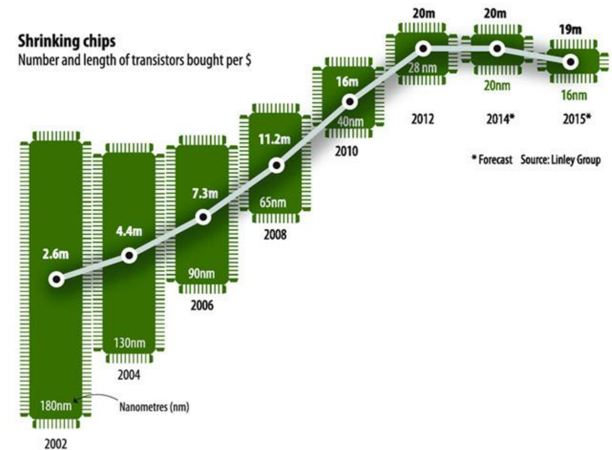
Snowmass 2021
Advanced Packaging – The New Moore's Law

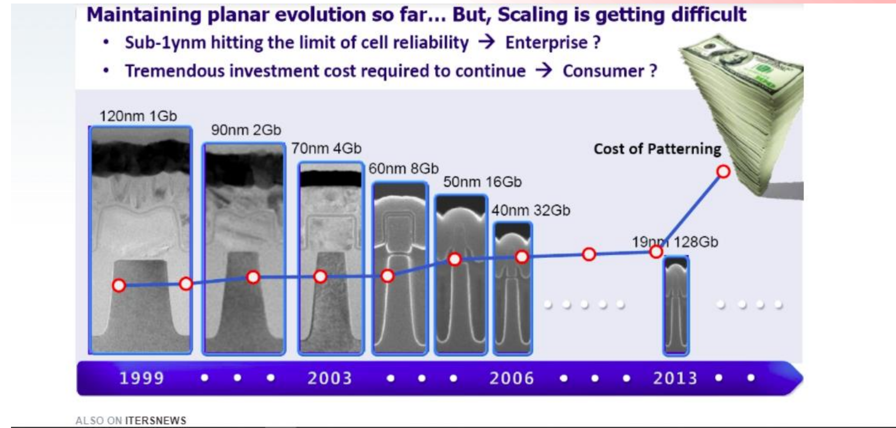
October 1, 2020

Robert Patti
rpatti@NHanced-semi.com
630-561-6813

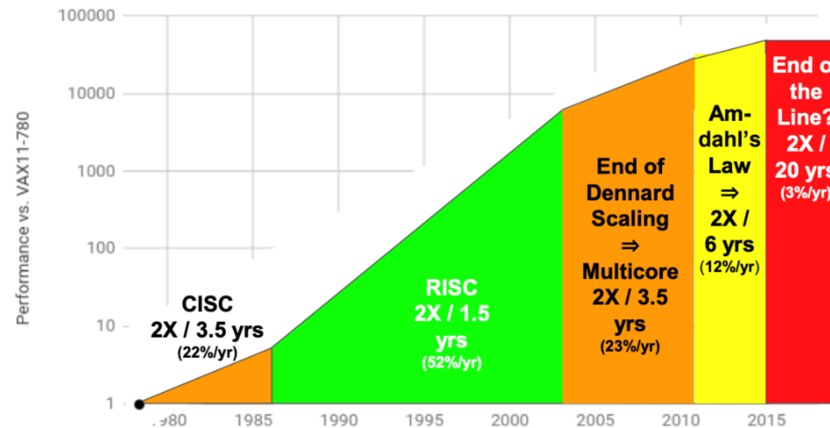
End of Old Moore's Law







End of Growth of Single Program Speed?



Apple A12 single thread performance (RISC ISA)
=
x86 Skylake single thread perf (SPEC), at much lower power, *Anandtech* 10/8/18

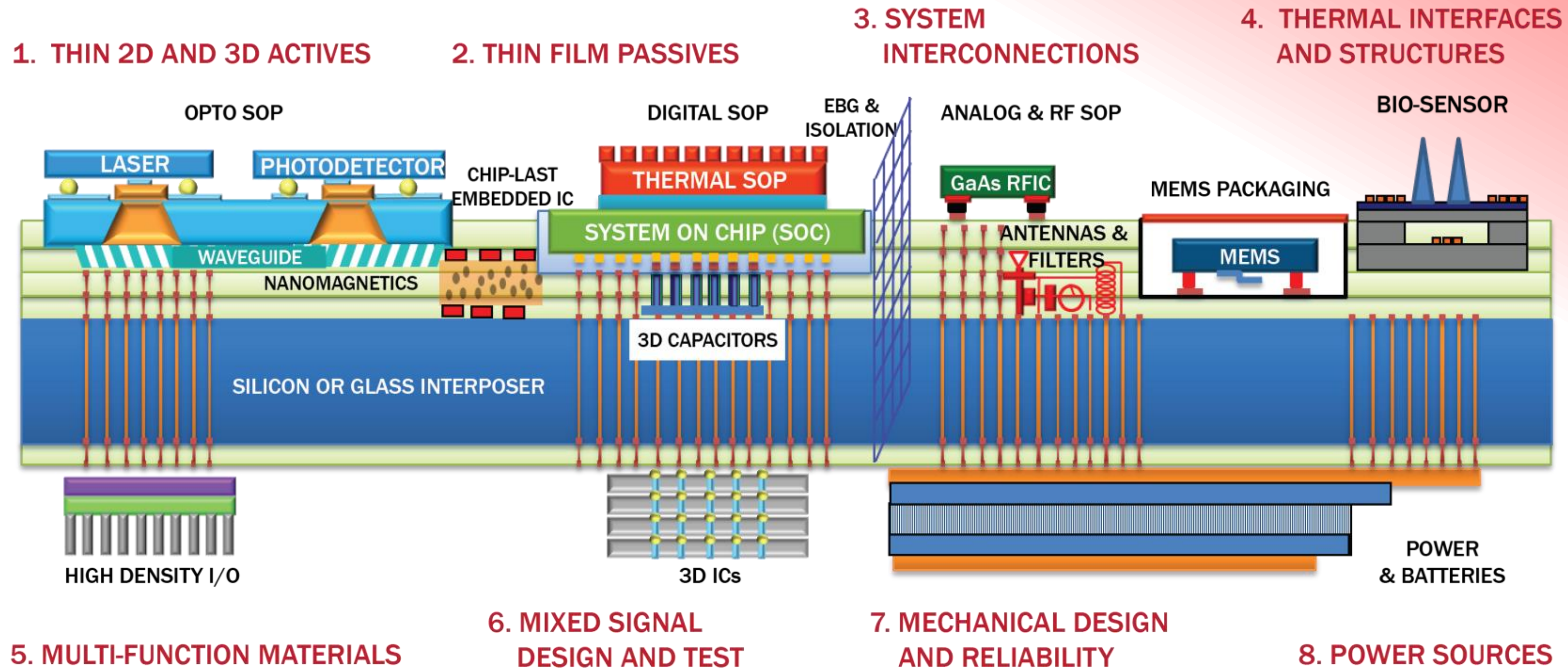
NHANCED SEMICONDUCTORS

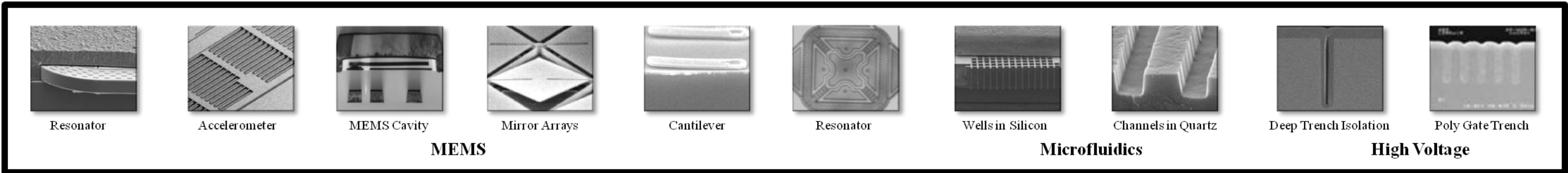
Internet Of Things

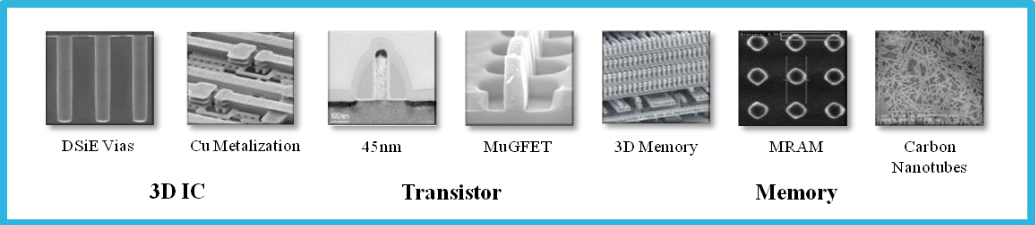
NHANCED SEMICONDUCTORS

More Than Moore

GEORGIA TECH PRC



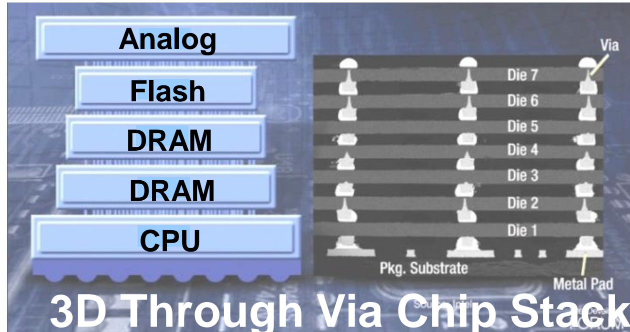




WHAT IS ADVANCED PACKAGING?

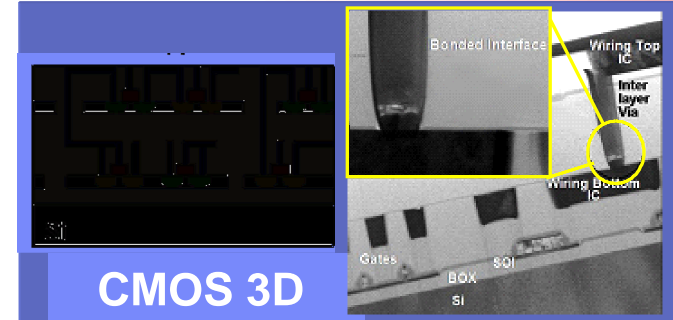
Span of Advanced Packaging

Packaging



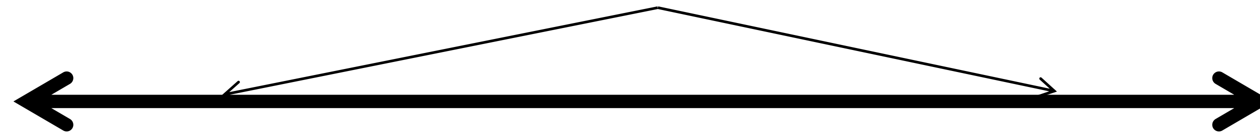
IBM/Samsung

Wafer Fab



IBM

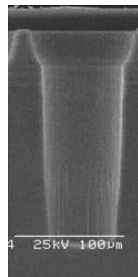
Advanced Packaging
100-1,000,000/sqmm
1000-10M Interconnects/device

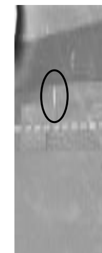


1s/sqmm

Peripheral I/O

- Flash, DRAM
- CMOS Sensors





100,000,000s/sqmm

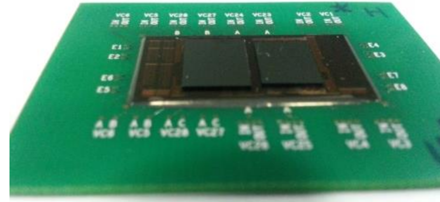
Transistor to Transistor

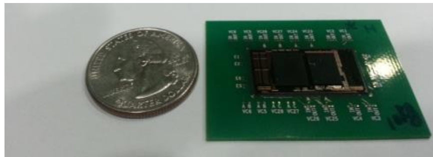
- Ultimate goal

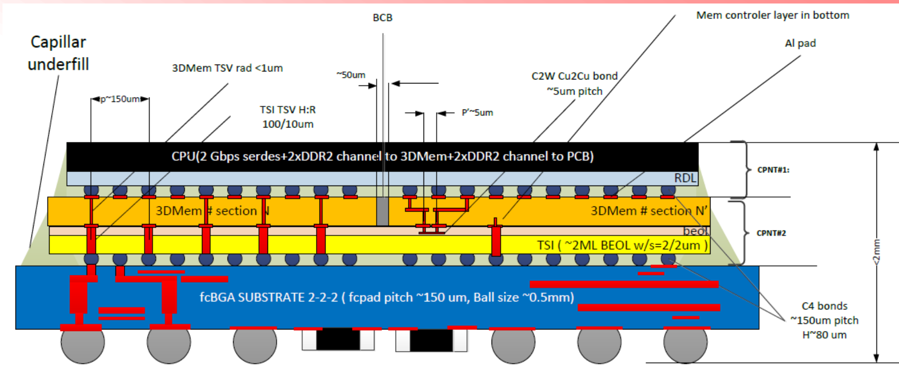
NHANCED SEMICONDUCTORS

Many Choices!

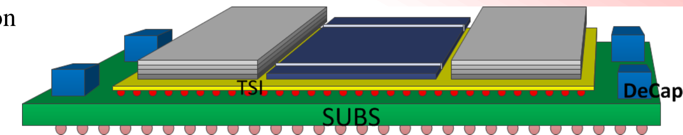
IME A-Star / Tezzaron Collaboration







IME A-Star / Tezzaron Collaboration



μBumps

Die to Wafer Cu Thermal Diffusion Bond

C4 Bumps

3 Layer 3D Memory

2 Layer Processor

FPGA (4Xnm)

level#4

C

level#3

level#2

Active Silicon Circuit Board

C

Organic Substrate

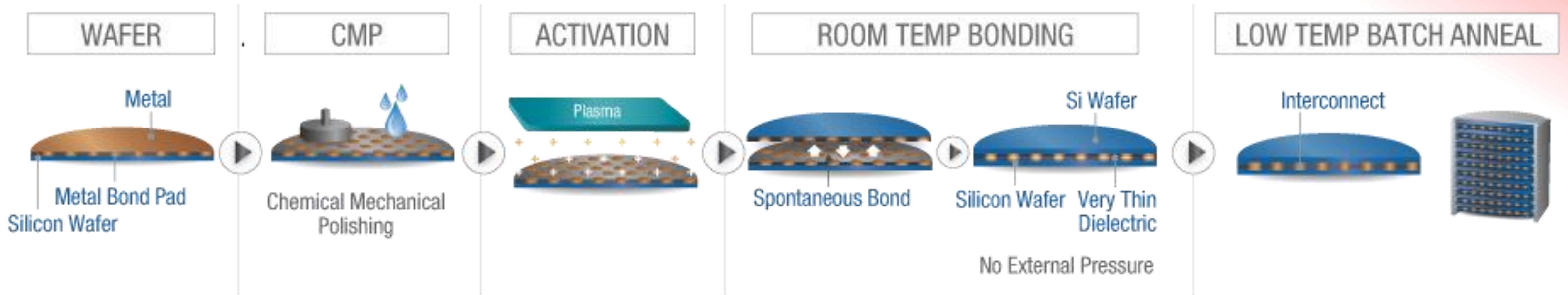
level#1

level#0

Solder Bumps

NHANCED SEMICONDUCTORS

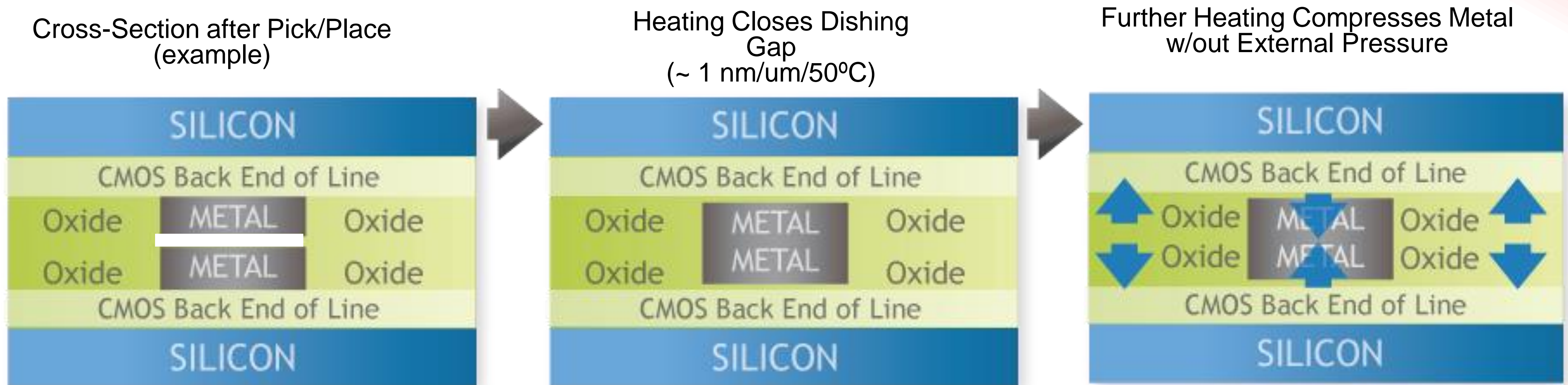
DBI®: Low Temperature Hybrid Bonding Process



NHANCED SEMICONDUCTORS

Hybrid Bonding Internal Thermo-Compression

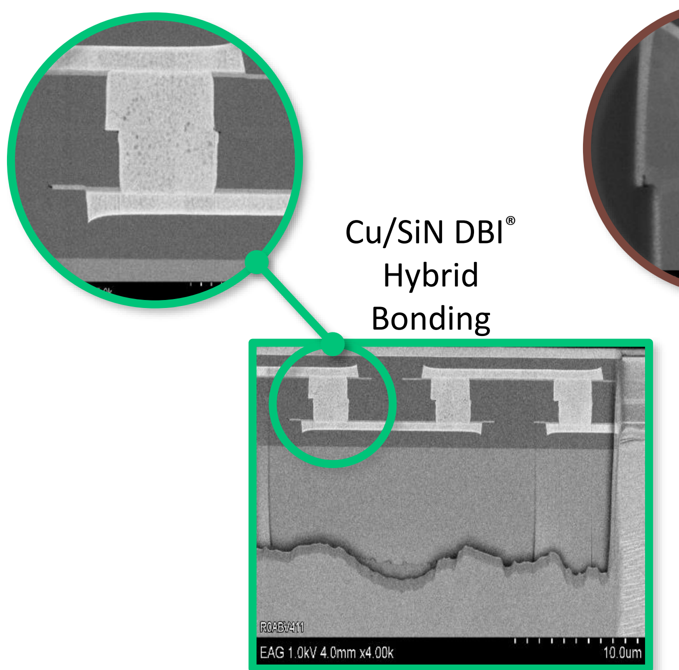
Electrical Interconnections without External Pressure
Minimizes Stress and Cost of Ownership



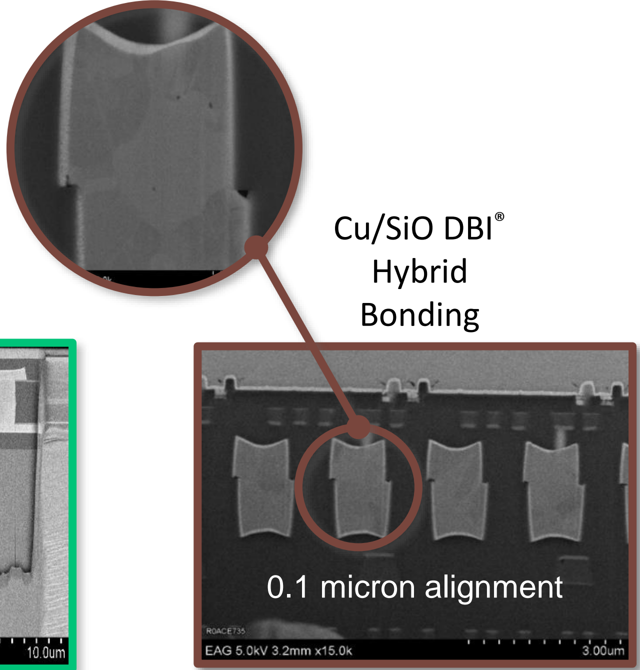
Spontaneous Chemical Reaction with Byproducts Diffusing Away from Bond Interface

NHANCED SEMICONDUCTORS

Hybrid Bonding Interconnect Pitch Scaling

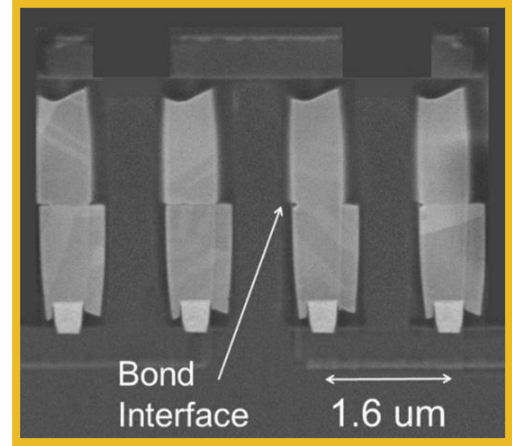


10 µm DBI® pitch, 300℃



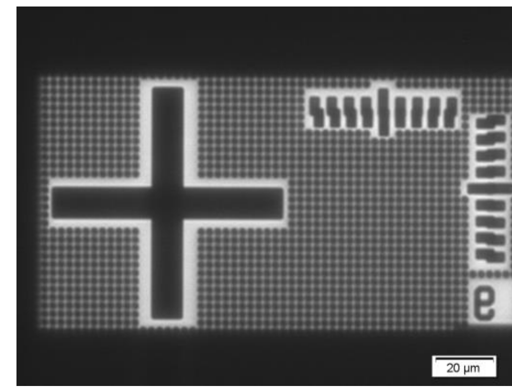
1.9 µm DBI® pitch, 300℃

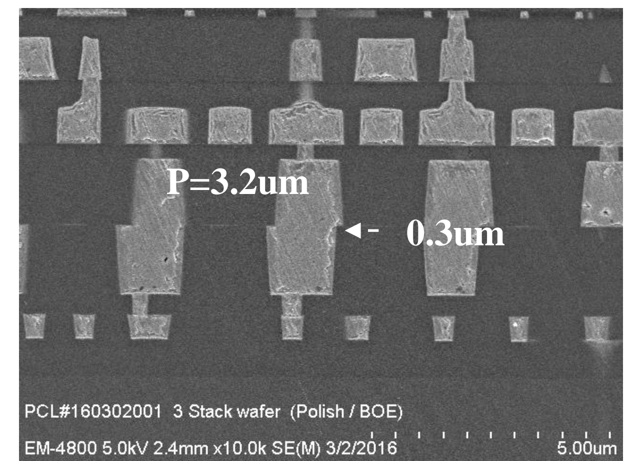
Scalable To < 1um Pitch



1.6 µm DBI® pitch, 300℃

- 3sigma < +/- 1um misalign performance
- Production Minimum pitch = 2.44um
- Best alignment is achieved with face-to-face bonding





Wafer-to-Wafer vs. Die-to-Wafer

Wafer-to-Wafer

- Process implementable in foundry back end of line (BEOL) with a low cost-of-ownership
  - Particle control requirement easily met
  - Proven in many applications
    - CMOS BSI Image Sensors
    - RF switches
- Requires wafer and die sizes to be matched

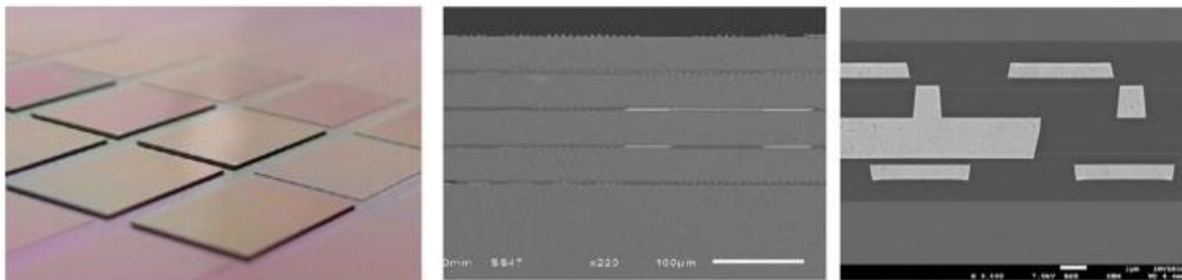
Die-to Wafer (DBI Ultra)

- Accommodates die tiling, stacking and mismatched die/wafer sizes
- Additional process steps of die singulation and handling required
  - Additional particulate/handling challenges

Die Stack with DBI® Hybrid Bonding

- Improved performance, cost, and yield/reliability potential
  - Throughput – no reflow/alloy, throughput improved x2
  - Thermals – no underfill, ΔT improved x5/10 for 4/8 high stack
  - Electrical parasitics – DBI® replaces bumps, RC improved ~ x20
  - Reduced stress – eliminate reflow/alloy and underfill
  - Reduced pitch – pick/place tool limited, throughput dependent

50um die stacked 4-high, optical and SEM cross-sections



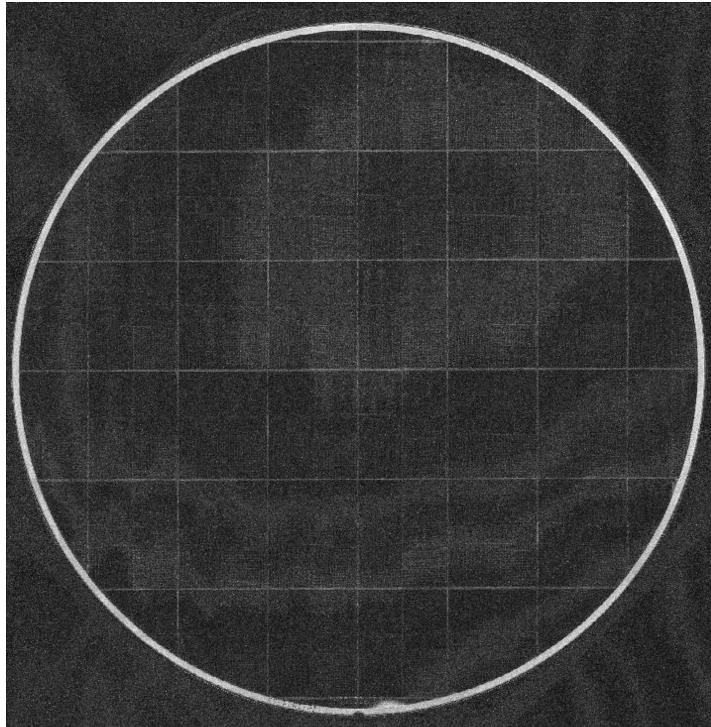
4-high 50um die stacks   4-high cross section   Die bond interface

NHANCED SEMICONDUCTORS

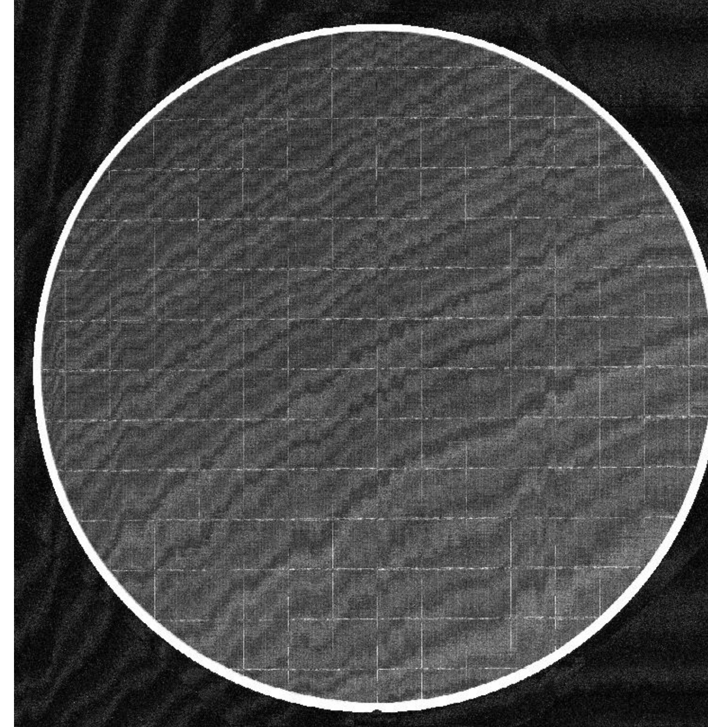
Hybrid Bonding:

Yield = 80% +/- 20% electrical yield depends on project

- 2 step anneal for SiO2 bonding first and followed by metal-to-metal bonding
- Cu and Ni are used for vertical interconnect bonding metal
- Front-to-front & back-to-front bonding depends on design
- Application for the high density fine pitch vertical interconnect



(a) C-SAM after anneal @350C of wafer bonded with large die size

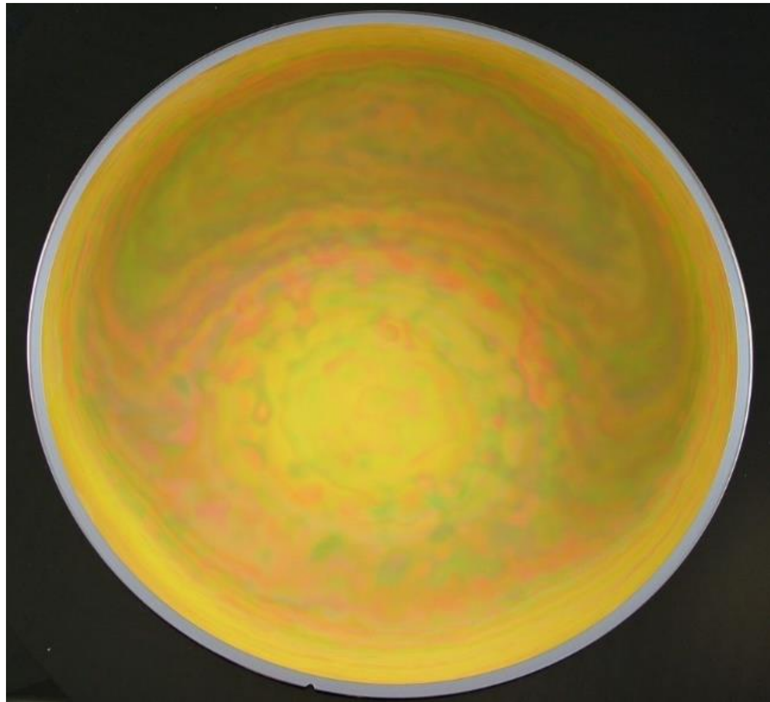


(b) C-SAM after anneal @350C of wafer bonded with small die size

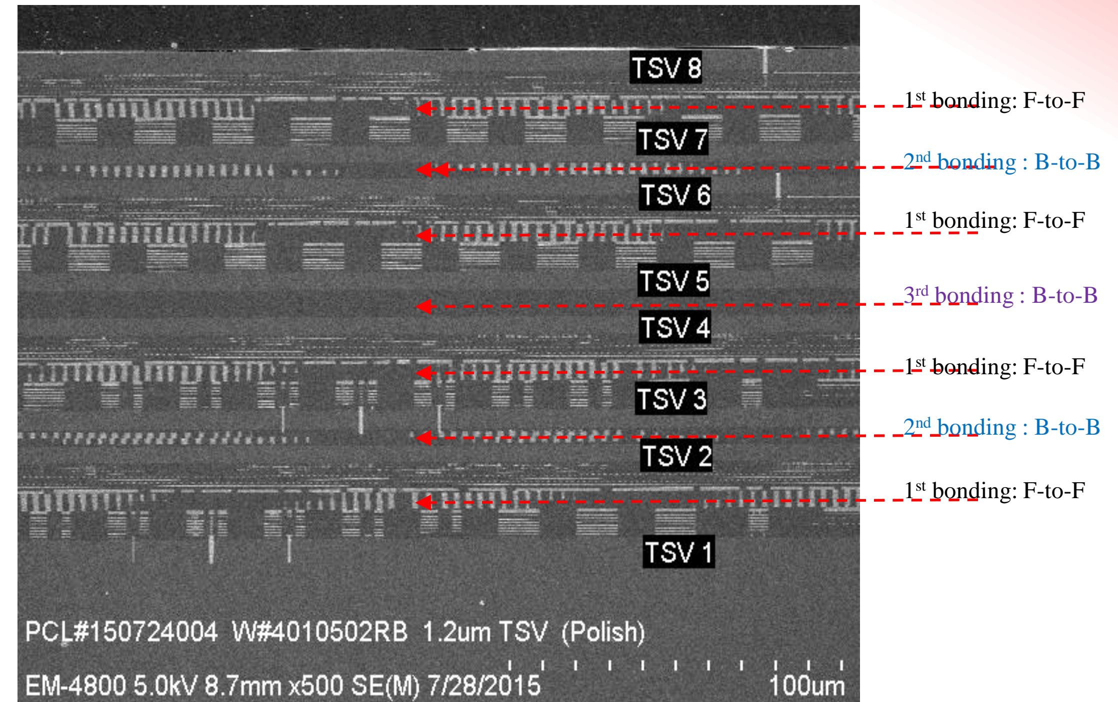
NHANCED SEMICONDUCTORS

SiO2 Bonding and Hybrid Bonding for Multi-Wafer Stacking

- 4 wafer stack : SiO2 bonding
- 8 wafer stack : Hybrid bonding
- 16 wafer stack : SiO2 bonding
- 20 wafer stacks : Hybrid bonding
- Currently ~80% of NHanced processed wafers are used for customer "production"



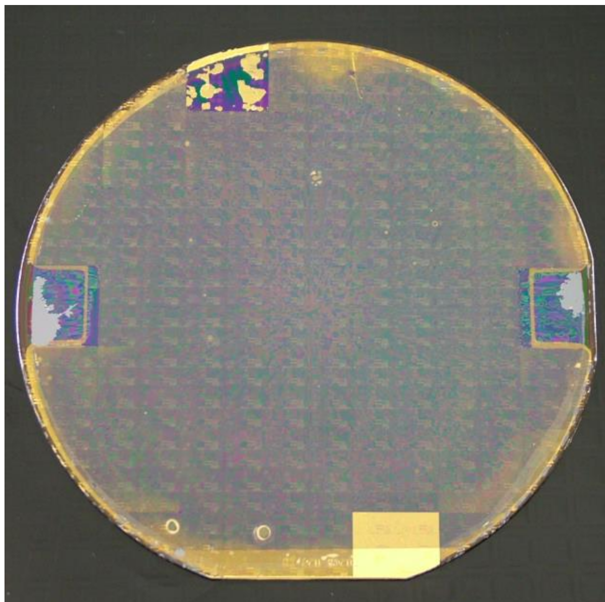
(a) Picture of 4 wafer stack bonded using SiO2 bond
Top Si has been removed



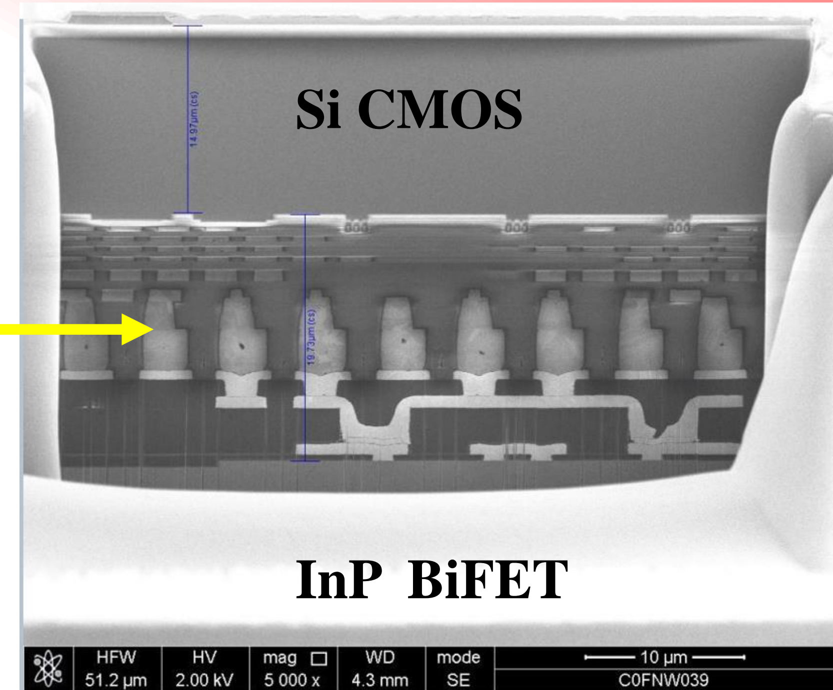
(b) SEM cross sectional micrograph for 8 device wafer stack

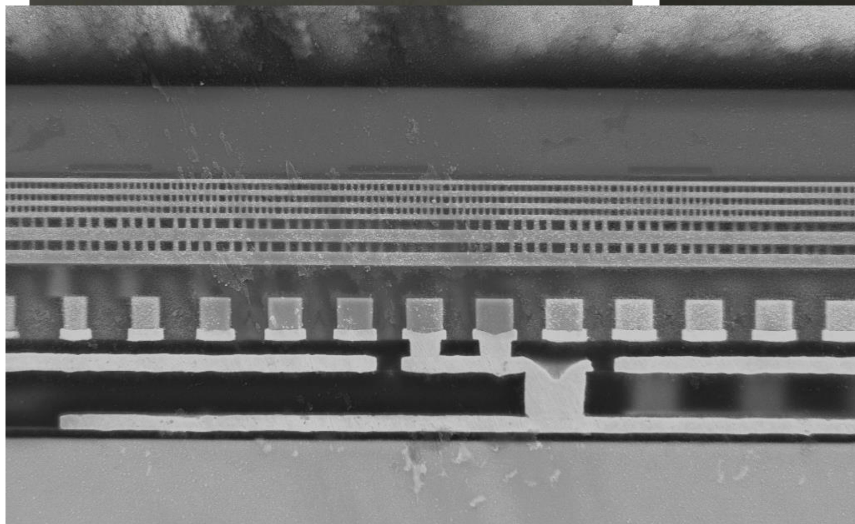
NHANCED SEMICONDUCTORS

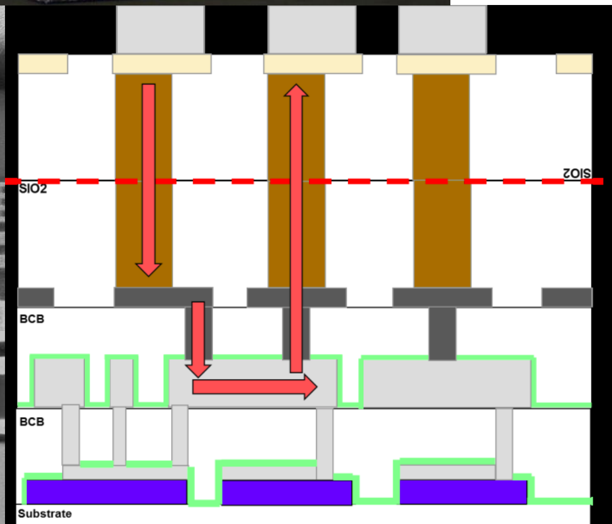
Hybrid Bonding of Heterogeneous Substrate:
Yield = 70% +/- 20% electrical yield depends on project



Bonding Interface





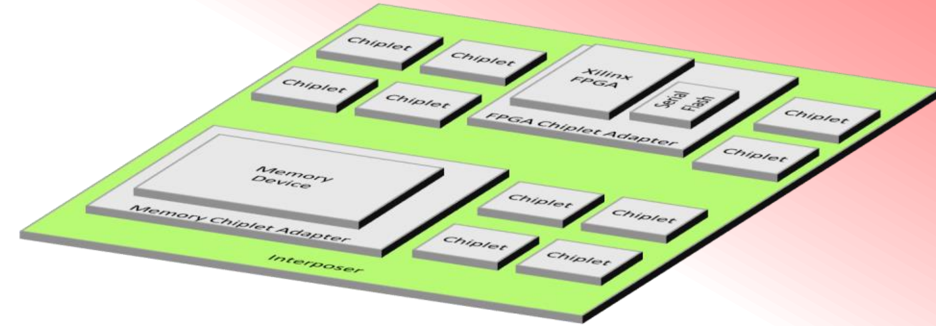


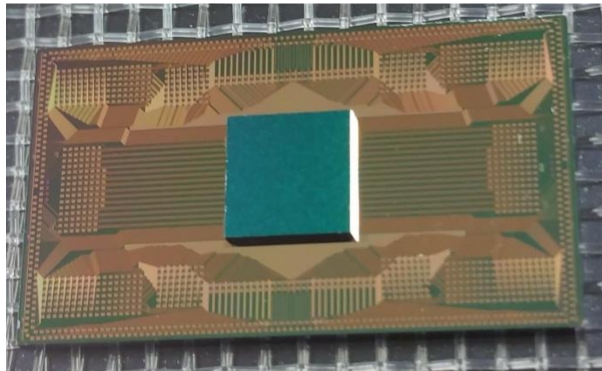
NHANCED SEMICONDUCTORS

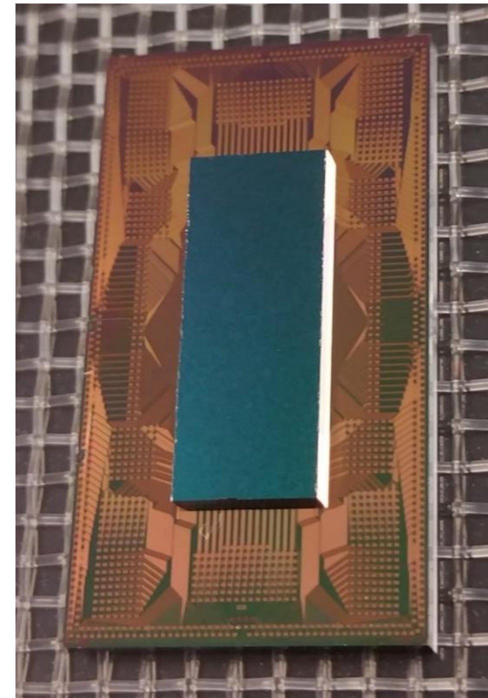
2.5D Systems

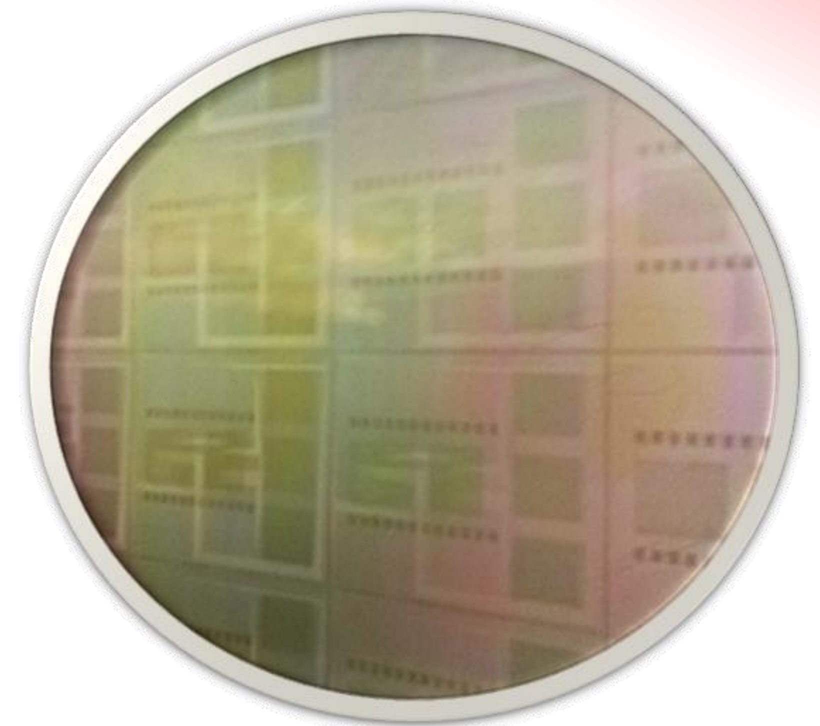
Mixed technology assemblies

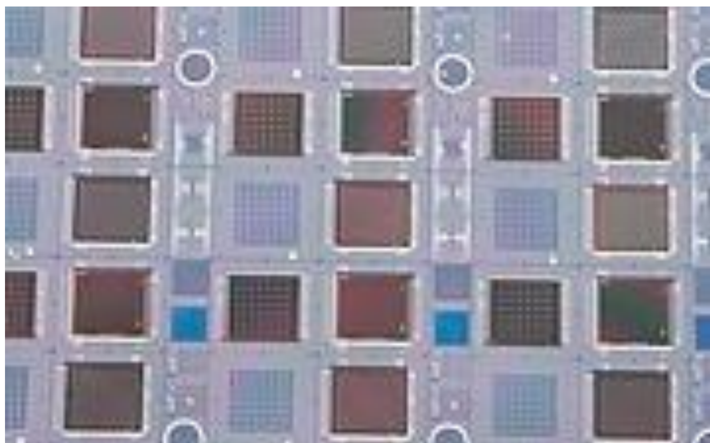
- Flip-chip
- Copper pillar
- DBI die to wafer
- Organics and silicon circuit boards







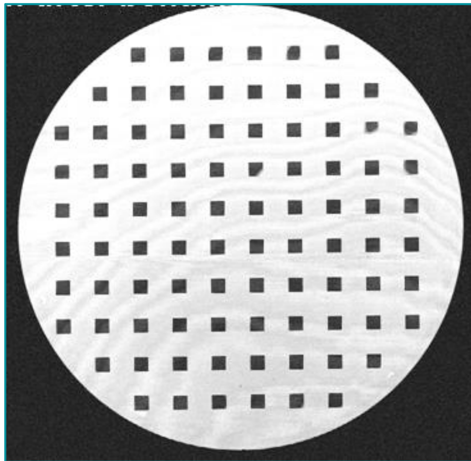
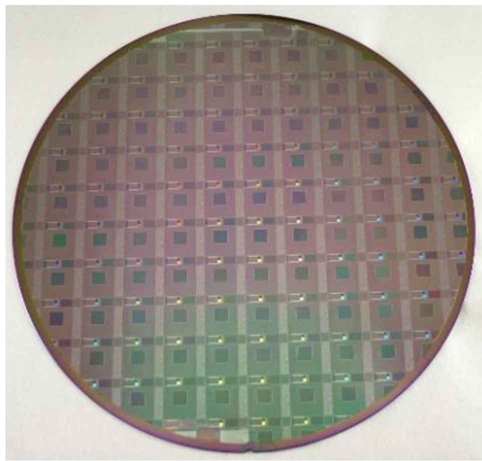




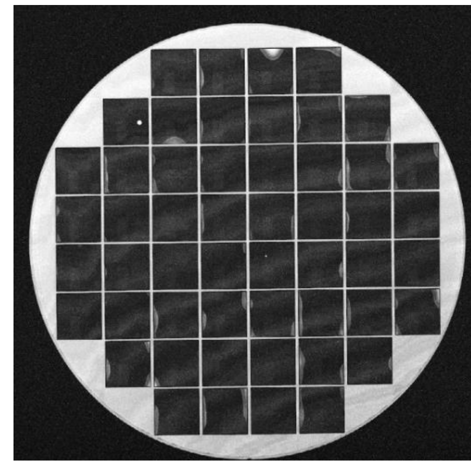
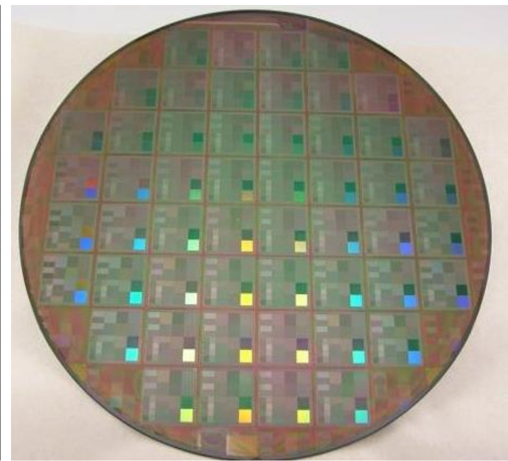
NHANCED SEMICONDUCTORS

Hybrid Bonding of Die-to-Wafer:
Yield = 80% +/- 20% electrical yield depends on project

- 2 step anneal for SiO2 bonding first and followed by metal-to-metal bonding
- Cu and Ni are used for vertical interconnect bonding metal
- Pad can be opened on die back or host wafer front.

(a) Die-to-wafer bonding for smaller die: C-SAM and wafer picture

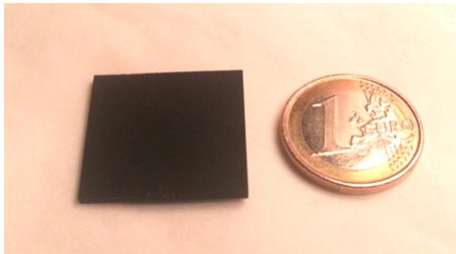



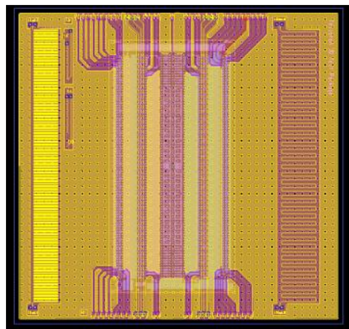
(b) Die-to-wafer bonding for bigger die: C-SAM and wafer picture

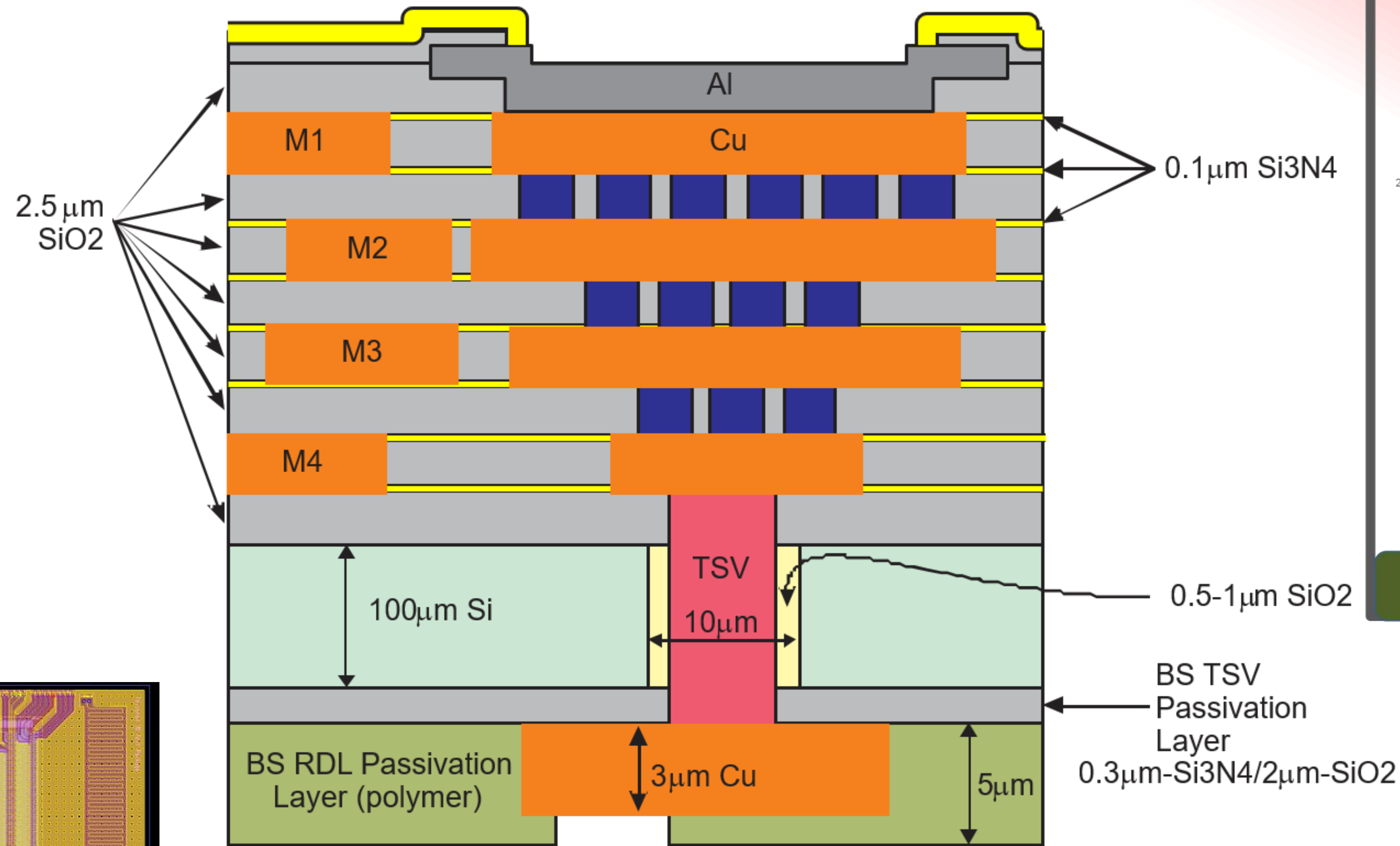
NHANCED SEMICONDUCTORS

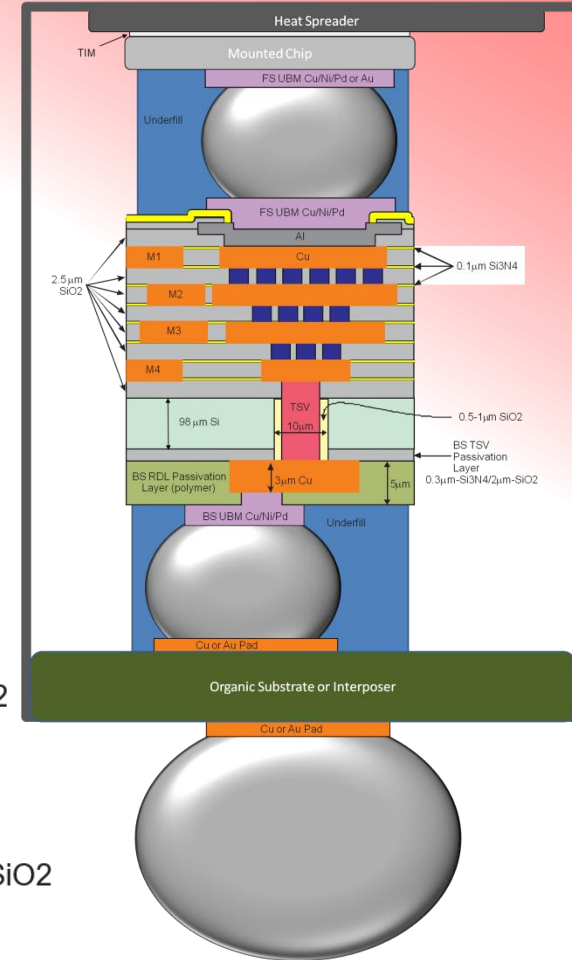
Si Interposers

Bigger, Better, Faster
>50x50mm, Up to 6 layers, Lower R,C









NHANCED SEMICONDUCTORS

Quilt Packaging

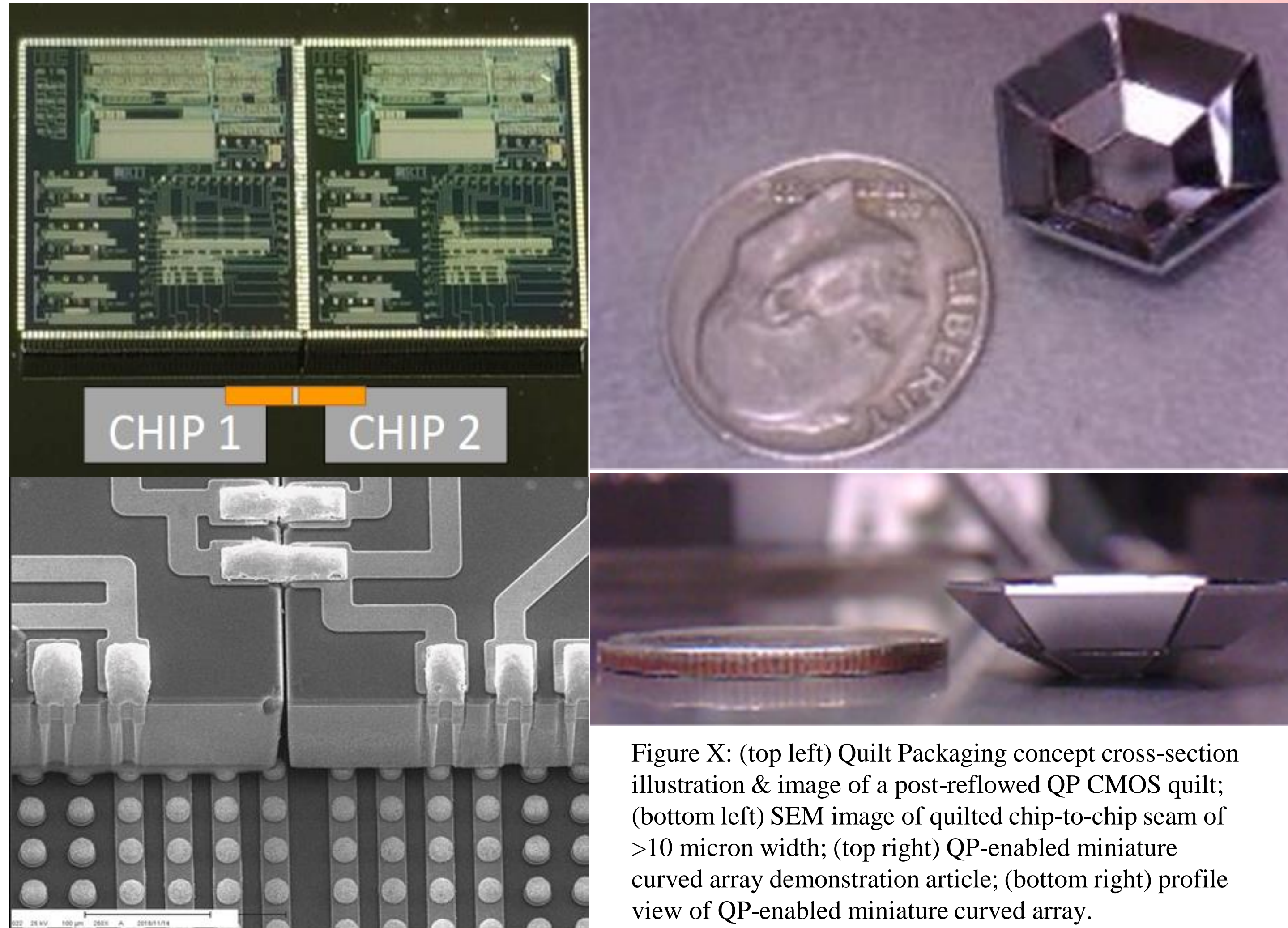
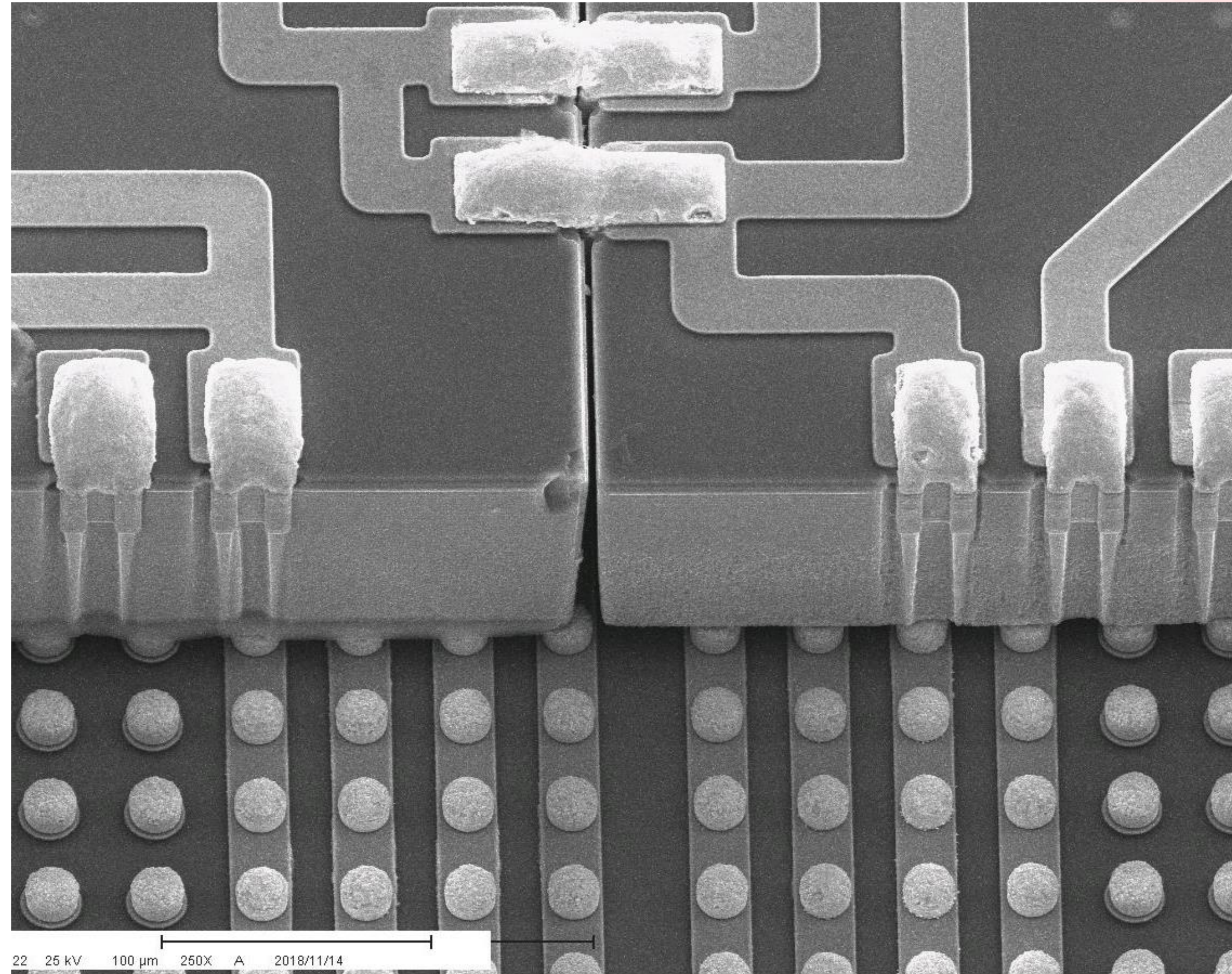


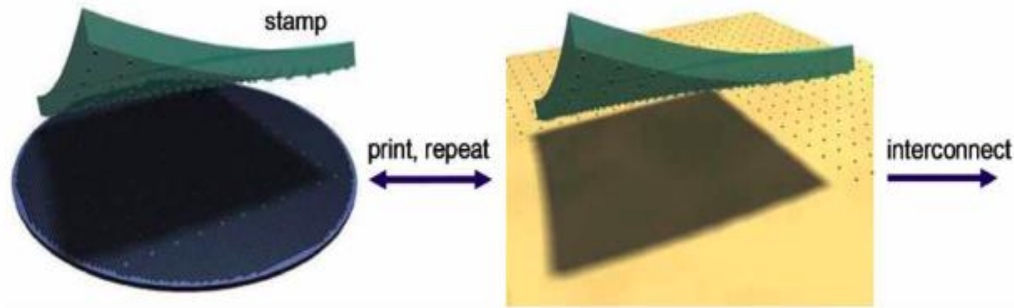
Figure X: (top left) Quilt Packaging concept cross-section illustration & image of a post-reflowed QP CMOS quilt; (bottom left) SEM image of quilted chip-to-chip seam of >10 micron width; (top right) QP-enabled miniature curved array demonstration article; (bottom right) profile view of QP-enabled miniature curved array.

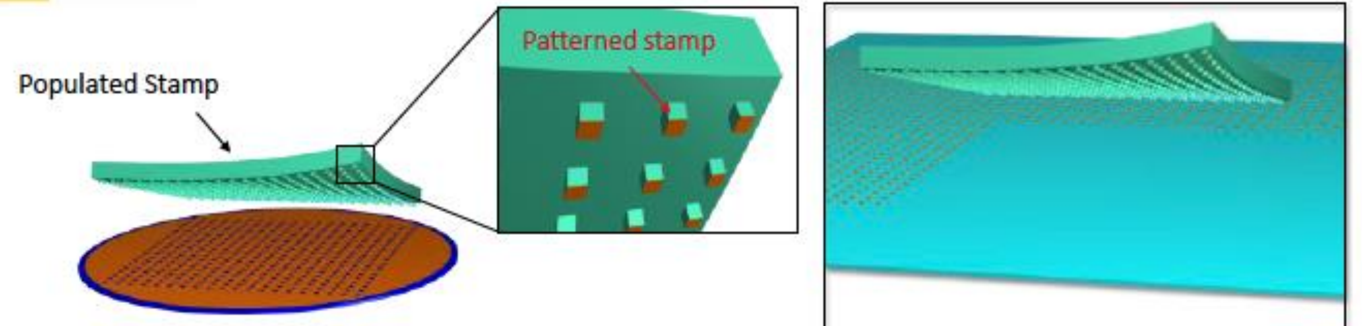
5 mm – 2x1 Quilt, Thermal Compressed – 8 µm TSV, 35 µm Pitch - Quilt #: NGQ-5-2615-2410



NHANCED SEMICONDUCTORS

Transfer Printing μChiplet





Source Wafer

Non-native “Target” Substrate

Densely packed micro components

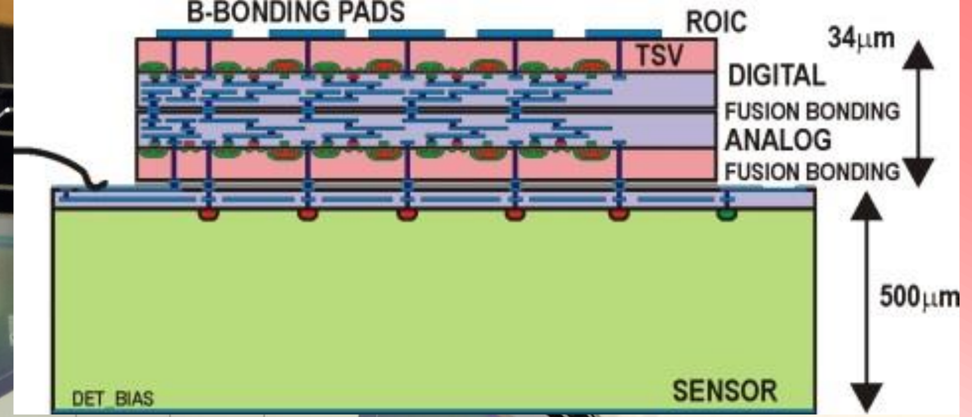
Printing

Dispersed micro components

NHANCED SEMICONDUCTORS

Wafer numbers
4 - 725μm no p spray
5 - 725μm
6 - 725μm

8 - 500μm
9- 500μm



Summary

- Advanced packaging is now driving semiconductors
- There are many options
- Investments of billions of dollars over the last decade+
  - Bought down risks
  - Created more options
- Orders of magnitude lower costs than new node
  - Technology mixing that enables
  - Denser
  - Lower power
  - Lower costs / cost of ownership
  - New directions and possibilities

NHANCED SEMICONDUCTORS