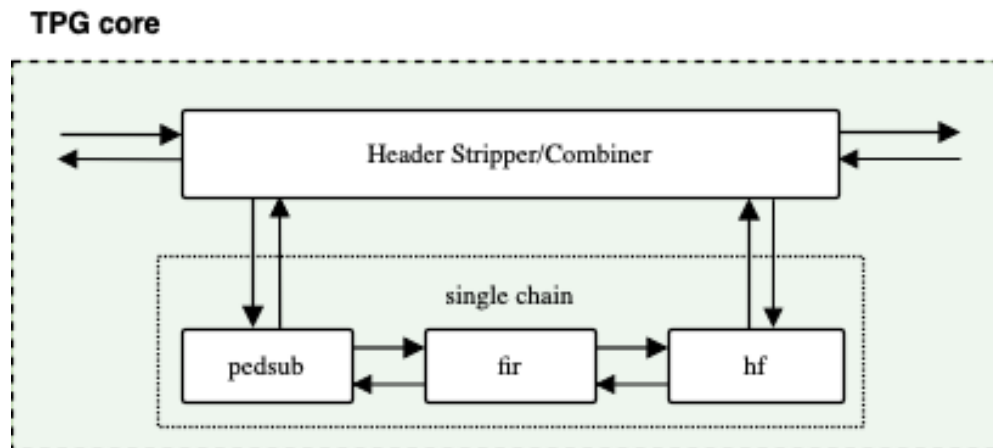# TPG core – Code Review

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Code Review

- Did a first pass through the TPG core vhdl code

- Documentation in place

  - Will be updated with more details in the next few week

- Added comments in the PedSub-FIR-HF chain

- Header SC needs some cleanup

Code Review

- Will reduce median/accumulator vector sizes in PedSub

    – Not expecting a major impact on resource utilization, but still it should be done

- Looking into how to convert the FIR to having reconfigurable number of taps & reconfigurable sets pf coefficients

    – Not going to happen within the "code review" task

- HF block registers a HitStart when 2 consecutive ADC values are above threshold and a HitEnd when the first ADC value after HitStart goes below threshold

    – Could that result to producing false hits?

    – Making it more robust is fairly straightforward

➢ Started going through the list of issues. Currently < 30 and will be further reduced

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