TPG Firmware
- Rough Resource Estimates for 128 Time Ticks
-

Kunal Kothekar

Firmware Meeting.

08/10/2020

- A complete resource utilization document prepared by DGC can be found at : Firmware Resource Utilization Document, January 2020

- It will need an update, as many things have changed from January 2020, till the final phase of the protoDUNE – I in July 2020.

- Nevertheless it's a very good estimate.

- Currently we use 64 ADC value (time ticks) frame as our standard unit to find hits and process the data.

- We have been asked by data-selection group to check the feasibility of the firmware if we increase this size to 128 ADC ticks.

- A short answer is YES*, details will follow.

  *Based on initial rough estimates and purely from the resource point of view.

Resource Utilization

- FPGA resources used by different processing blocks. The amount of dedicated RAM has been expressed both as the number of 36kbit Block RAM tiles and also as the number of Mbits used.

Resource	Felix Infras-tructure	per hit finder	per filter	per com-pression unit	per buffer manager	per NVMe inter-face	total per APA
CLB LUTs	26071	514	2435	165	26876	2951	183409
CLB Registers	11232	420	1884	184	32846	4495	152588
Block RAM Tile	176	0	0.5	8	384	66	1032
RAM/Mb	6.19	0.00	0.02	0.28	13.50	2.32	36.28
DSPs	0	0	32	0	3	0	1283

- FPGA resources used by different processing blocks. The amount of dedicated RAM has been expressed both as the number of 36kbit Block RAM tiles and also as the number of Mbits used.

| Resource	Felix Infras- tructure	per hit finder	per filter	per com- pression unit	per buffer manager	per NVMe inter- face	total per APA
CLB LUTs	26071	514	2435	165	26876	2951	183409
CLB Registers	11232	420	1884	184	32846	4495	152588
Block RAM Tile	176	0	0.5	8	384	66	1032
RAM/Mb	6.19	0.00	0.02	0.28	13.50	2.32	36.28
DSPs	0	0	32	0	3	0	1283

Can be removed

Resource Utilization

- FPGA resources used by different processing blocks. The amount of dedicated RAM has been expressed both as the number of 36kbit Block RAM tiles and also as the number of Mbits used.

Resource	Felix Infras- tructure	per hit finder	per filter	per com- pression unit	per buffer manager	per NVMe inter- face	total per APA
CLB LUTs	26071	514	2435	165	26876	2951	183409
CLB Registers	11232	420	1884	184	32846	4495	152588
Block RAM Tile	176	0	0.5	8	384	66	1032
RAM/Mb	6.19	0.00	0.02	0.28	13.50	2.32	36.28
DSPs	0	0	32	0	3	0	1283

Should be doubled
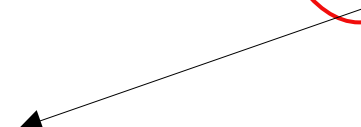
Current standings

- Fraction of resources used to process a single APA for different FPGA

Resource	per APA	Zynq Ultra-scale+ ZU15EG	Fraction of resources used	Virtex Ultra-scale+ VU9P	Fraction of resources used	Versal VM1802	Fraction of resources used
CLB LUTs	183409	341000	0.54	1296000	0.14	899840	0.20
CLB Registers	152588	682000	0.22	2592000	0.06	1968000	0.08
Block RAM Tile(36kb)	1032	744	1.39	2160	0.48	967	1.07
Block RAM/Mb	36	26	1.39	76	0.48	34	1.07
Ultra RAM/Mb	0	31.5		270		27	
Total RAM/Mb	36	58	0.63	346	0.10	61	0.59
DSPs	1283	3528	0.36	6840	0.19	1968	0.65

Projected Standings for 128 ticks

Resource	Versal VM1802	Per APA (before)	Per APA *(after)	Fractions of resources used (before)	Fractions of resources used *(after)
CLB LUTs	899840	183409	197783	0.20	0.21
CLB Registers	1968000	152588	169084	0.08	0.085
Block RAM Tile (36 kb)	967	1032	964	1.07	1.00
Block RAM/Mb	34	36	34.99	1.07	1.02
Ultra RAM/Mb	27	0	0		
Total RAM/Mb	61	36	34.99	0.59	0.57
DSPs	1968	1283	1286	0.65	0.65

* after doubling the buffer manager and removing compression and NVMe

Summary

- As can be seen from the previous slide, 128 ADC ticks does not make much difference to current resource utilization.

- As per doing this, will need significant changes in buffer/data reception block.

- Hit finding will not be affected by this.

- Need to know the motivation to do this changes, as it will not benefit to firmware design. The interface (to the trigger) as it is, does not see this frame division.

- Another interesting thing is to introduction of new parameters in HFA, which will not affect resources as much.

Back-up