Fast Waveform Digitizer

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- Plan of my talk
  - Need
  - Approaches
  - Present status
  - Future plans

Need of pulse profile

- Pulse capture and processing is the present day demand in Particle physics and Astroparticle physics experiments
- Sample the waveform in real time and record digitized data only on a event
- Accuracy depends on the sampling frequency , digitization resolution, process noise removal etc.

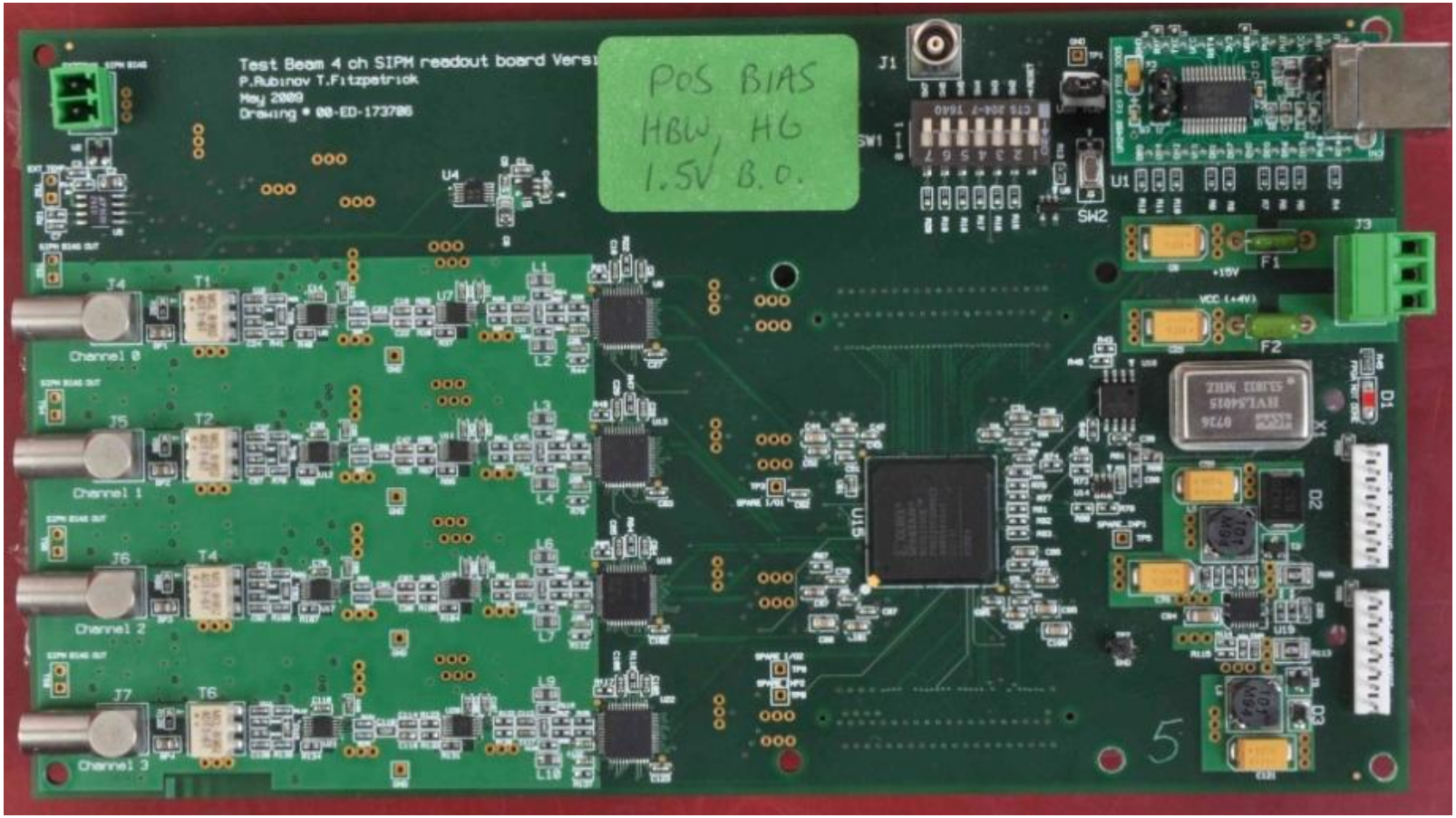
Basic approaches

- Sample the wave form at optimum sample rate for proper reconstruction of original wave form
- Few Techniques
  - Flash ADC
    - Concurrent Sampling and Digitization
    - Long sampling depth (limited by memory size)
    - Better accuracy and stability
    - Max resolution is fairly low;
    - Commercial fast digitizers exploit this technique.
  - Pipelined ADC
    - Multiple Flash stages
    - Achieve higher resolution than flash Adc for a given no of comparators
    - Same throughput as Flash ADC
  - Switched Capacitor Array
    - Analog Sampling at higher speed, but slow digitization
    - Self calibration needed for correction
    - Lower power and Cost at low sampling depth
    - Need an external trig to get digitized data

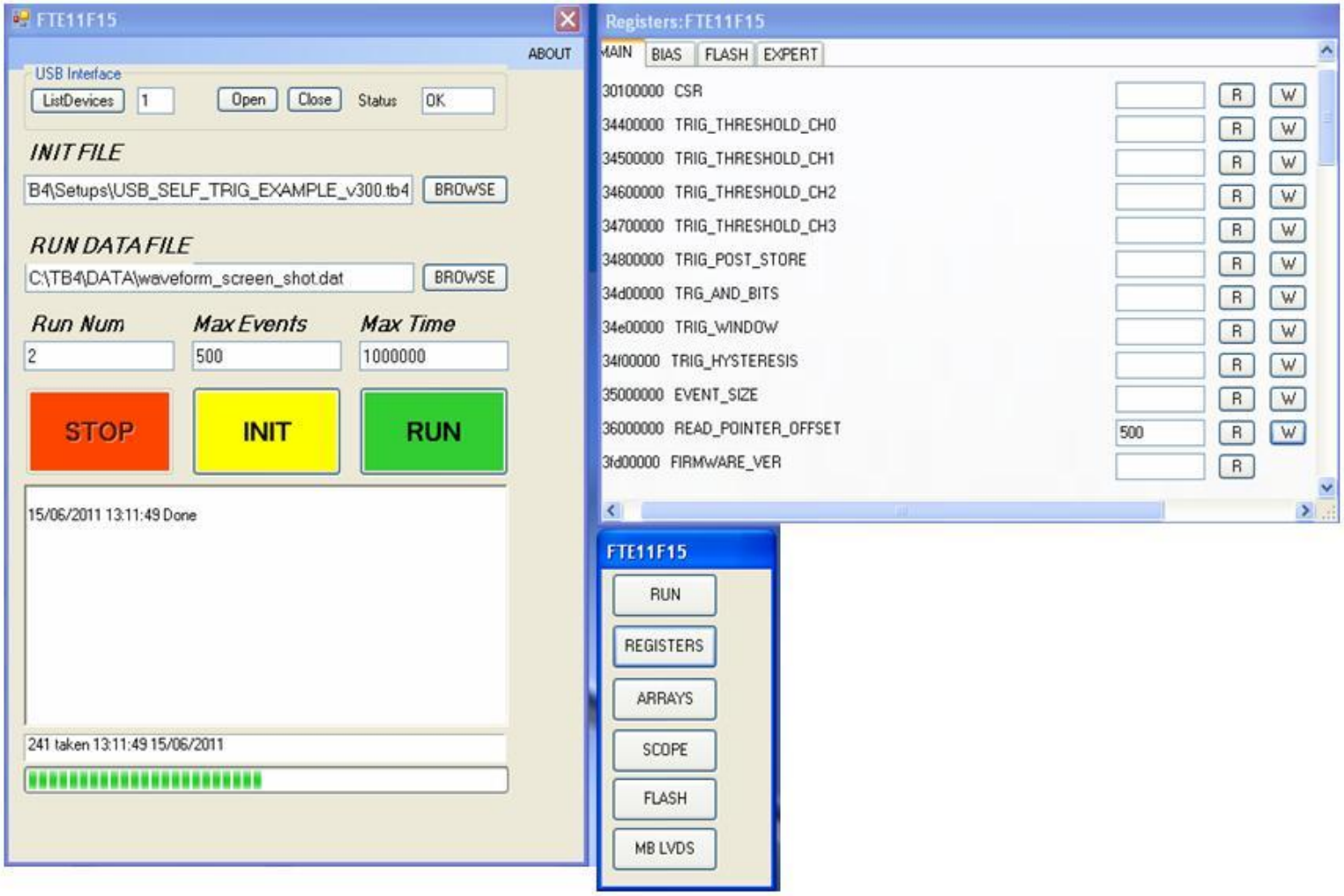
TB4 Digitizer Tests

- FNAL group provided TB4 waveform Digitizer used in Test beam activities at FNAL
  - Flash ADC based digitizer
  - 4 channel, 14 bit, bipolar 210 MSPS digitizer
  - input range : ~30mV full scale
  - Built in amplifier stages
  - Memory depth of 4k samples/channel
  - USB interface
  - Built in Bias generator for SiPMs

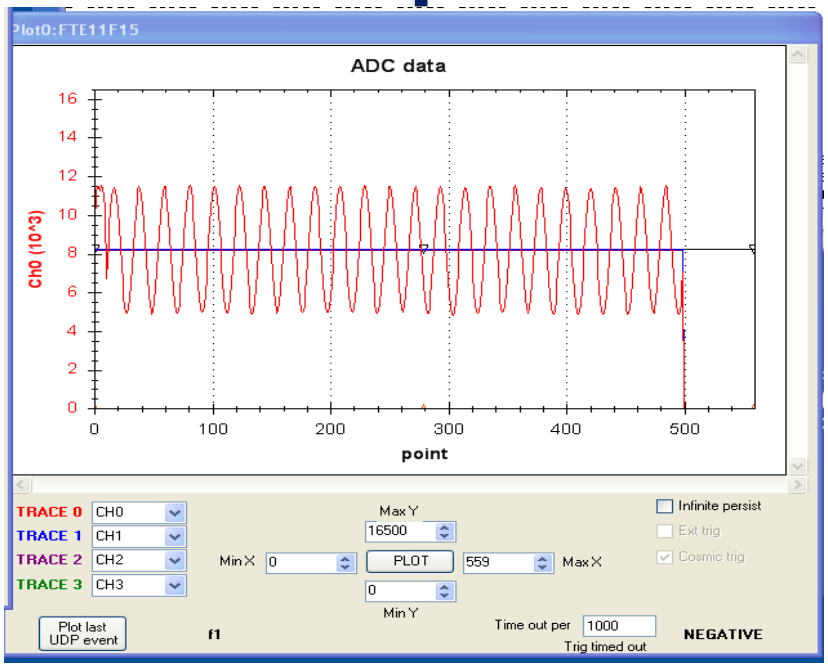
TB4 board (Developed by FNAL)

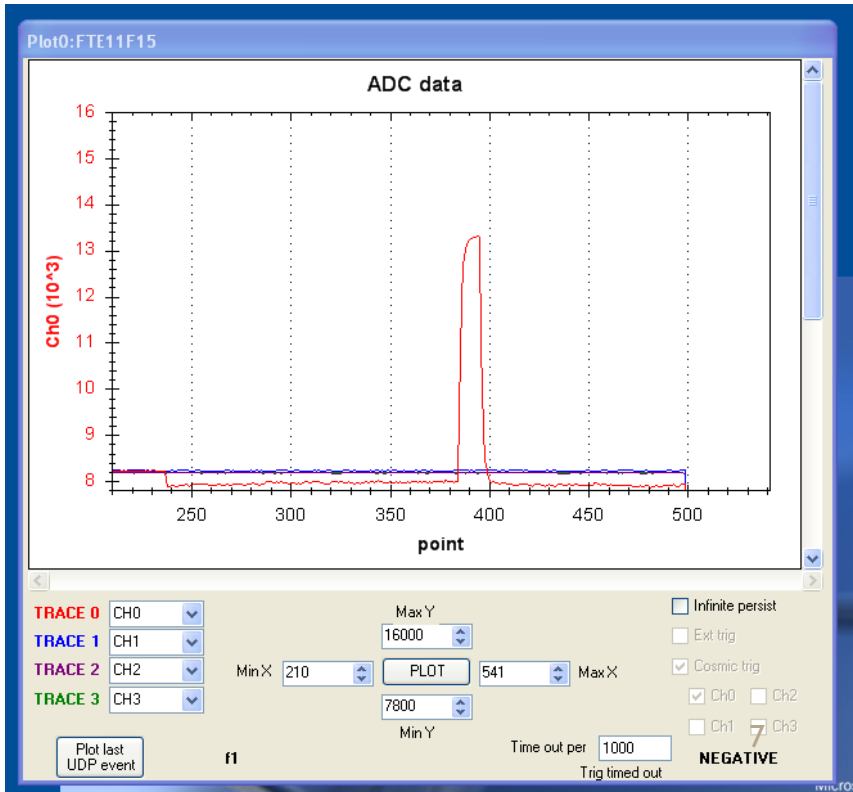


TB4 GUI components…

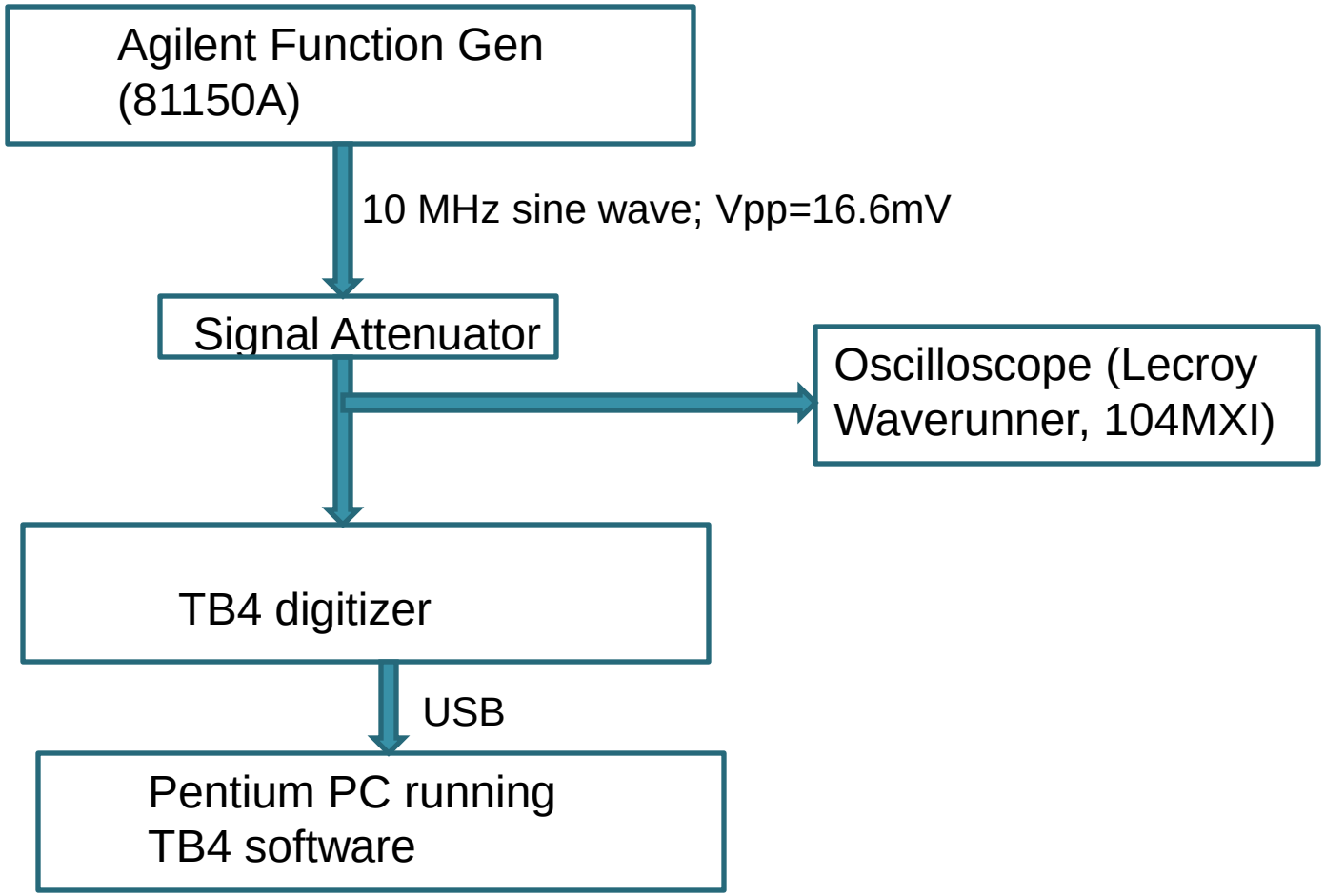


Captured waveforms in TB4



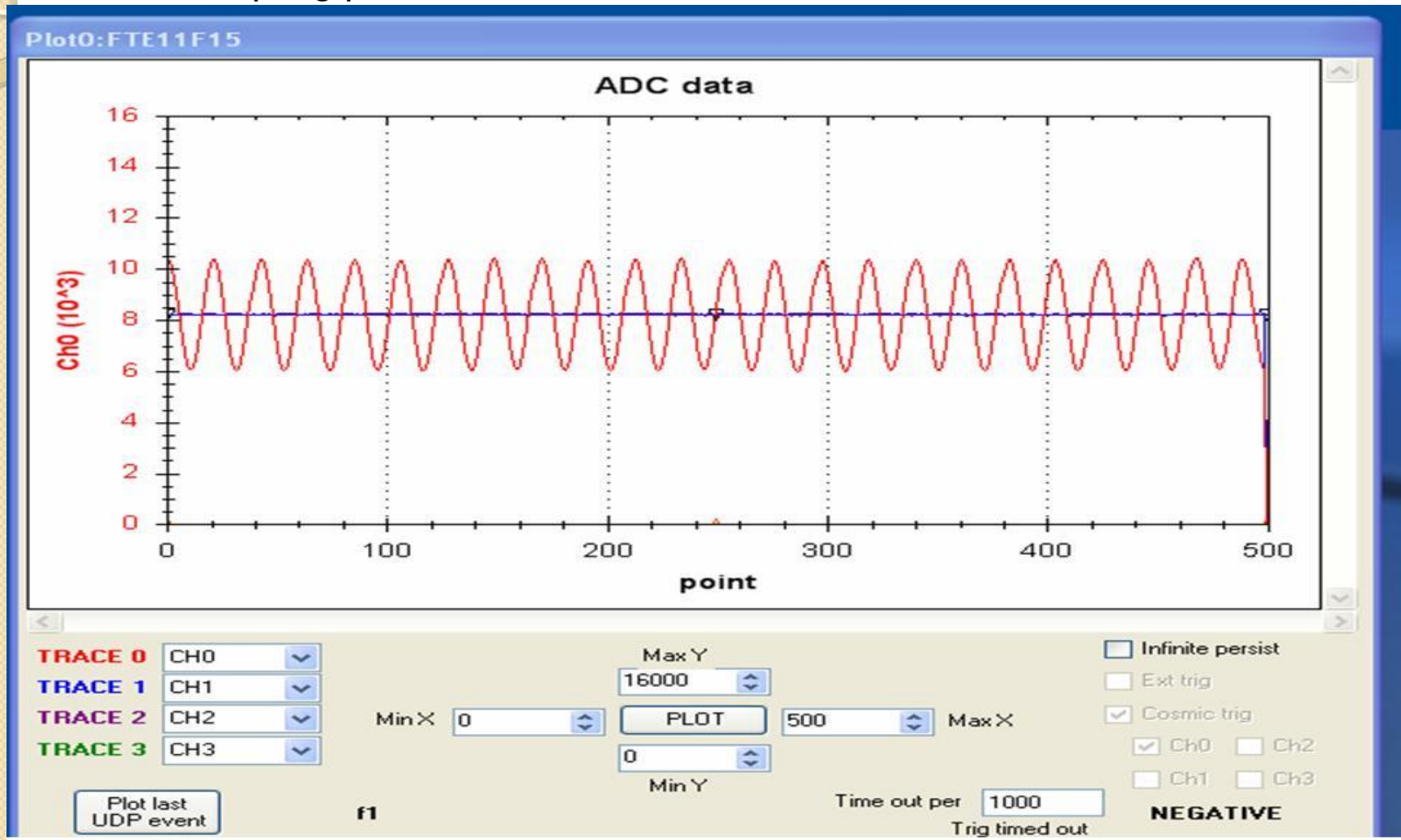


Gain Linearity Test set-up

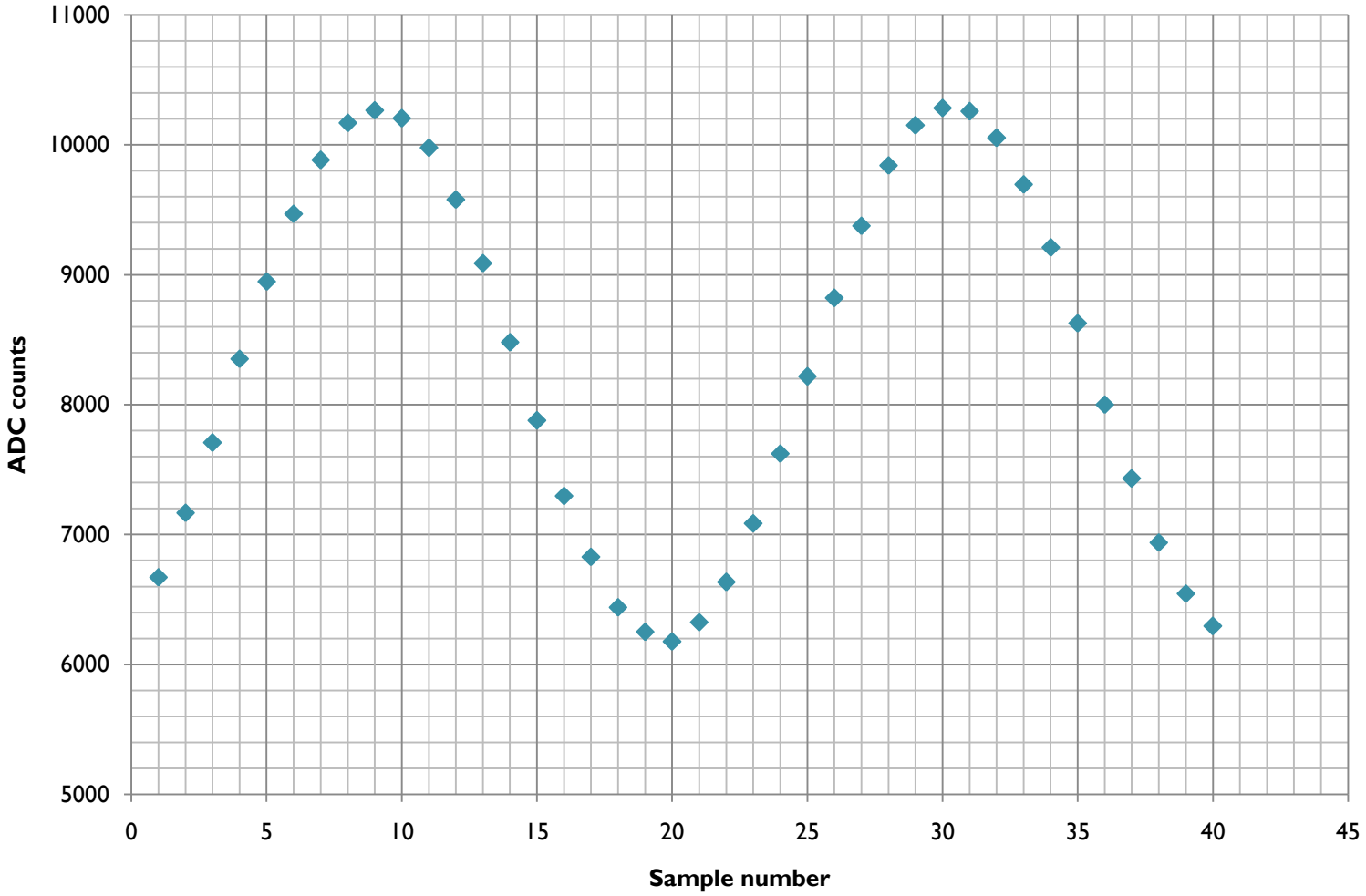


TB4 tests…
waveform reconstructed by TB4…

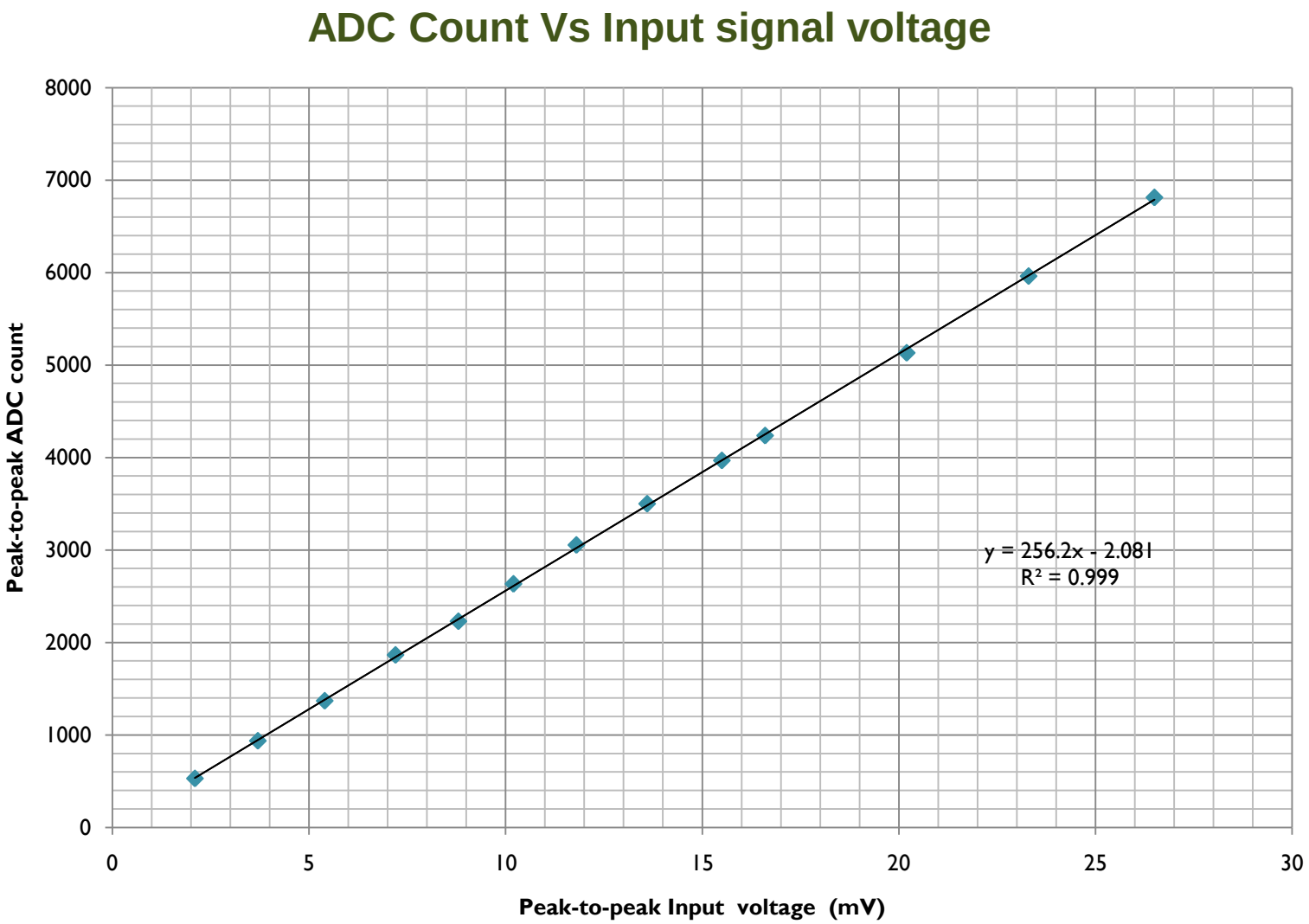
Input: 10 MHz sine wave; Vpp = 16.6 mV ;
Sampling period: 4.76 ns



Digitized Output Data

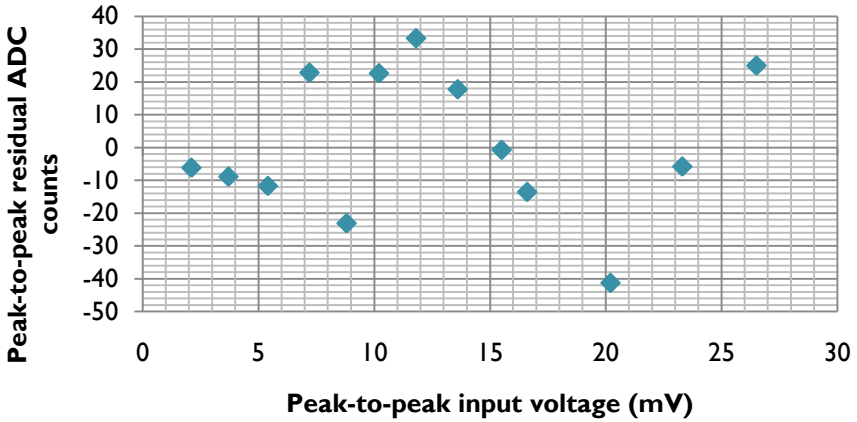


Gain Linearity Test Result

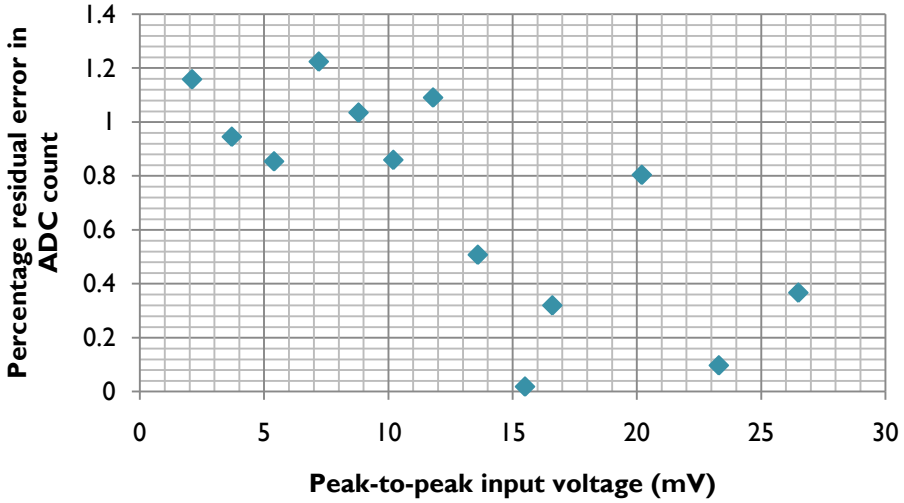


Gain Linearity Test result

Residual ADC counts (absolute) Vs Input voltage



Percentage error in ADC counts Vs Input voltage



Future plan

- Detailed understanding of TB4 board
- Propose to design 4/8 channel board in collaboration with FNAL/ANL, USA
  - Higher sampling freq with enough sampling depth
  - Standard interfacing for control and data transfer
  - Flexibility and scalability
  - The architecture may be used for project X experiments