DUNE Timing System-Single Phase Test Results

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1 Introduction

This document describes the results from the first steps taken to prototype the DUNE Timing System-Single Phase (DTS-SP) [3], as well as functionality tests carried out with the ProtoDUNE-Single-Phase (SP) Run I timing system.

2 Integration tests

As part of the DTS-SP prototyping process, a Schroff 11890-170 Micro Telecommunications Computing Architecture (μTCA) crate, and an AMC FMC Carrier (AFC) board [2] were purchased. The AFC is being considered to be the advanced mezzanine card (AMC) which hosts the Fibre Interface Board (FIB). The two units were operated together, and the existing timing FPGA Mezzanine Card (FMC) was used to start assessing AFC's suitability as a fan-out AMC.

2.1 μTCA crate-AFC

The following operations were successfully tested with the μTCA crate and the AFC.

- remote programming of AFC FPGA
- configuration of AFC clock routing circuity using Intelligent Platform Management Interface (IPMI) commands
- configuration of AFC on-board oscillator using IPMI commands

2.2 AFC-Timing FMC

The timing FMC, in endpoint mode, acts as a downstream/upstream timing link via a Small Form-Factor Pluggable (SFP) transceiver, and recovers the clock from the data-stream using a Clock Data Recovery (CDR) IC. The existing timing endpoint firmware was ported over to the AFC, and the following operations were successfully tested.

- IPBus communication over Ethernet (routed via the crate controller) with the AFC FPGA
- establishment of stable downlink between timing master and endpoint, i.e. successful transmission of commands and timestamp from master to endpoint
- establishment of stable uplink between timing master and endpoint, i.e. successful transmission of commands from endpoint to master

3 Functionality tests

This section describes tests which were performed using the hardware developed for the ProtoDUNE-SP Run I timing system. Performing these tests with the ProtoDUNE-SP Run I hardware serves to inform and refine the test procedure for the eventual tests with DTS-SP hardware. The setup for these tests consists of a timing master unit, physically realised using an AIDA 2020 TLU [1]. The master unit generates the 50 MHz (frequency used at ProtoDUNE-SP Run I) clock and timestamp, and encodes them in a 8b/10b data-stream, which is clocked at 250 MHz. The data-stream is sent to two endpoints using single-mode optical fibres, and a passive optical splitter. One endpoint was connected to the optical splitter with a 2 m fibre, whereas the other used a 120 m fibre. The endpoint connected with the 2 m fibre will be referred to as "endpoint 1", whereas the 120m fibre endpoint will be referred to as "endpoint 2". The endpoint hardware consist of a timing FMC hosted by an Enclustra base board (PM3), with an AX3 FPGA module.

3.1 Fixed-length message synchronisation

A modified firmware version of the endpoint firmware was used for this test, where an electrical pulse is emitted at the receipt of a particular timing command. The time difference between the two pulses was measured before and after the endpoints were aligned. The alignment procedure consisted of applying a delay to the endpoint with the shorter fibre, so that timing commands from

the master reach the two endpoints at the same time. In the current version of the firmware, the delay can be applied in units of 50 MHz clock ticks, i.e. 20 ns.

The time difference between the pulses emitted from the endpoints, before they were aligned was measured to be 579 ns, see figure 1. This is consistent with a path length difference of 118 m, as 1 m of fibre introduces approximately 4.9 ns of delay, $118 * 4.9 = 578.2$ ns.

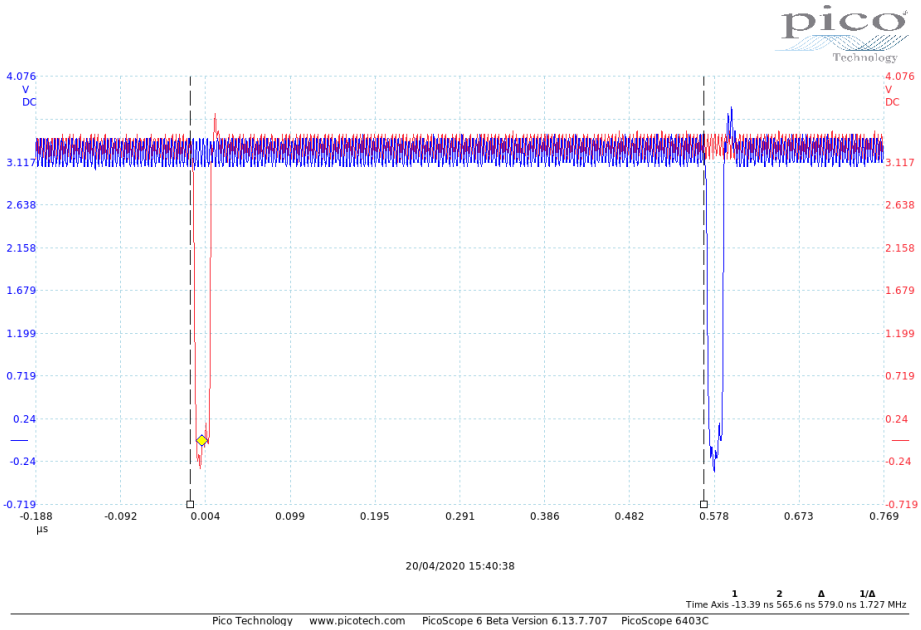

Figure 1: A screenshot of the oscilloscope output showing the arrival time of the two electrical pulses from the two unaligned endpoints. The red signal is from endpoint 1, and the blue signal from endpoint 2.

To align the endpoints, a delay of 28 clock ticks, i.e. 580 ns, was applied to endpoint 1. The time difference between the pulses with the delay applied was measured to be 19 ns, as would be expected, see figure 2.

The firmware which will be developed for DTS-SP will be capable of finer-grain delay adjustment, where delays will be applied in ticks of the 62.5 MHz (the DUNE clock frequency) clock, as well as in ticks of the IO clock, which runs at 312.5 MHz.

3.2 Endpoint clock charecterisation

The synchronisation of timestamp and fixed-length messages between endpoints relies on the clock edges at endpoints being aligned, as well as the overall effective path length. The alignment of the clocks coming from the two endpoints were studied, where the difference in arrival time of the clock edges and cycle-to-cycle jitter were studied. The time difference between clock edges from the two endpoints was found to have a mean of 0.802 ns, and a standard deviation of 0.140 ns. A plot of the clock edges data is shown in figure 3.

Another factor which affects endpoint synchronisation is the cycle-to-cycle jitter of the clock used

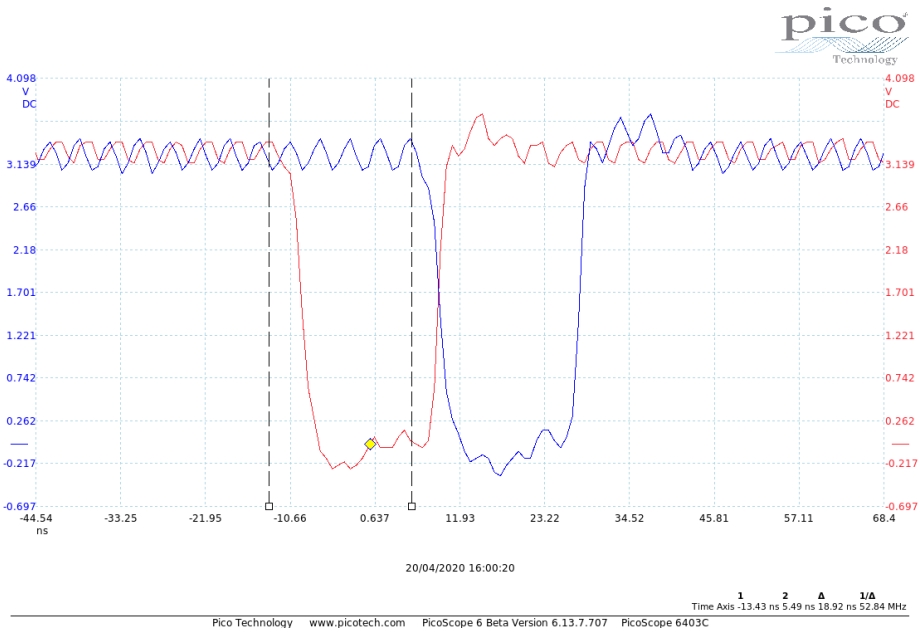

Figure 2: A screenshot of the oscilloscope output showing the arrival time of the two electrical pulses from the two aligned endpoints. The red signal is from endpoint 1, and the blue signal from endpoint 2.

to increment the timestamp at the endpoints. Figure 4 shows the difference between consecutive clock periods, where the mean and standard deviation were found to be -0.019 ns and 0.155 ns respectively.

4 Conclusion

These preliminary tests demonstrate a part of the capability and performance which will be required from the DTS-SP in its role of synchronising components of the DUNE DAQ.

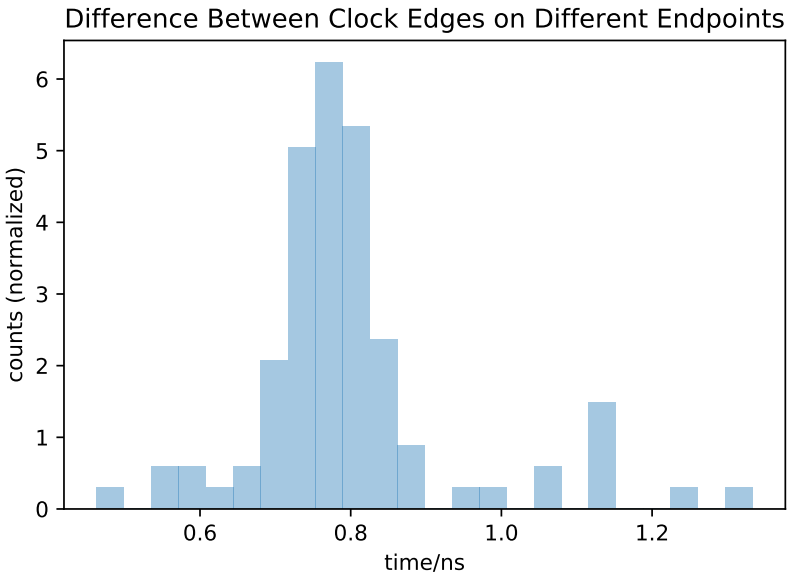

Figure 3: A plot of the difference in arrival time of the clock edges from the two endpoints.

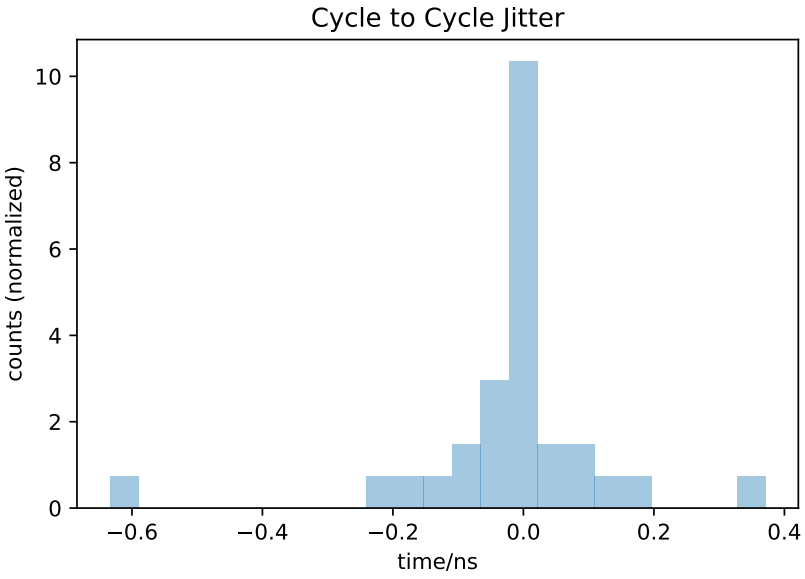

Figure 4: A plot of the difference of consecutive clock periods.

Glossary

AMC FMC Carrier (AFC) Holds digitizing electronics and lives in μTCA crates. 1, 2

advanced mezzanine card (AMC) Holds digitizing electronics and lives in μTCA crates. 1, 6

Fibre Interface Board (FIB) interface to the timing endpoints. 1

FPGA Mezzanine Card (FMC) An ANSI/VITA (VMEbus International Trade Association) 57.1 standard that defines I/O mezzanine modules with connection to an FPGA. Can be plugged into an AMC. 1, 2

Intelligent Platform Management Interface (IPMI) A set of computer interface specifications for an autonomous computer subsystem management and monitoring. 2

Small Form-Factor Pluggable (SFP) A hot-pluggable transceiver for carrying Gigabit/s serial signals. The transport medium is usually an optical fiber. 2

DUNE Timing System-Single Phase (DTS-SP) A timing and synchronization system which will be developed and deployed at ProtoDUNE SP II, and eventually DUNE. It will distribute clock and synchronisations signal to SP detector modules only.. 1–4

Single-Phase (SP) Distinguishes one of the DUNE far detector technologies by the fact that it operates using argon in its liquid phase only . 1, 2

Micro Telecommunications Computing Architecture (μTCA) The computer architecture specification followed by the crates that house charge and light readout electronics in the dual-phase module. 1, 2, 6

References

[1] P. Baesso, D. Cussans, and J. Goldstein. "The AIDA-2020 TLU: a flexible trigger logic unit for test beam facilities". In: *JINST* 14.09 (2019), P09019. DOI: 10.1088/1748-0221/14/09/P09019. arXiv: 2005.00310 [physics.ins-det].

[2] Brazilian Synchrotron Light Laboratory and Warsaw University of Technology. *AMC FMC Carrier (AFC)*. https://www.ohwr.org/project/afc/wikis/home.

[3] J. Brooke et al. *DUNE Timing System-Single Phase Design*. EDMS doc 2209895 v.2. URL: https://edms.cern.ch/document/2209895/2.