Tackle the scaling challenges with CMOS in beyond ton-scale 0νββ experiments

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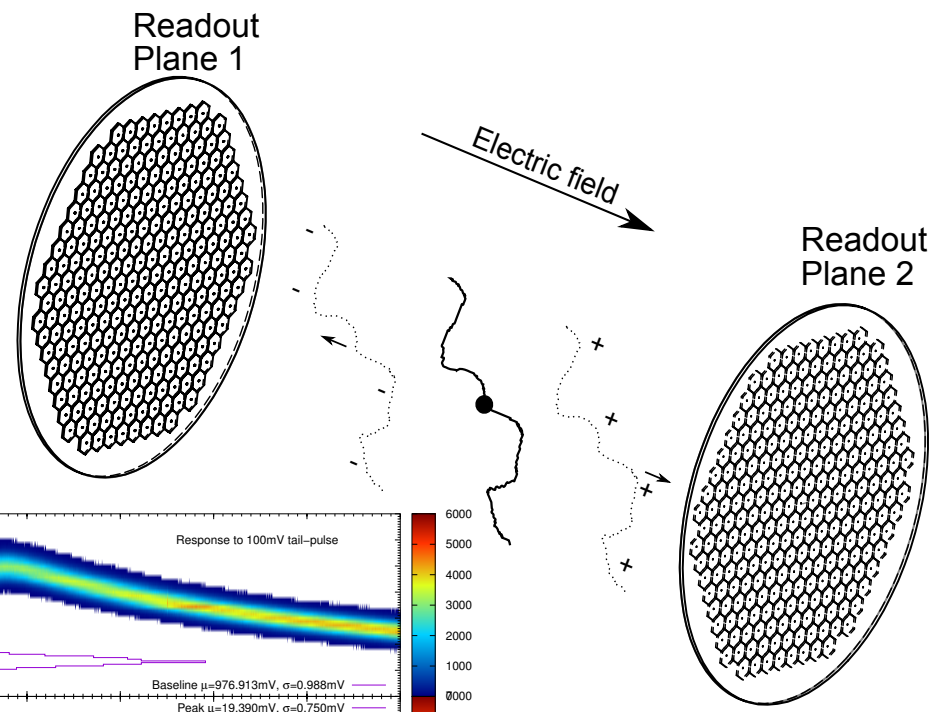
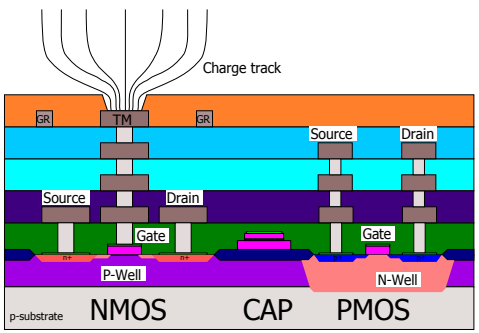
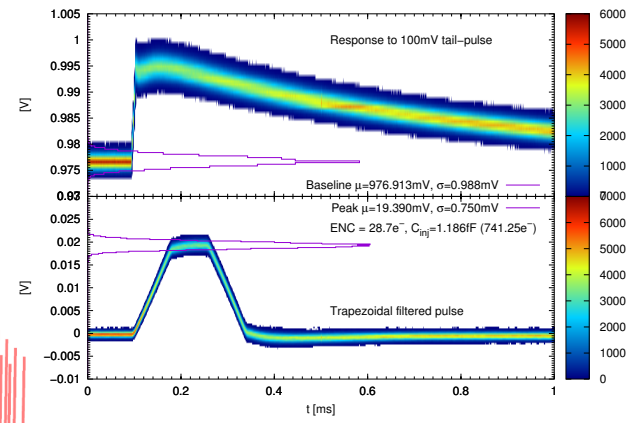
CMOS charge sensor array for TPC

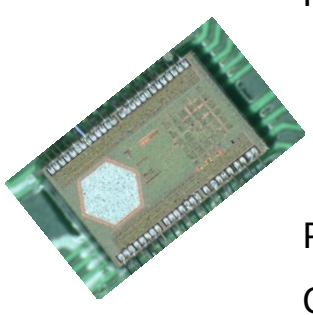
- Scaling up to larger size while keeping spatial resolution means drastic increase in channel number
- With or without charge multiplication, or SiPM array
- Fill the plane with CMOS sensor
- Use bonding pad for charge collection
- Amplify and digitize on the spot
- CMOS sensors talk to neighbors to form a network
- In-chip regulation of power, eliminating external components (reduce radioactivity)
- Economy of scale: leverage standard industrial processes

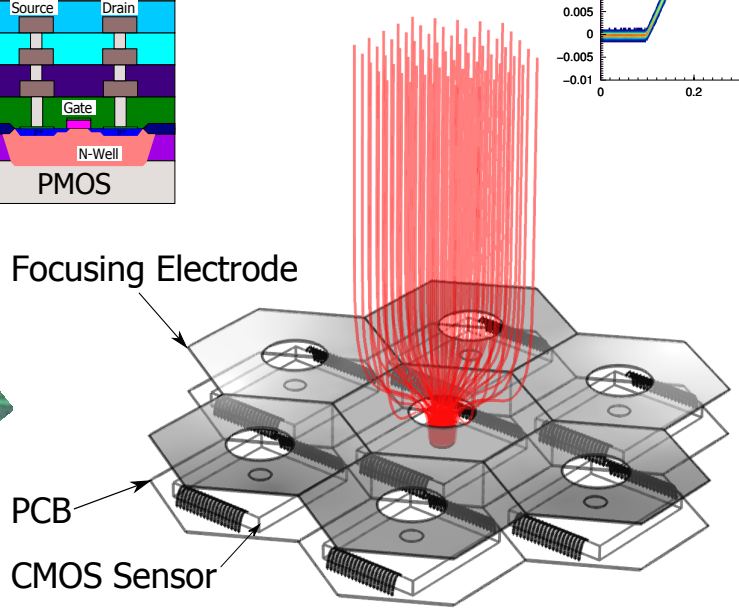


Topmetal sensor project(s)





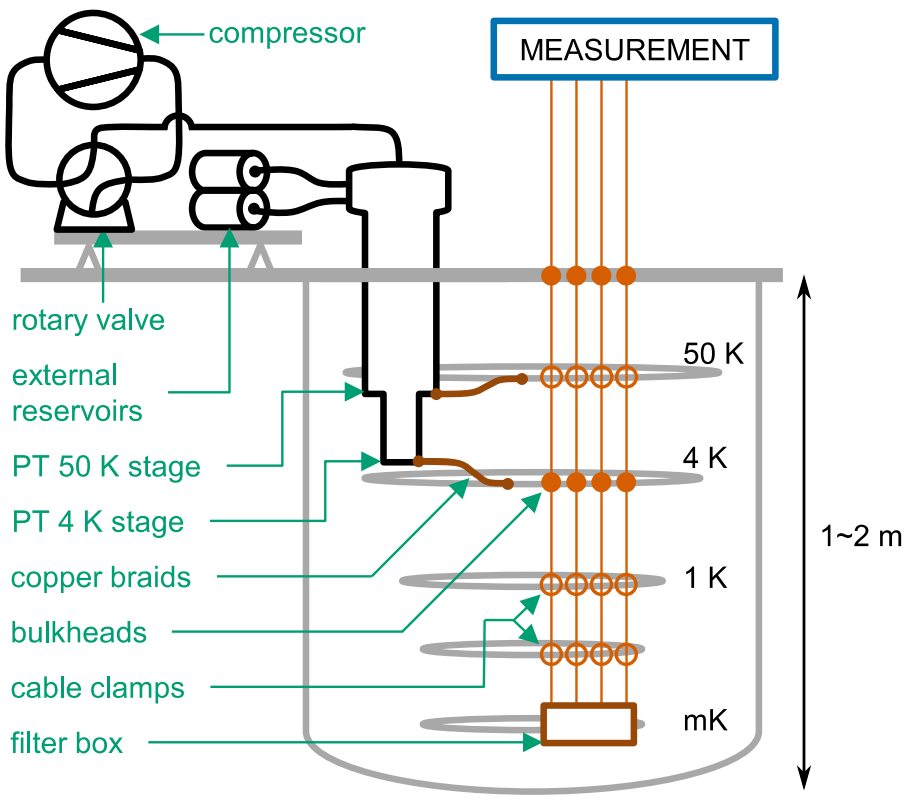




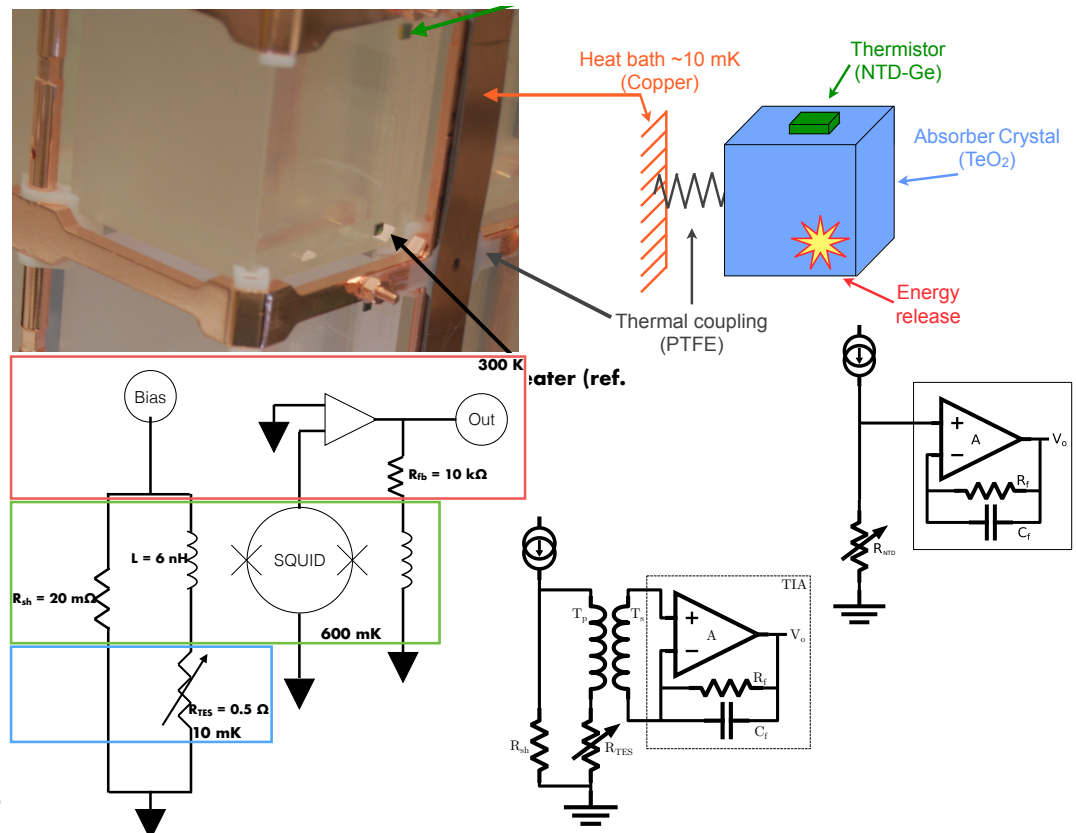
- LBNL LDRD funded (FY16,17)
- <30e- noise per pixel (CMOS electrical test)
- Should reach 1% FWHM without charge multiplication
- In-gas validation in (slow) progress
- Can detect drifting ions directly. May enable $^{82}SeF_6$ as a detector medium

D.R. Nygren 2007 J. Phys.: Conf. Ser. 65 012021
M. An et al 2016 NIMA 810, 144
D.R. Nygren et al 2018 JINST 13 P03015
Y. Mei et al arXiv:2010.09226

Deep cryogenic CMOS



NTD, TES in CUORE/CUPID, cryogenic sensors in general



Problem: at scale, it is highly undesirable to run thousands or more wires, meters long, from T_{room} to T_{mK}

- Trouble with heat load and feedthroughs.
- Noise and interference.
- Sheer complexity.

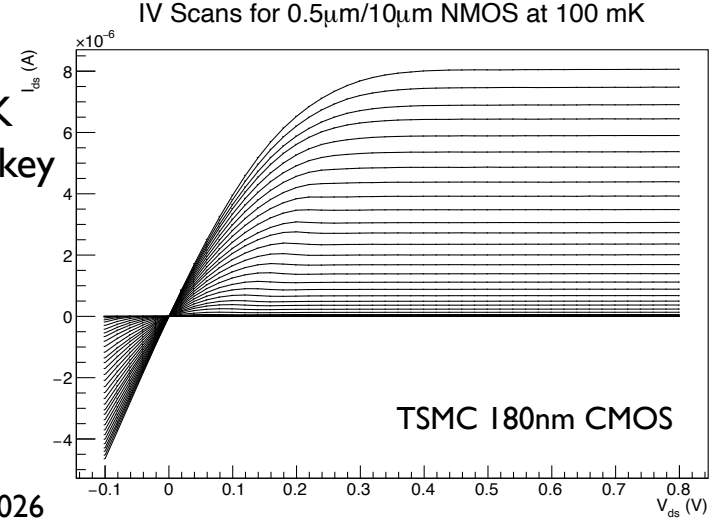
Solution: electronics (CMOS) at 4K, 1K or below, as close as possible to the sensors.

- Amplify and transform impedance as early as possible
- Multiplex or digitize early, reduce the number of lines.
- Actively drive the cables.

This is a common solution for many deep cryogenic detector systems.

- LBNL LDRD funded (FY20,21)
- Basic devices work down to mK
- Extremely low power design is key

IV Scans for 0.5μm/10μm NMOS at 100 mK



R.G. Huang et al 2020 JINST 15 P06026