Evaluation of phase 2 and 4. 8 Gbps phase1 testing

DUNE Upstream DAQ Firmware

Alessandro Palombi

EP-DT
Detector Technologies

Evaluation of phase 2 master

- Register map rm-5.0 is **matched** with phase2/master firmware registers
- Fifo memory implemented in CRToHostdm.vhd is **suitable** for 4 KB Blocks
- JBSC logic has been **implemented** by Frans
  - Same logic as phase1 but it uses **EnableTlast** instead of ChunkEnable signal
- **Succesfully** tested phase2 (rm5.0) firmware with and without JBSC
  - The main software tools are provided also in a version supporting rm5.0

4.8 Gb/s version of phase 1 master

- **Changes** branching out from the atlas-tdaq-felix master are **based** on **wwulf/48g-fullmode** branch

- Loopback test in BNL712
  - BNL712 correctly **transmits** and **receives** data at **4.8 Gb/s**

- Test BNL712 ➡ VC709
  - **BNL712** with emulator **transmits** data to VC709 at **4.8 Gb/s**
  - **VC709 receives** correctly data at **4.8 Gb/s**
  - Investigating on VC709 links alignment stability

- Branch of the 4.8 Gb/s version manageable by generics
  - Branch updated to master with IP for **Vivado 2020.1** version
  - **FULL_HALFRATE** generic allows us to **configure** RX data rate both for **BNL712** and **VC709** cards
  - https://gitlab.cern.ch/DUNE-SP-TDR-DAQ/felix/firmware/-/tree/updateformerge/48Gbps

Next steps…

- **Integration** of 4.8 Gb/s work in **phase 2** master firmware
  - We will do in phase 2 the **same changes** made in phase 1
  - Integration of the **emulator** only for test
  - Same **tests** made for phase 1

THANKS