CPAD 2021
READOUT & ASICS PLENARY

MITCH & GABRIELLA

MARCH 22, 2021

RELATING TO ELECTRONICS & ASICS BASIC RESEARCH NEEDS

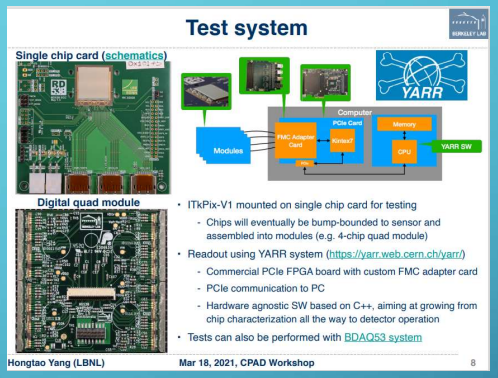
Priority Research Directions	Thrusts	Technical Requirements
PRD 16: Evaluate process technology and develop models for ASICs in extreme environments	Develop models, standard cell libraries, and demonstrators for extreme rate and radiation; Develop models, standard cell libraries, and demonstrators for intermediate cryogenic range: Develop models, standard cell libraries, and demonstrators for quantum sensor controls and data acquisition for deep cryogenic range; Investigate emerging design and verification methodologies; Investigate CMOS with integrated photonics nodes when commercially available; Investigate processes with Internet of Things (IoT) technology to enable self-assembly or assembly-free very large scale detectors; Adopt Artificial Intelligence (AI) and Machine Learning (ML) techniques	TR 1.1, TR 1.2, TR 3.47, TR 5.3, TR 5.6, TR 5.8, TR 5.11
PRD 17: Create building blocks for Systems-on-Chip for extreme environments	Develop advanced low power high speed I/O protocols; Develop wireless blocks beginning with control and monitoring; Develop power management blocks (DC/DC) converters, regulators, pulsed power; Circuit development for monolithic designs with sensor and readout integrated (MAPS, SPADs, SiPM); Develop Single Event Effects flows and techniques relevant for new technologies; Develop analog and multiplexing blocks for 4K environments and below; Develop fault tolerant communications for long lifetime inaccessible readout; Develop precision clock and timing circuits (PLL, DLL, Timing Discriminators, Delay Lines, Picosecond TDCs); Develop multi-channel RF digitizers	TR 1.5, TR 2.1, TR 2.3- 2.5, TR 2.6- 2.7, TR 4.3- 4.4, TR 5.3,TR 5.6, TR 5.8,TR 5.11

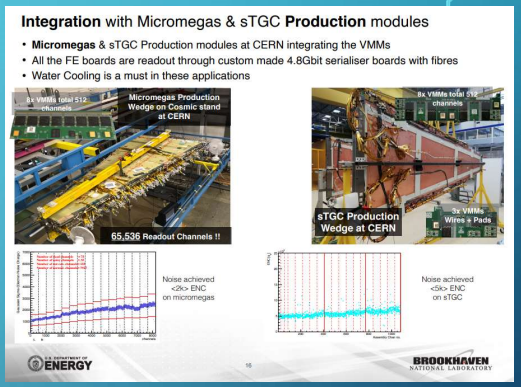
THURSDAY - 8 PRESENTATIONS IN TWO SESSIONS

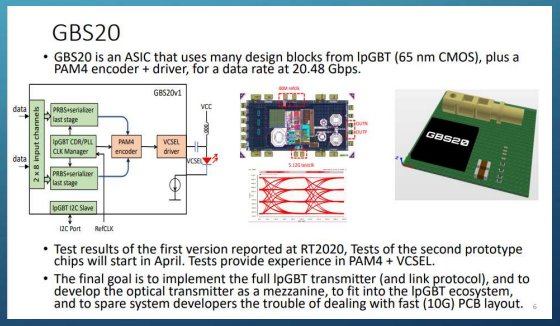
Session I 4 talks covering primarily LHC related efforts

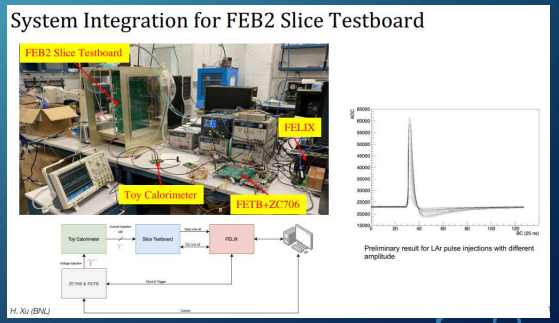
- George Iakovidis (BNL) : "The VMM ASIC - From R&D to production" ATLAS Muon system
- Hongtao Yang (LBNL): "Characterization of ITkPix-V1 pixel readout chip" a manifestation of the CERN RD53 group effort.
- Hao Xu (BNL) : "Design and Integration of the Readout Electronics for ATLAS Liquid Argon Calorimeter for HL-LHC"
- Jingbo Ye (SMU): "R&Ds of ASICs and Optical Modules for Detector Data Communication"

A look to the future of High Speed Readout using the CERN LHC developments as a springboard





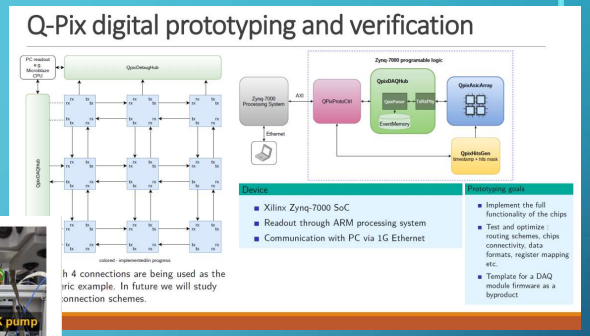


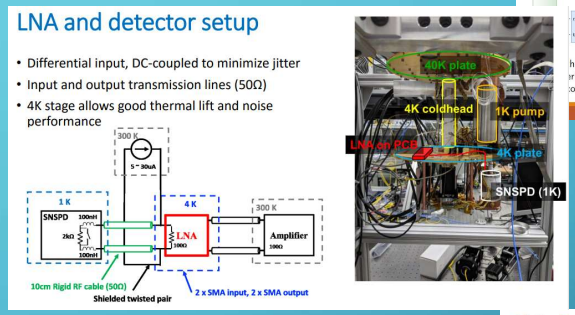


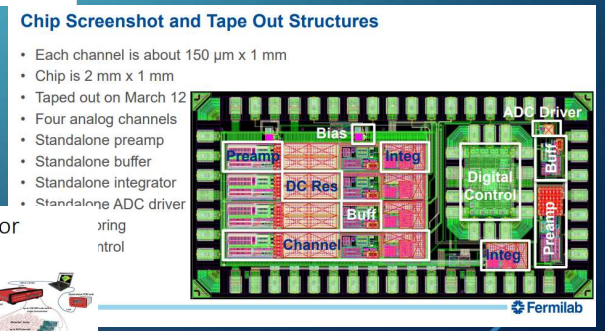
THURSDAY - 8 PRESENTATIONS IN TWO SESSIONS

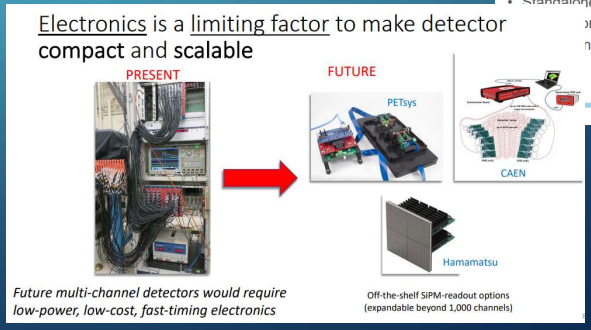
Session II - 4 talks

- Gang Liu (U Hawaii): "The QPIx pixelated readout concept for future Liquid Argon Time Projection Chambers: status and prospects."
- Davide Braga (FNAL): "Low noise, low jitter cryogenic amplifier for superconducting nanowire detectors."
- Troy England (FNAL): "A scalable low-noise skipper-CCD readout ASIC in 65 nm LP CMOS."
- Viacheslav Li (LLNL): "Towards scalable fast-neutron and reactor-antineutrino detectors based on 6Li-doped PSD plastic scintillators and SiPM arrays."



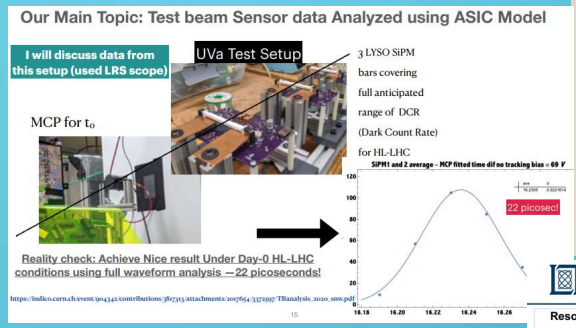


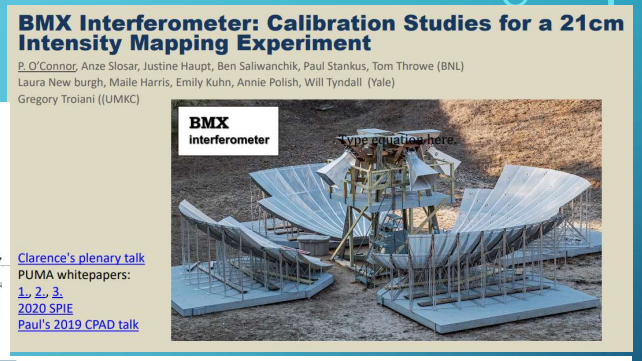


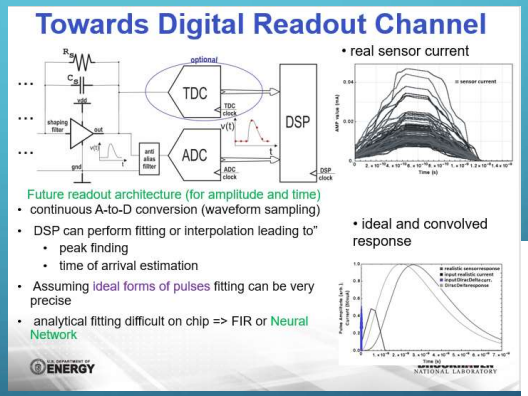


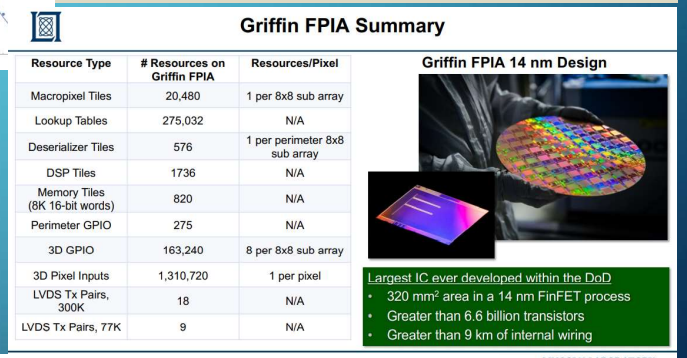
FRIDAY - 5 PRESENTATIONS & ROUNDTABLE

- Paul O'Connor (BNL): “First Observations with the BMX 21cm Intensity Mapping Pathfinder.”
- Sebasatian White (UVa): “Testing Virtual ASICs with Real Data: an Example from CMS timing upgrade.”
- Richard Younger (MIT-LL): “Multi-use advanced digital readouts using 3D stacking Applications.”
- Sandeep Miryala (BNL): “Towards Edge Computing: Co-Design for Machine Learning based ASICs for Scientific Applications.”
- James Hirschauer (FNAL): “A reconfigurable neural network ASIC for detector front-end data compression at the HL-LHC.”

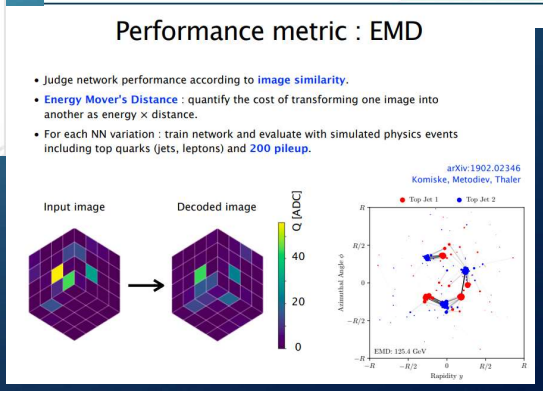








Resource Type	# Resources on Griffin FPIA	Resources/Pixel
Macropixel Tiles	20,480	1 per 8x8 sub array
Lookup Tables	275,032	N/A
Deserializer Tiles	576	1 per perimeter 8x8 sub array
DSP Tiles	1736	N/A
Memory Tiles (8K 16-bit words)	820	N/A
Perimeter GPIO	275	N/A
3D GPIO	163,240	8 per 8x8 sub array
3D Pixel Inputs	1,310,720	1 per pixel
LVDS Tx Pairs, 300K	18	N/A
LVDS Tx Pairs, 77K	9	N/A



FRIDAY SESSION II -- COMMUNITY DISCUSSION
IN THE CONTEXT OF THE BASIC RESEARCH NEEDS OBJECTIVES

- Recognition that after many years of seeking funding agency support for Instrumentation Careers there appears to be movement with new legislation being considered by congress.
- It may be interesting to pursue US foundries (e.g. Skywater) for future projects but we should not forget the huge benefit of implementing innovative HEP circuit & logic based-designs with commercially vetted design kits (PDK's).
- Observed (once again) that *CERN's* open acceptance and support for member participants in R&D programs and multi-user agreements as well as a similar attitude from *Europractice* have been highly beneficial for the US HEP community.
  - The European model provides Bureaucratic support with a dedicated work force interact with foundries or their representatives, support user PDK's and multi-user agreements as well as community training. This benefits the global scientific community.
- On technology
  - Continue to evaluate commercial off-the-shelf (COTS) components for radiation tolerance (e.g. wireless).
  - Continue evaluation of opportunities and model of engagement with foundries for adopting new technologies (e.g. 3D, interconnects, memristors, etc.).
  - Continue to explore new circuits for low power implementation.