



# CPAD 2021 READOUT & ASICS PLENARY

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MARCH 22, 2021

# RELATING TO ELECTRONICS & ASICS BASIC RESEARCH NEEDS

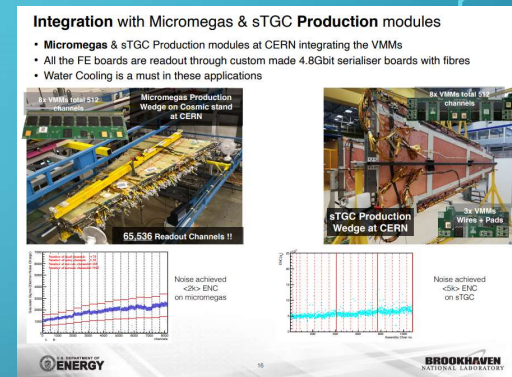
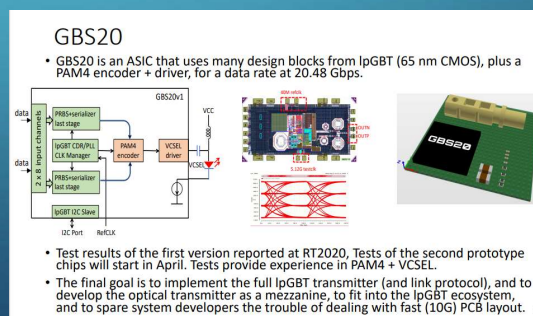
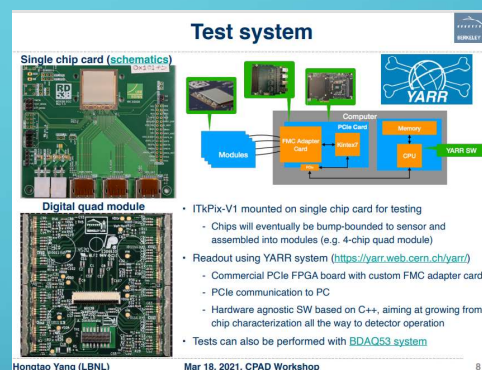
Priority Research Directions	Thrusts	Technical Requirements
<p><b>PRD 16:</b> Evaluate process technology and develop models for ASICs in extreme environments</p>	<p>Develop models, standard cell libraries, and demonstrators for extreme rate and radiation;            Develop models, standard cell libraries, and demonstrators for intermediate cryogenic range;            Develop models, standard cell libraries, and demonstrators for quantum sensor controls and data acquisition for deep cryogenic range;            Investigate emerging design and verification methodologies;            Investigate CMOS with integrated photonics nodes when commercially available;            Investigate processes with Internet of Things (IoT) technology to enable self-assembly or assembly-free very large scale detectors;            Adopt Artificial Intelligence (AI) and Machine Learning (ML) techniques</p>	<p>TR 1.1, TR 1.2, TR 3.47, TR 5.3, TR 5.6, TR 5.8, TR 5.11</p>
<p><b>PRD 17:</b> Create building blocks for Systems-on-Chip for extreme environments</p>	<p>Develop advanced low power high speed I/O protocols;            Develop wireless blocks beginning with control and monitoring;            Develop power management blocks (DC/DC) converters, regulators, pulsed power;            Circuit development for monolithic designs with sensor and readout integrated (MAPS, SPADs, SiPM);            Develop Single Event Effects flows and techniques relevant for new technologies;            Develop analog and multiplexing blocks for 4K environments and below;            Develop fault tolerant communications for long lifetime inaccessible readout;            Develop precision clock and timing circuits (PLL, DLL, Timing Discriminators, Delay Lines, Picosecond TDCs);            Develop multi-channel RF digitizers</p>	<p>TR 1.5, TR 2.1, TR 2.3- 2.5, TR 2.6- 2.7, TR 4.3- 4.4, TR 5.3, TR 5.6, TR 5.8, TR 5.11</p>

# THURSDAY - 8 PRESENTATIONS IN TWO SESSIONS

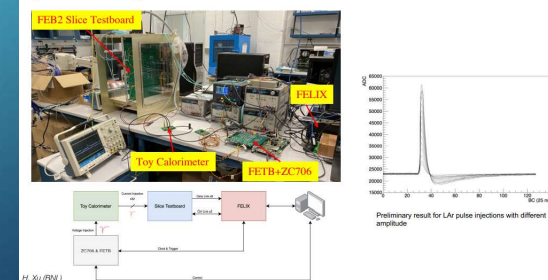
## Session I 4 talks covering primarily LHC related efforts

- George Iakovidis (BNL) : “The VMM ASIC - From R&D to production” ATLAS Muon system
- Hongtao Yang (LBNL): “Characterization of ITkPix-V1 pixel readout chip” a manifestation of the CERN RD53 group effort.
- Hao Xu (BNL) : “Design and Integration of the Readout Electronics for ATLAS Liquid Argon Calorimeter for HL-LHC”
- Jingbo Ye (SMU): “R&Ds of ASICs and Optical Modules for Detector Data Communication”

A look to the future of High Speed Readout using the CERN LHC developments as a springboard



## System Integration for FEB2 Slice Testboard





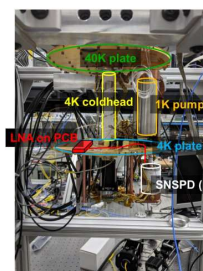
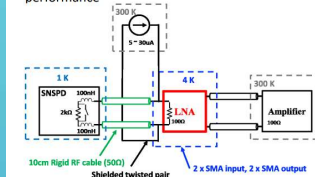
# THURSDAY - 8 PRESENTATIONS IN TWO SESSIONS

## Session II - 4 talks

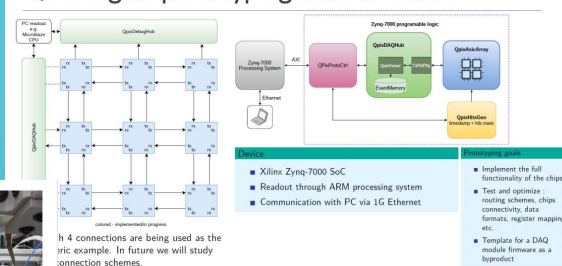
- Gang Liu (U Hawaii): “The QPix pixelated readout concept for future Liquid Argon Time Projection Chambers: status and prospects.”
- Davide Braga (FNAL): “Low noise, low jitter cryogenic amplifier for superconducting nanowire detectors.”
- Troy England (FNAL): “A scalable low-noise skipper-CCD readout ASIC in 65 nm LP CMOS.”
- Viacheslav Li (LLNL): “Towards scalable fast-neutron and reactor-antineutrino detectors based on  $^6\text{Li}$ -doped PSD plastic scintillators and SiPM arrays.”

### LNA and detector setup

- Differential input, DC-coupled to minimize jitter
- Input and output transmission lines (50Ω)
- 4K stage allows good thermal lift and noise performance

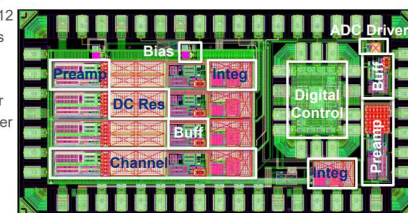


### Q-Pix digital prototyping and verification

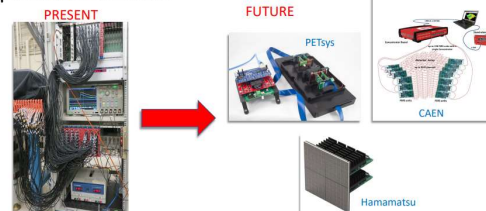


### Chip Screenshot and Tape Out Structures

- Each channel is about  $150 \mu\text{m} \times 1 \text{ mm}$
- Chip is  $2 \text{ mm} \times 1 \text{ mm}$
- Taped out on March 12
- Four analog channels
- Standalone preamp
- Standalone buffer
- Standalone integrator
- Standalone ADC driver



### Electronics is a limiting factor to make detector compact and scalable



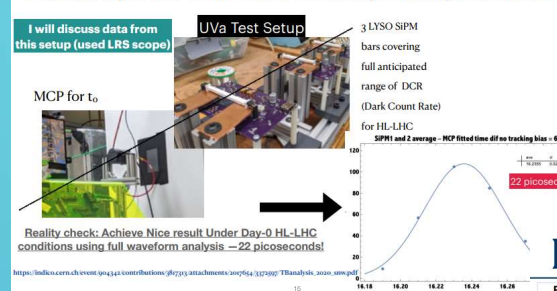
Future multi-channel detectors would require low-power, low-cost, fast-timing electronics

Off-the-shelf SiPM-readout options (expandable beyond 1,000 channels)

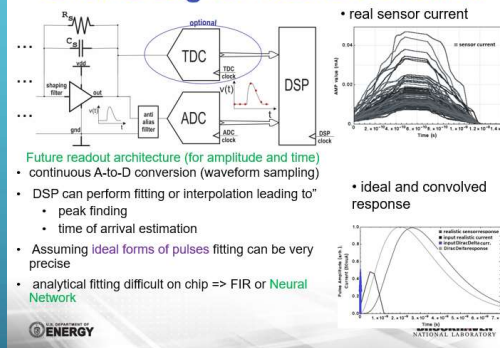
# FRIDAY - 5 PRESENTATIONS & ROUNDTABLE

- Paul O'Connor (BNL): "First Observations with the BMX 21cm Intensity Mapping Pathfinder."
- Sebastian White (UVA): "Testing Virtual ASICs with Real Data: an Example from CMS timing upgrade."
- Richard Younger (MIT-LL): "Multi-use advanced digital readouts using 3D stacking Applications."
- Sandeep Miryala (BNL): "Towards Edge Computing: Co-Design for Machine Learning based ASICs for Scientific Applications."
- James Hirschauer (FNAL): "A reconfigurable neural network ASIC for detector front-end data compression at the HL-LHC."

## Our Main Topic: Test beam Sensor data Analyzed using ASIC Model



## Towards Digital Readout Channel



## BMX Interferometer: Calibration Studies for a 21cm Intensity Mapping Experiment

P. O'Connor, Anze Slosar, Justine Haupt, Ben Saliwanchik, Paul Stankus, Tom Throwe (BNL)  
Laura Newburgh, Maile Harris, Emily Kuhn, Annie Polish, Will Tyndall (Yale)  
Gregory Troiani (UMKC)

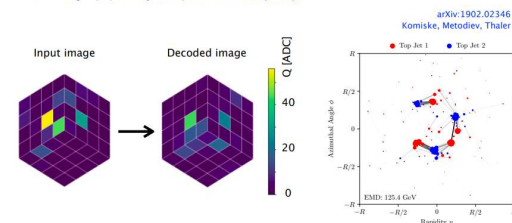


## Griffin FPIA Summary

Resource Type	# Resources on Griffin FPIA	Resources/Pixel	Griffin FPIA 14 nm Design
Macropixel Tiles	20,480	1 per 8x8 sub array	<p>Largest IC ever developed within the DoD</p> <ul style="list-style-type: none"> <li>• 320 mm<sup>2</sup> area in a 14 nm FinFET process</li> <li>• Greater than 6.6 billion transistors</li> <li>• Greater than 9 km of internal wiring</li> </ul>
Lookup Tables	275,032	N/A	
Deserializer Tiles	576	1 per perimeter 8x8 sub array	
DSP Tiles	1736	N/A	
Memory Tiles (8K 16-bit words)	820	N/A	
Perimeter GPIO	275	N/A	
3D GPIO	163,240	8 per 8x8 sub array	
3D Pixel Inputs	1,310,720	1 per pixel	
LVDS Tx Pairs, 300K	18	N/A	
LVDS Tx Pairs, 77K	9	N/A	

## Performance metric : EMD

- Judge network performance according to **image similarity**.
- **Energy Mover's Distance** : quantify the cost of transforming one image into another as energy x distance.
- For each NN variation : train network and evaluate with simulated physics events including top quarks (jets, leptons) and **200 pileup**.



## FRIDAY SESSION II -- COMMUNITY DISCUSSION IN THE CONTEXT OF THE BASIC RESEARCH NEEDS OBJECTIVES

- Recognition that after many years of seeking funding agency support for Instrumentation Careers there appears to be movement with new legislation being considered by congress.
- It may be interesting to pursue US foundries (e.g. Skywater) for future projects but we should not forget the huge benefit of implementing innovative HEP circuit & logic based-designs with commercially vetted design kits (PDK's).
- Observed (once again) that CERN's open acceptance and support for member participants in R&D programs and multi-user agreements as well as a similar attitude from *Euopractice* have been highly beneficial for the US HEP community.
  - The European model provides Bureaucratic support with a dedicated work force interact with foundries or their representatives, support user PDK's and multi-user agreements as well as community training. This benefits the global scientific community.
- On technology
  - Continue to evaluate commercial off-the-shelf (COTS) components for radiation tolerance (e.g. wireless).
  - Continue evaluation of opportunities and model of engagement with foundries for adopting new technologies (e.g. 3D, interconnects, memristors, etc.).
  - Continue to explore new circuits for low power implementation.