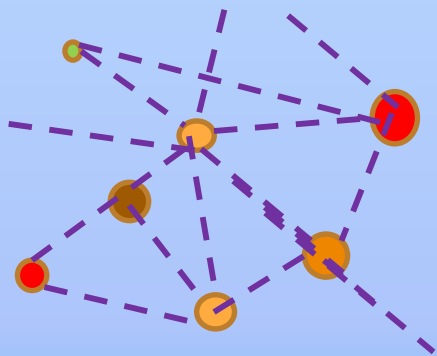




# **Integration of Squid/Memristor Neurons with Precision Space and Time Particle Physics Detectors for 4D Image Reconstruction using Neuromorphic Computing**

**Alice Bean, Hao Li, Nicola Minafra, Chris Rogan, Judy Wu**  
University of Kansas

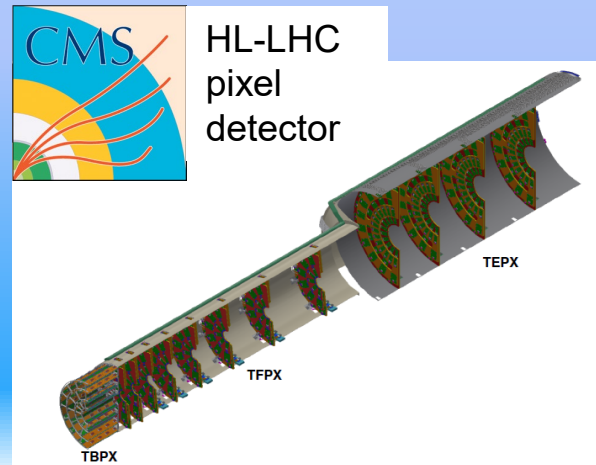
# Neuromorphic computing (NC) could tackle Tracking Challenges



## NC Emulates human brain

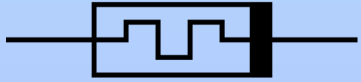
- Memory and computing elements aren't separated
- Neurons communicate in parallel architecture

- Challenge: HL-LHC CMS pixel detector  
- 2 billion readout channels!

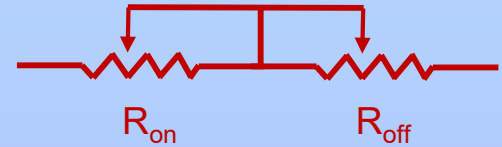




# Neuron System Development



- MEMRISTOR: resistor with memory
- passive device with a state (on/off)
  - non-volatile
  - adjustable resistance
  - Can act as logic gate as well

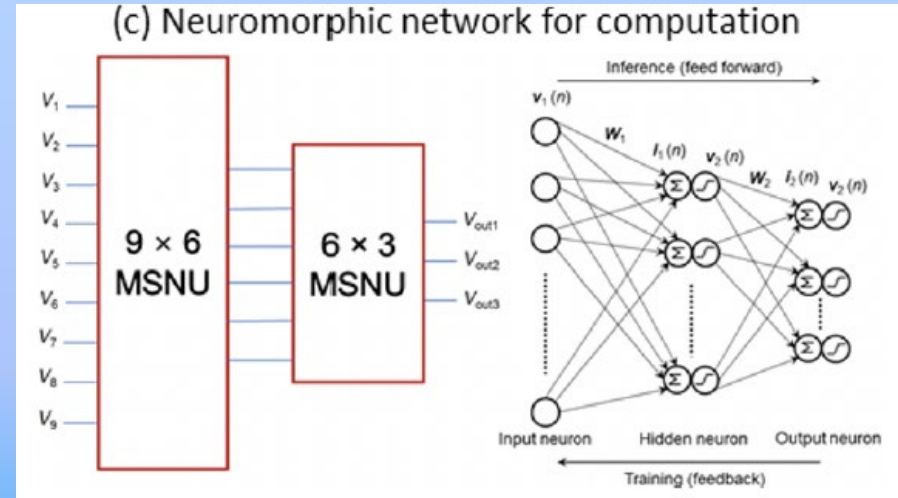


- Report from DOE Office of Science 2015
- [https://science.osti.gov/-/media/ascr/pdf/programdocuments/docs/Neuromorphic-Computing-Report\\_FNLBLP.pdf](https://science.osti.gov/-/media/ascr/pdf/programdocuments/docs/Neuromorphic-Computing-Report_FNLBLP.pdf)
- Intel has 8M neuron system (100M soon) with 64 Loihi 14nm chip
- <https://spectrum.ieee.org/tech-talk/robotics/artificial-intelligence/intels-neuromorphic-system-hits-8-million-neurons-100-million-coming-by-2020.amp.html>
- Present applications use CMOS technology (2D)

Possibility of petabits/cm<sup>2</sup>

# Neuromorphic Computing Readout Electronics

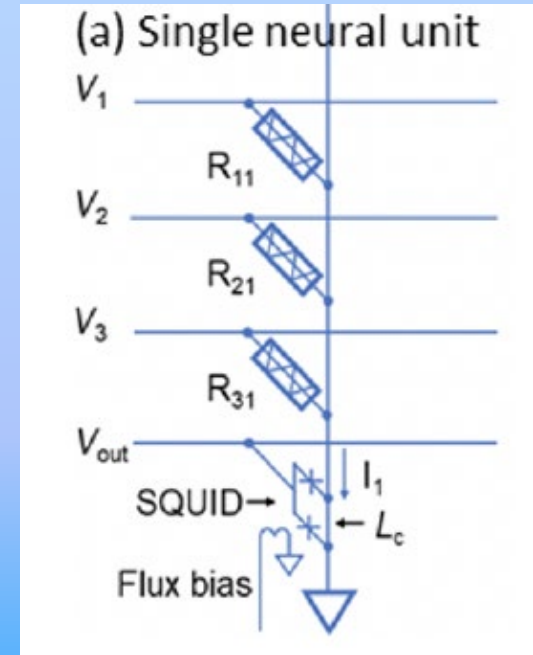
- Downstream implementation of Deep Neural Networks is available already as part of Neuromorphic Computing
- Layout architecture more flexible
- Can add **temporal characteristics** to implement Spiking Neural Network





# KU CMP group NC development

- Atomically tunable **memristors** with superconductor electrodes paired with Superconducting **SQUID** for neuronal units
  - IP disclosure filed
- SQUID has  $1 \text{ pA/Hz}^{1/2}$  reading out  $0.1 \mu\text{A}$  signal in  $0.1 \text{ ns}$
- Reduced power from  $\sim N \times N$  to  $\sim N$  for  $N(\text{row}) \times N(\text{column})$  network of NC circuit, **3D scalability**
- Logic gates can be implemented



# Timing detectors: LGADs

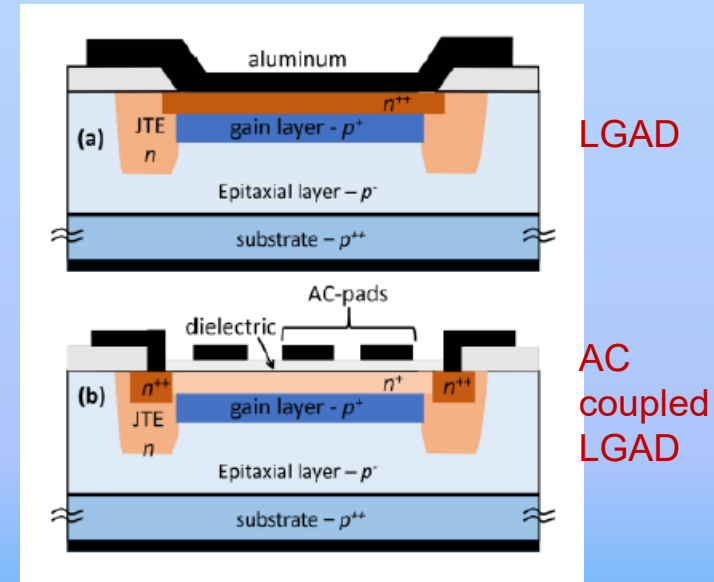
AC coupling: remove pixilation and add  $n^+$  implant, di-electric layer, as well as AC coupling to readout pads

Expected 100% fill factor gives fast timing per pixel (now  $\sim 30\text{ps}$ ), and spatial resolution (currently  $\sim 50\mu\text{m}$  spatial)

- sparse readout at lower power

Charge is shared between multiple pads  
cross talk is expected

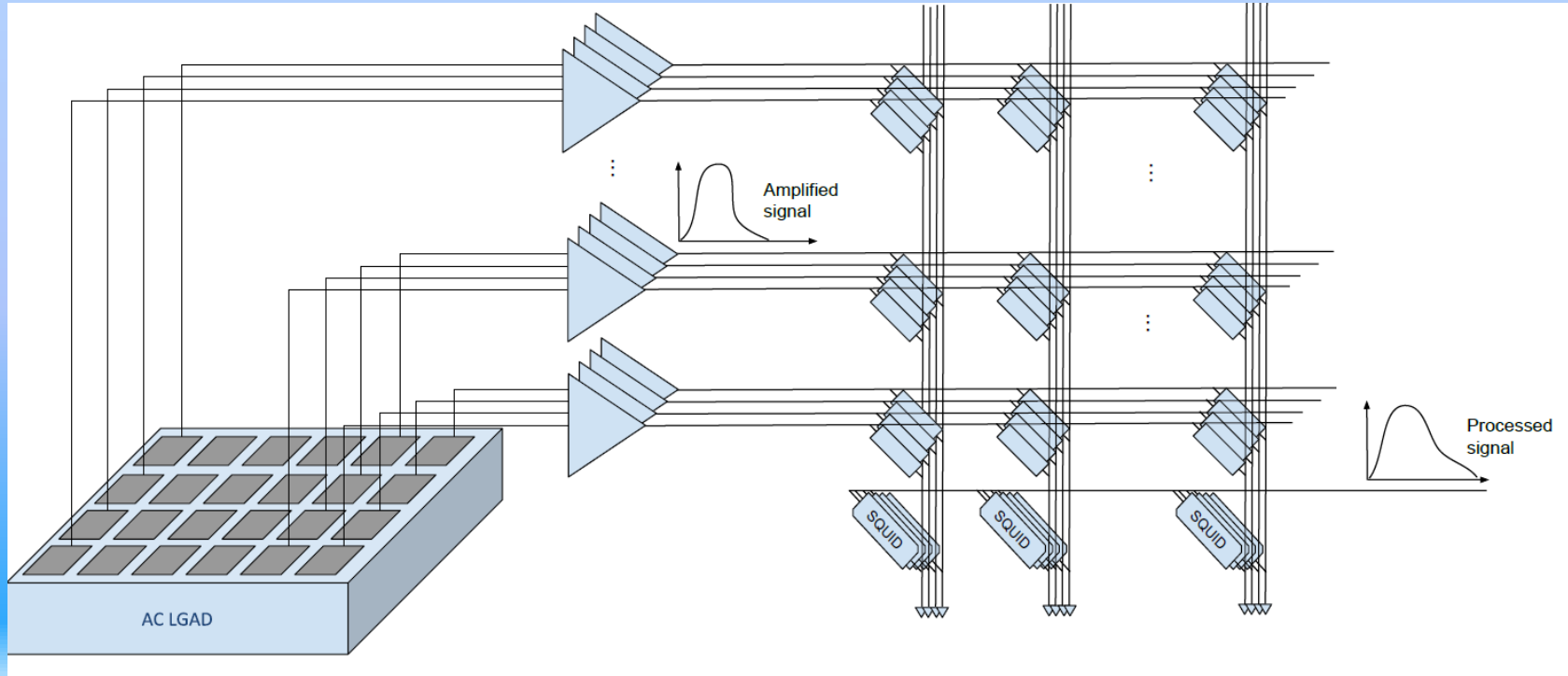
Need new readout to exploit this property



G. Giacomini, W. Chen, G. D'Amen, and A. Tricoli, Journal of Instrumentation 14 no. 09 (Sept 2019) P09004.




# Make Cross Talk work for you - Processing intrinsic to readout electronics

- Essentially you have an analog readout





# Integrate NC backend with AC LGAD

- Hardware exists now to start:  
CMOS NC units commercially available  Superconducting NC at KU
- Need new algorithms to exploit 4D spatial and temporal info  
Deep Neural Network  Spiking Neural Network
- Future promises:  
better usage of analog signals  **LESS POWER**