Integration of mini TECs on the CMS MTD barrel timing layer 16 ch SiPM array to reduce the DCR after very high irradiation

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BTL Layout inside the CMS tracker support tube

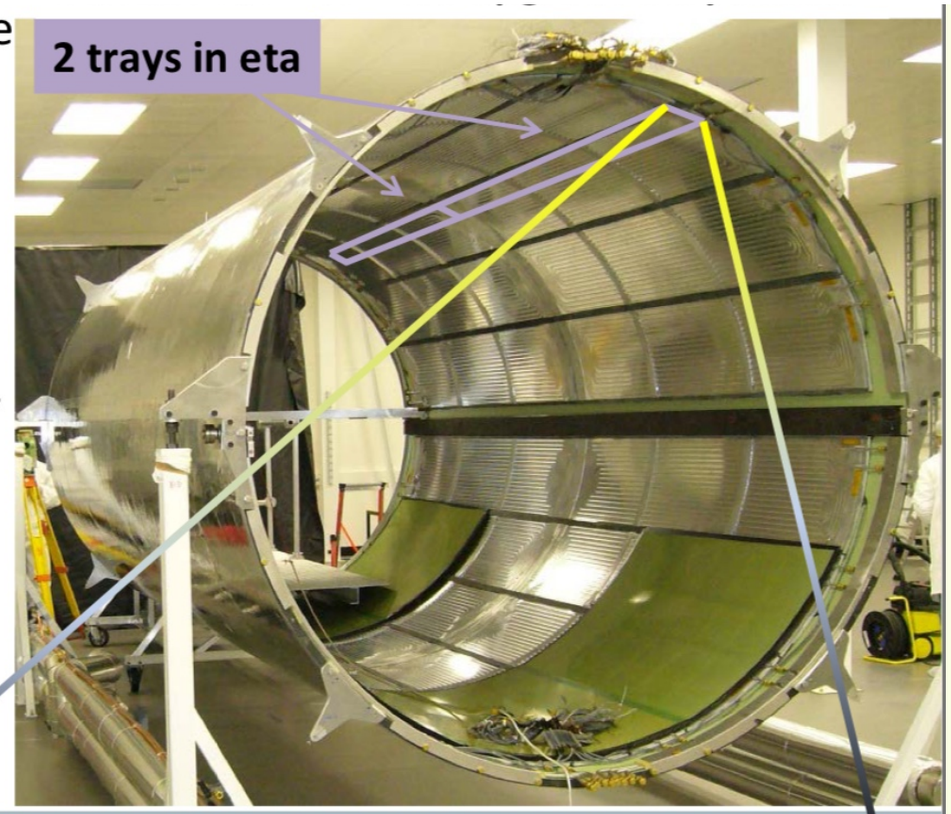
LYSO bars with double sided 16ch SiPM array readout

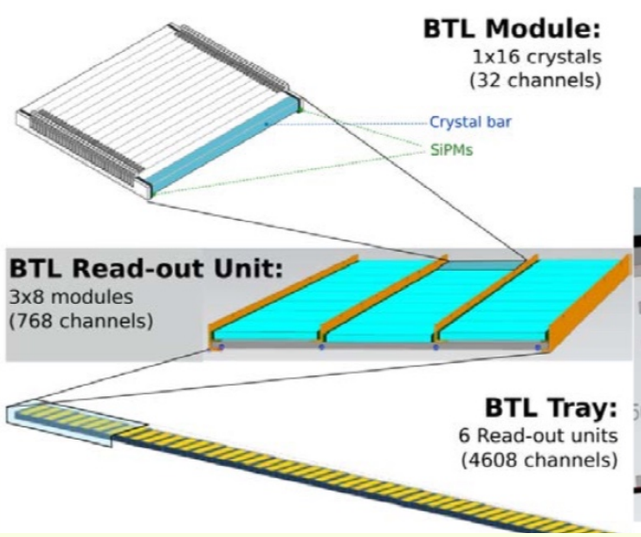
BTL will be attached to the inner wall of the Tracker Support Tube (TST).

Cold volume shared with Tracker (TRK).

BTL Segmentation :

- 72 trays (36 in $\varphi \times 2$ in η)
- 331k readout channels, 165k LYSO bars, organized in 6 Readout Units per tray.
- Tray dimensions : 250 x 18 x 2.5 cm





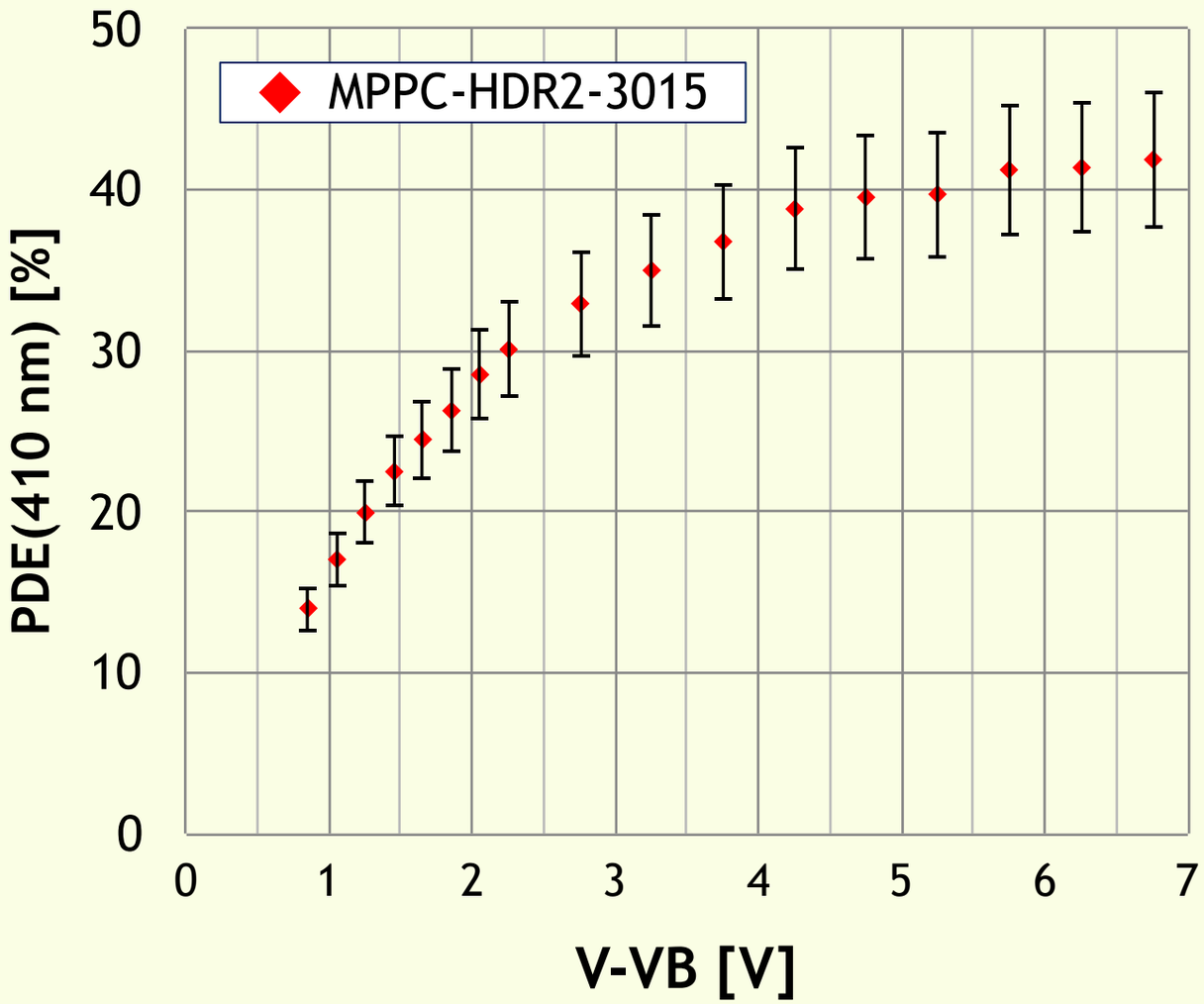
Timing resolution goals are 30 ps (BOO) to 60 ps (EOO) to resolve multiple interactions at high luminosity

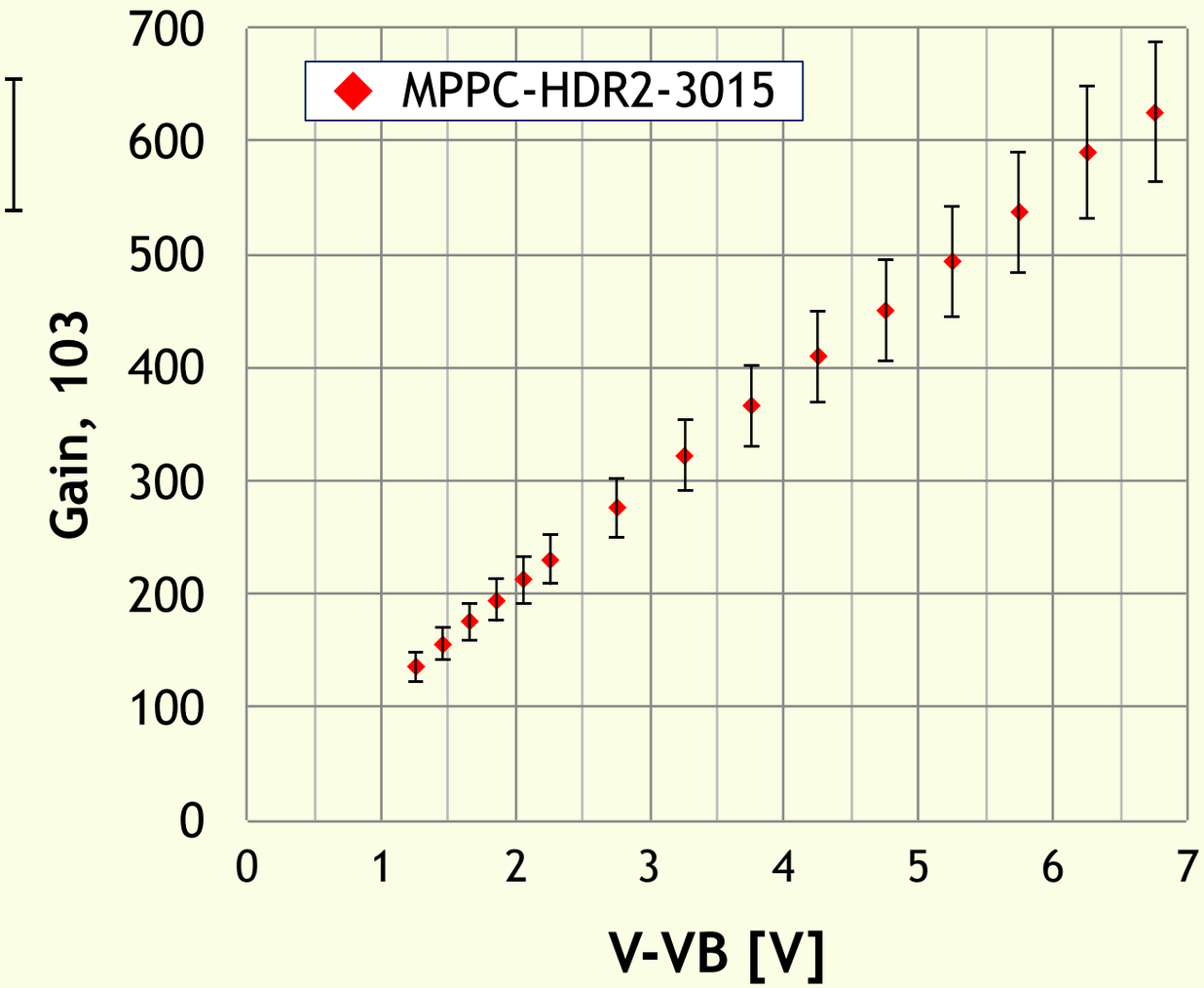
CMS Barrel Timing layer photo detector

- Silicon Photomultipliers (SiPM) are the photodetectors of choice for the BTL. Features of SiPMs include:
  - Compact size, 3mm x 3mm for the BTL
  - Small pixels (15 micron or less) provide extended linear dynamic range and keep dark count manageable
  - High photon detection efficiency (PDE) of > 20% for 15 micron pixels
  - Fast recovery time of < 10 ns
  - Insensitivity to magnetic fields
  - Good uniformity over large numbers of channels
  - Relative ease of operation
  - Sufficiently radiation resistant for use in the BTL, still performant at end of life of the detector
- Given the constraints from the detector design and the features listed above, SiPMs are the only reasonable option for the BTL
- Challenges after very high expected radiation (2E14 n_{eq}/cm2)
  - High DCR resulting in a large noise contribution dominating the timing resolution
  - High SiPM gain results in large power consumption at end of CMS data taking
- BTL is planning to operate at -30 to -35°C and is limited by the CO_2 cooling system
- R&D was conducted to investigate the use of TECs to even further lower the temperature to reduce DCR without exceeding the total power budget (800 mW/16channel SiPM array)

SiPM parameters

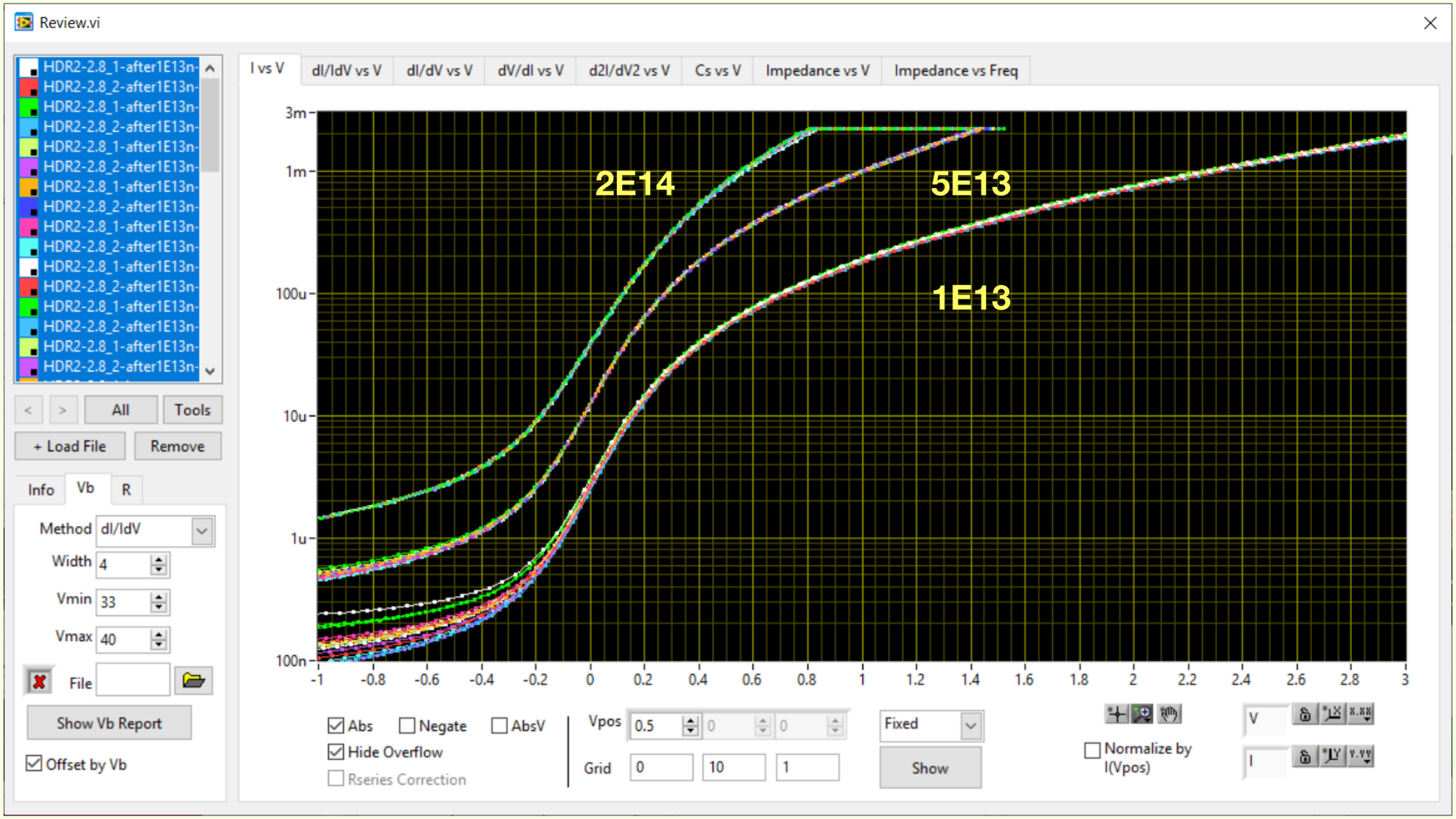
We work with multiple SiPM vendors in the BTL but for this TEC R&D we used the Hamamatsu 3x3 mm HDR2 SiPM





Due to the fast rising PDE data shows that these HDR2 SiPMs have optimum S/N after high irradiation at 1 to 1.5V over voltage (V-Vb)

SiPM measured dark current at nominal -35°C



I_{dark} vs $V-V_{br}$

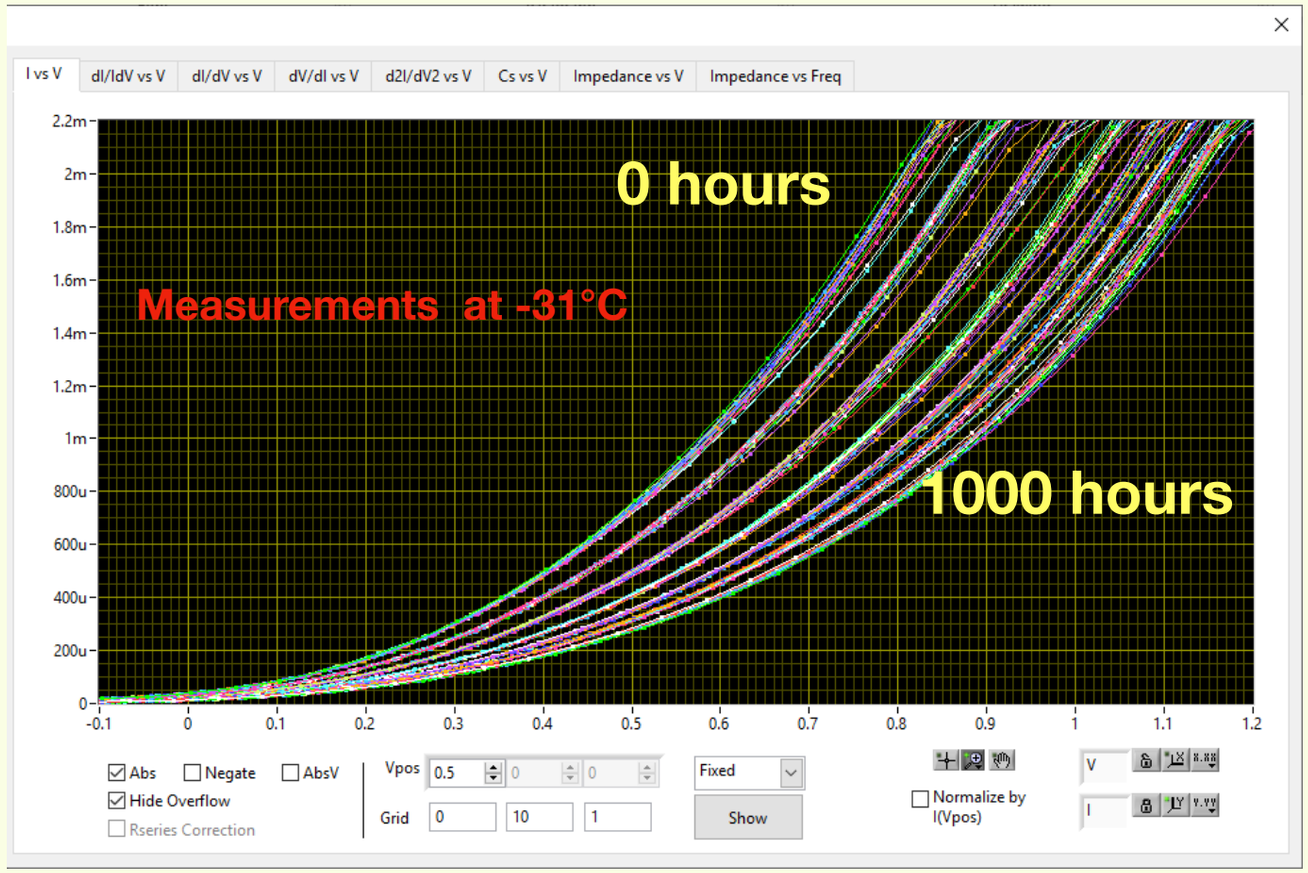
Dark Count Rate

DCR = I / (Gain x q x A)

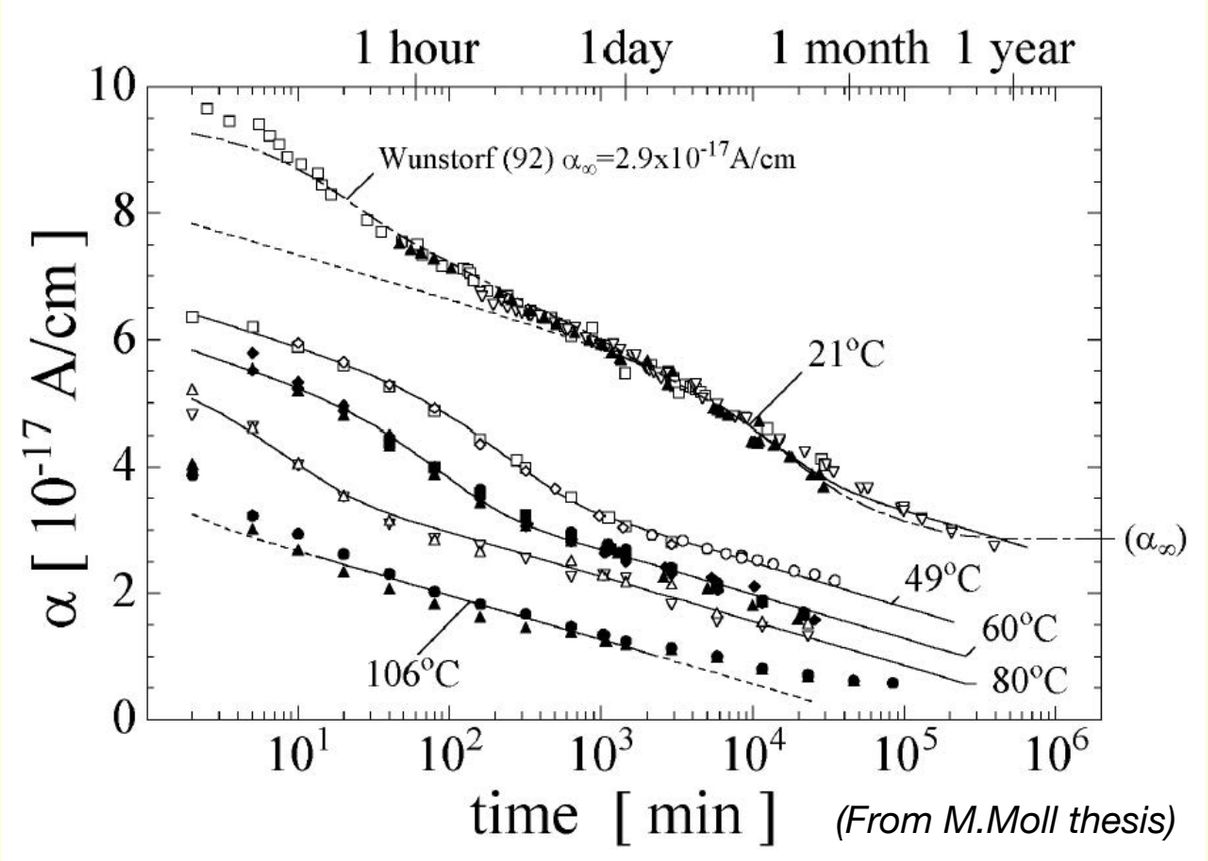
We find a DCR of 14 GHz/mm2 <u>before</u> annealing at 2E14 n/cm² at 0.8V (-35°C)

Annealing

16 ch array annealing at 40°C after 2E14 n/cm2



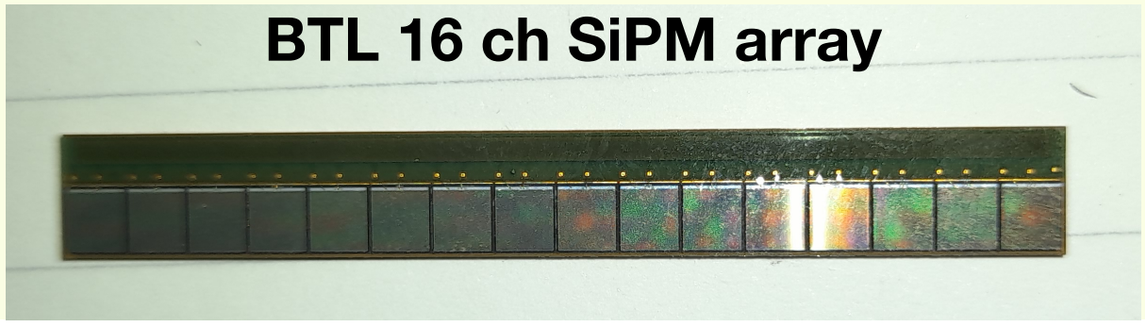
Silicon Anneling vs temperature

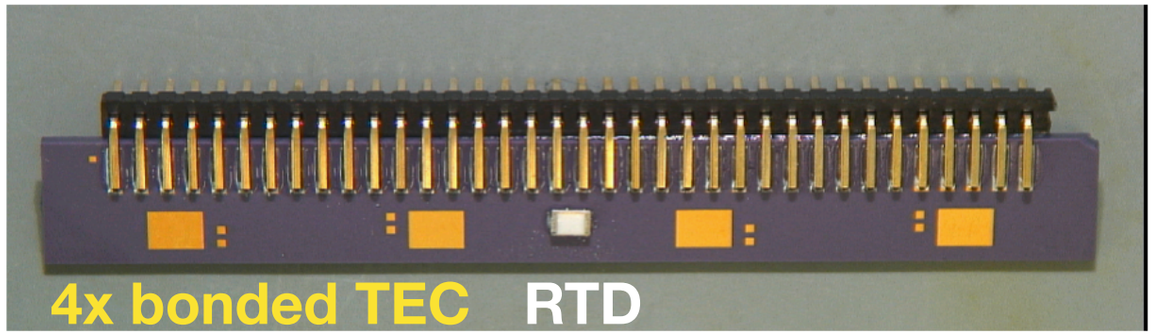


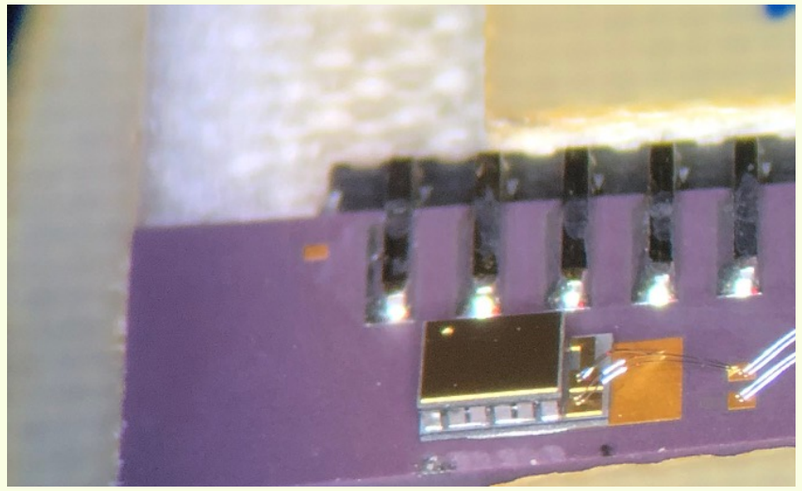
- In general an annealing of 80 min at +60C can be used to simulate long RT annealing after irradiation
- Good agreement is found by using 4 days at +40°C

- We also studied SiPM annealing on higher temperatures to investigate if TEC can also be used to enhance annealing during LHC yearly shutdown/maintenance cycles.

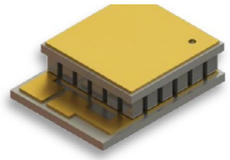
Off the shelf mini TECs from Phononics







Phononics 2 x 2 x 0.9 mm3



- High-performance solid-state thermoelectric cooler (TEC) delivering precise temperature control to meet unique thermal requirements of optical electronics
- Customizable TECs assembled in a US-based, ISO-certified, automated production facility under tight process control and metrology for superior performance and reliability

Features and Benefits

Benefits

- Up to 30% lower power consumption
- Up to 60% better heat pumping density
- Accurate, precise temperature control
- Small mechanical footprint

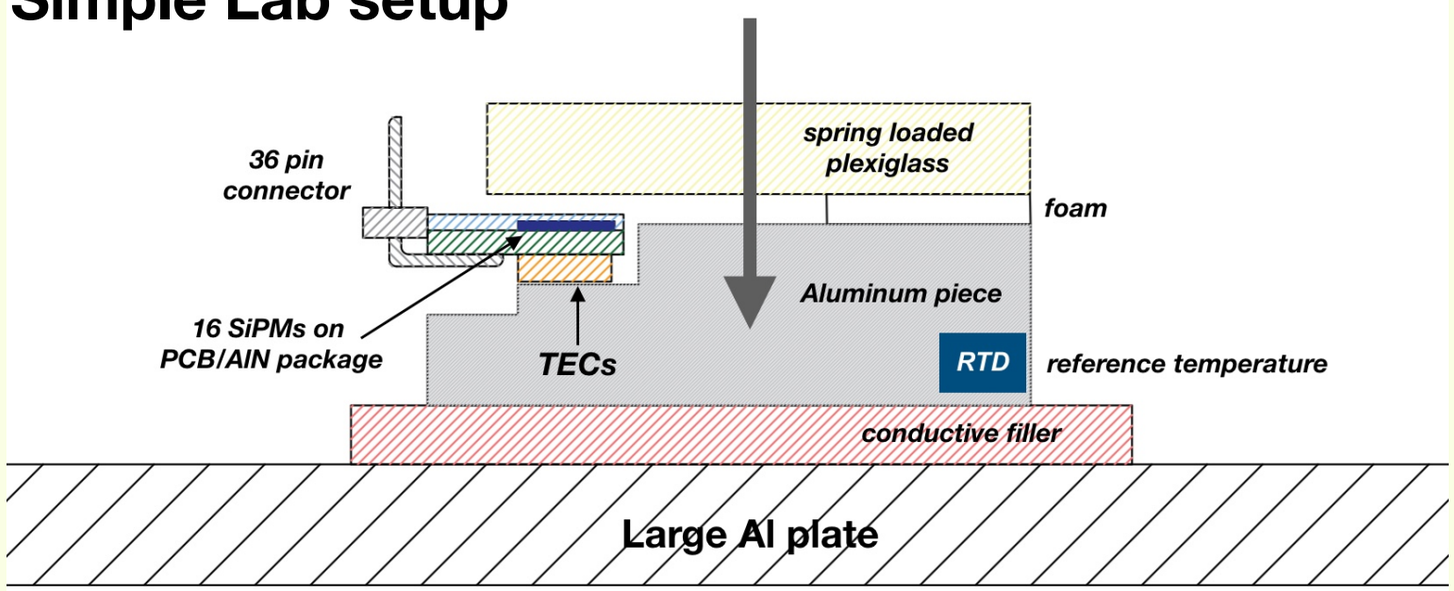
Features

- Industry-leading diffusion barriers and electrical contacts
- High-temperature solder with integration temperatures up to 215°C
- Aluminum nitride ceramic header materials
- RoHS compliant designs

Specifications

Parameter	Performance Values	
Hot Side Temperature	25°C	75°C
ΔT_{MAX} (°C, vacuum)	65	84
Q_{MAX} (Watts)	1.18	1.61
I_{MAX} (Amps)	1.00	1.02
V_{MAX} (Volts, DC)	2.19	2.91
AC Resistance (Ohms)	1.87*	2.38

Simple Lab setup



Data at room temperature vs Simulation

General TEC equations:
(from thermodynamics)

$$Q_c + Q_{ev}\,\Delta T = \alpha\, I\, T_c - 0.5\, I^2 R - K\,\Delta T$$

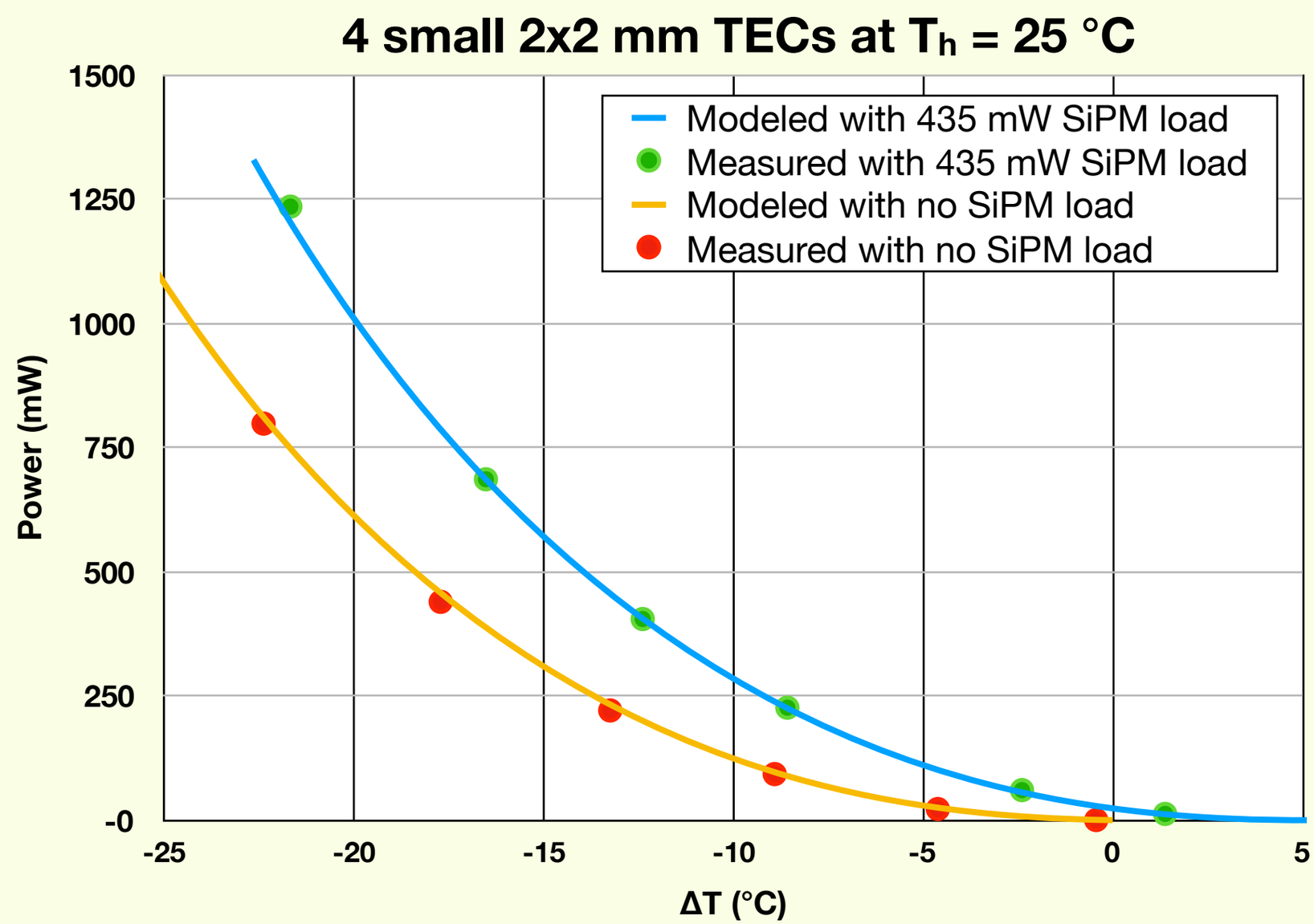
$$V = \alpha\,\Delta T + I\, R_{AC}$$

Q_c = SiPM power (W)
Q_{ev} = Thermal leakage (0.039 W/K)

α = Seebeck coeficient (0.028 V/K)
K = TEC conductance (0.044 W/K)
R_{AC} = TEC resistance (8.0 Ω)

435 mW was used as a SiPM load :

SiPM power is expected to be reduced by 1.85 from 800 mW for 10 °C more cooling

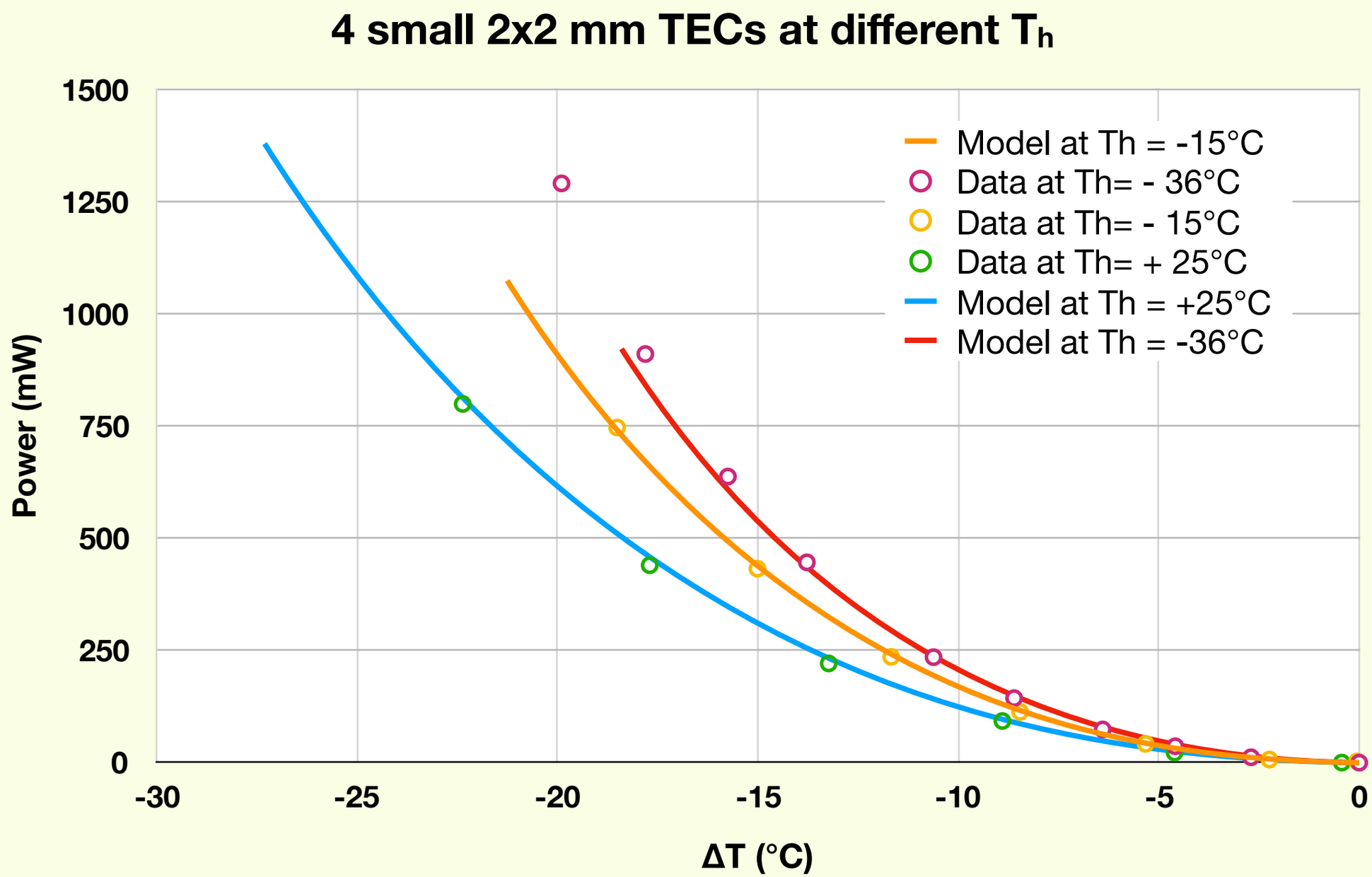


Climate chamber data

TEC parameters linear regression

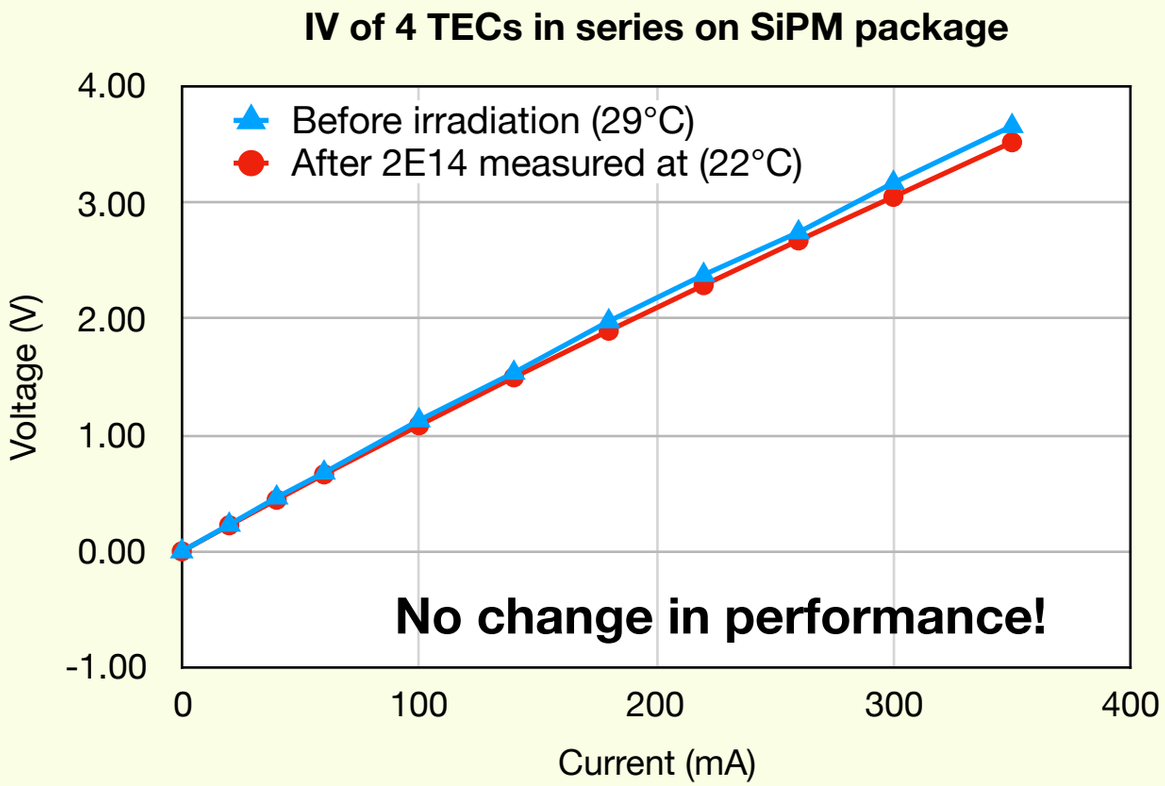
T_h = -36C :

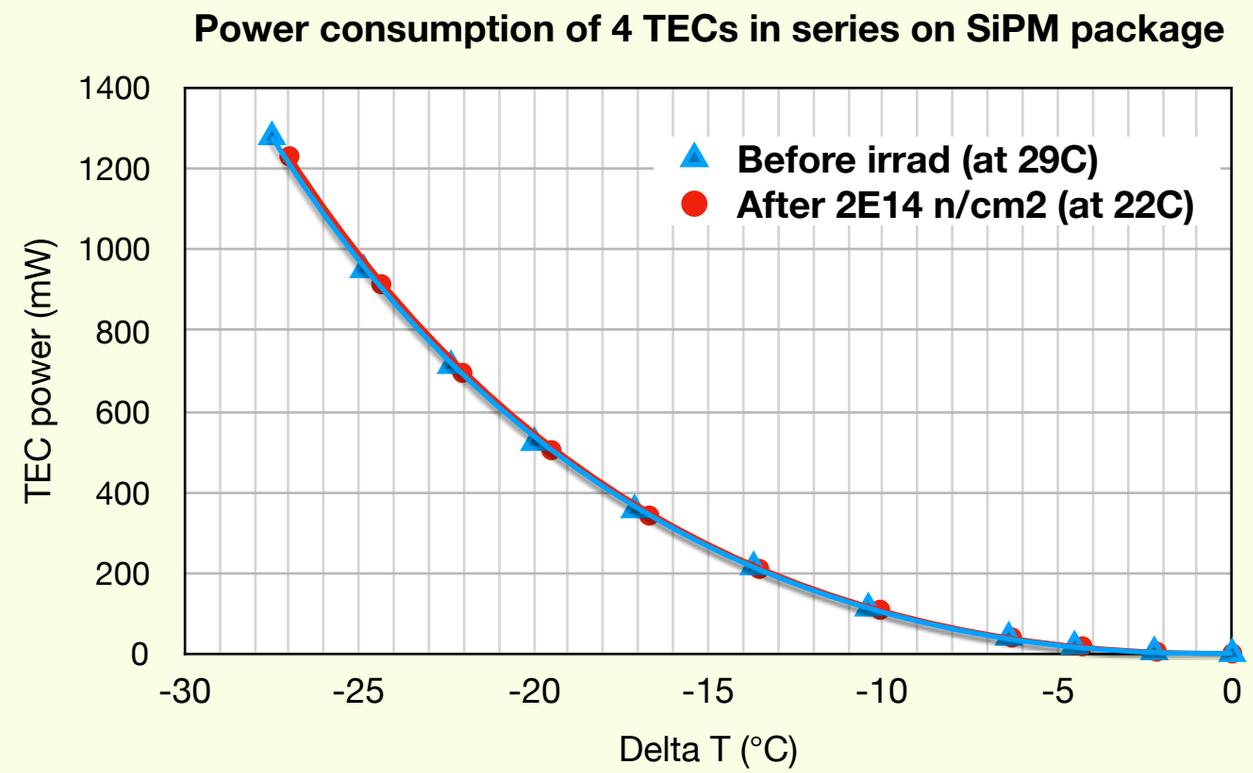
$Q_c = 0$
$Q_{ev} = 0.039$ W/K
$\alpha = 0.0235$ V/K
$K = 0.044$ W/K
$R = 5.6\ \Omega$

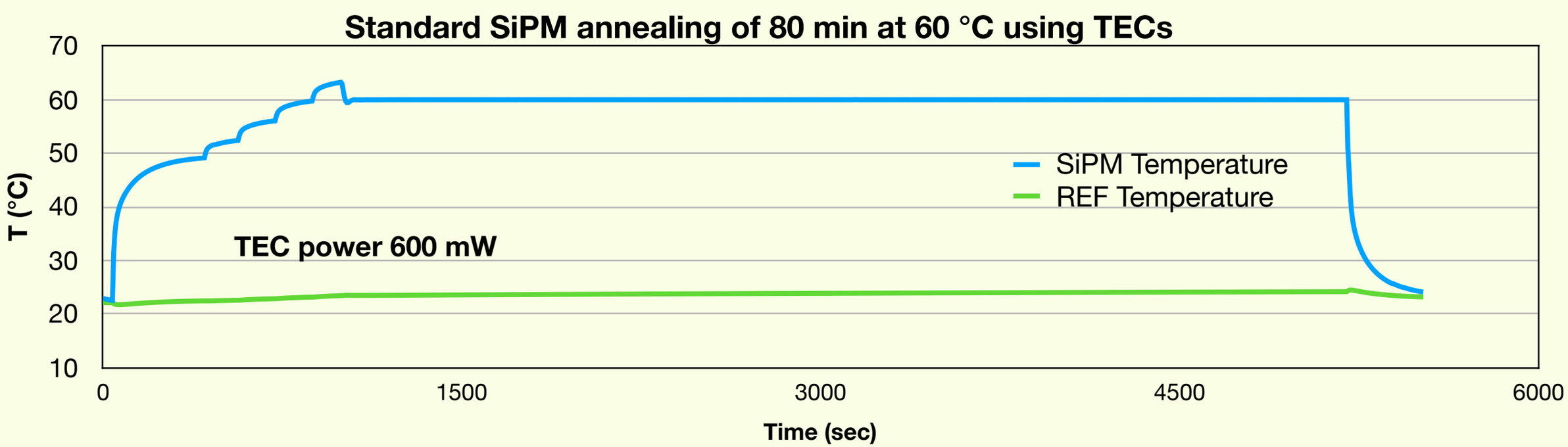


Higher power consumption for -35°C agrees with the TEC thermodynamic model

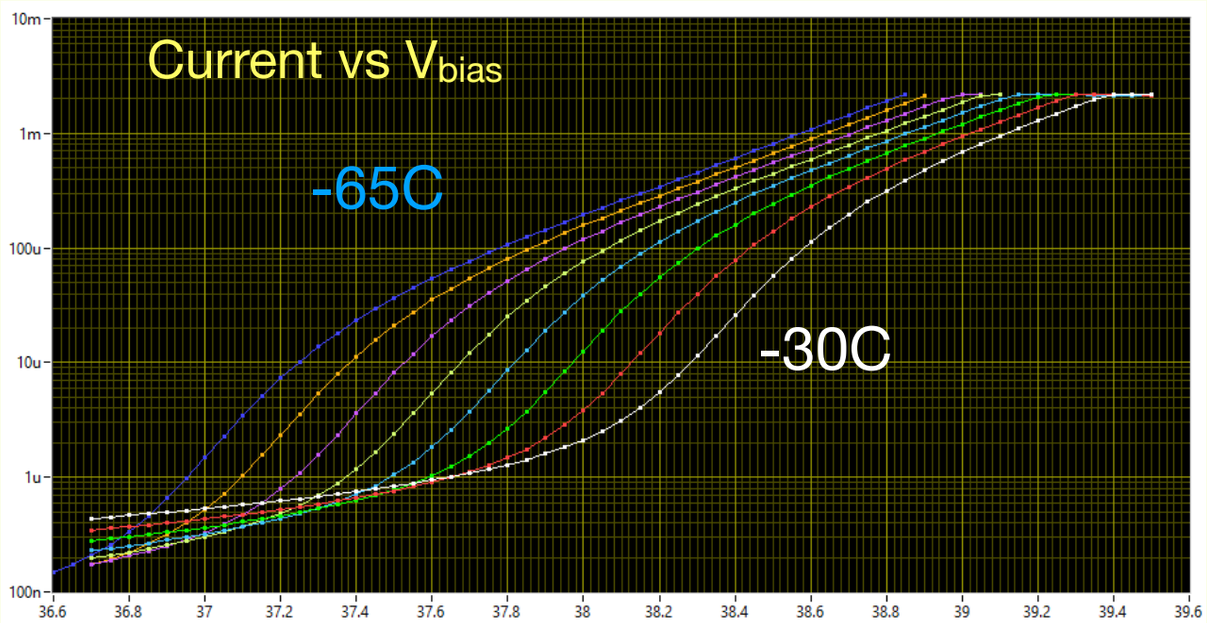
(TEC + SiPM) package irradiated to 2E14

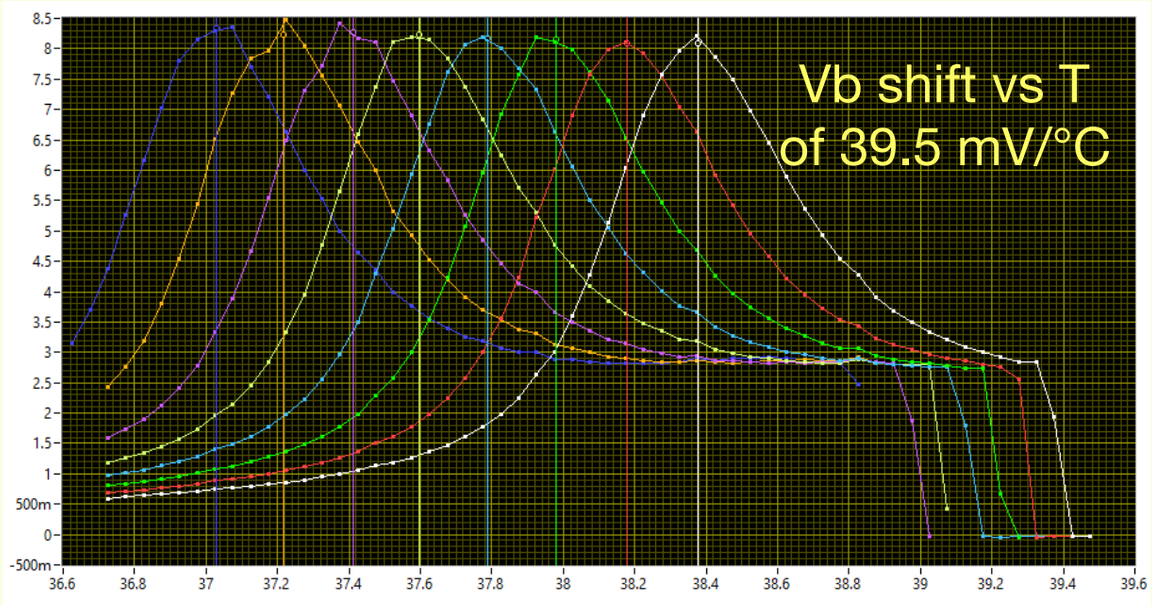


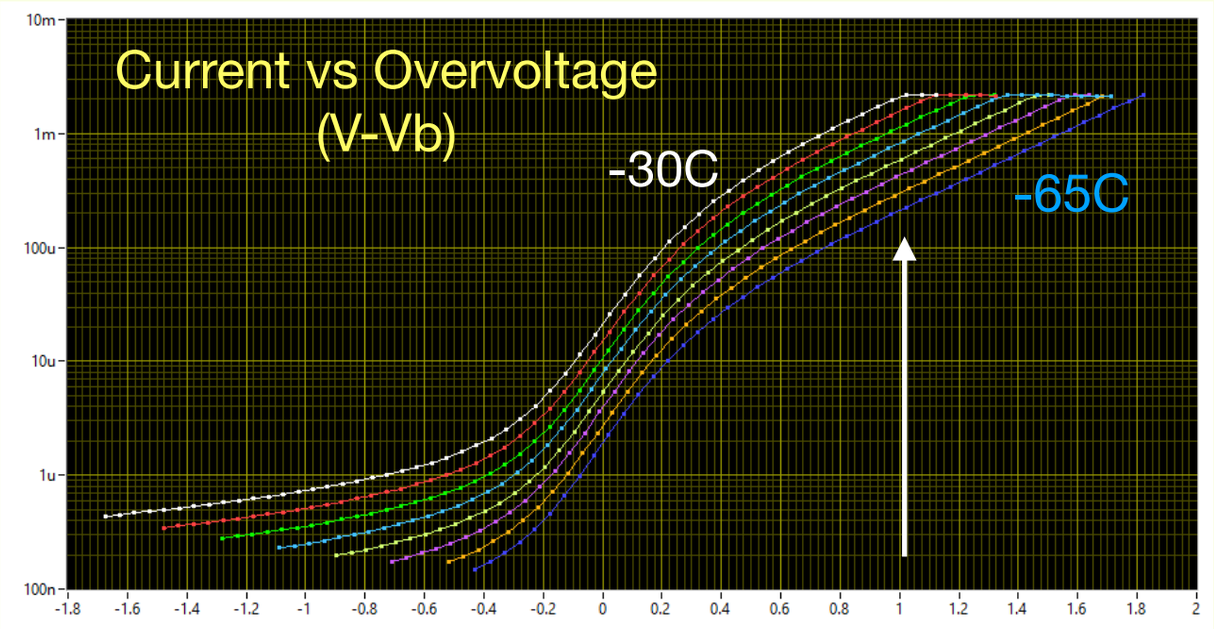


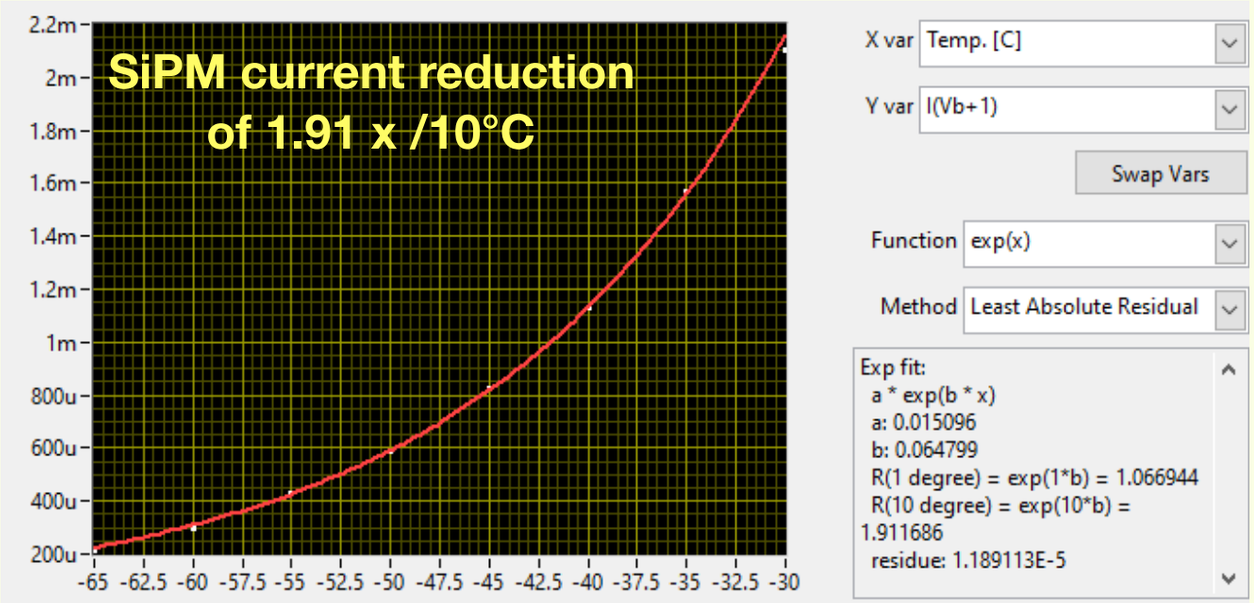


SiPMs data of ch 9 (-30°C to -65 °C)



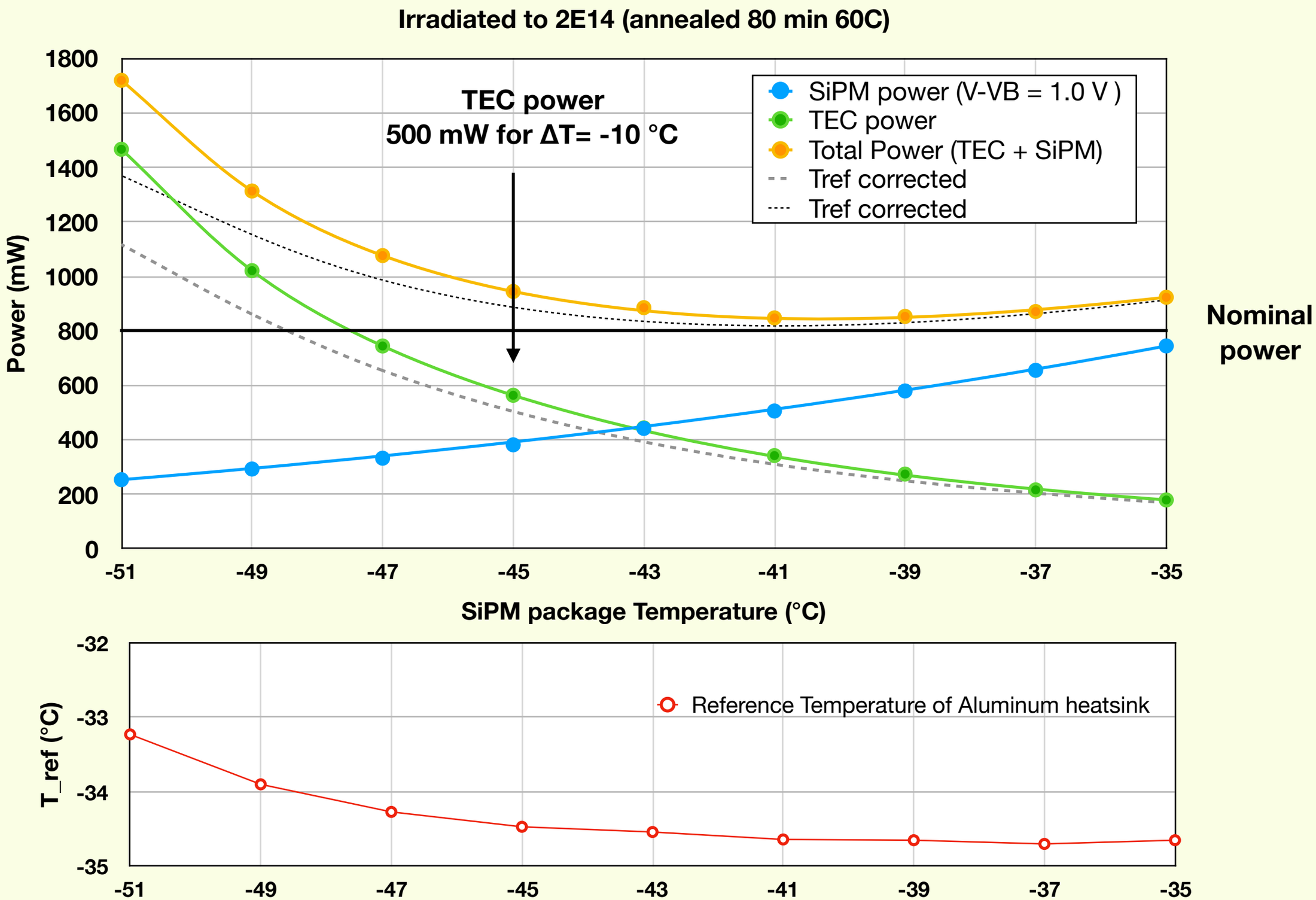






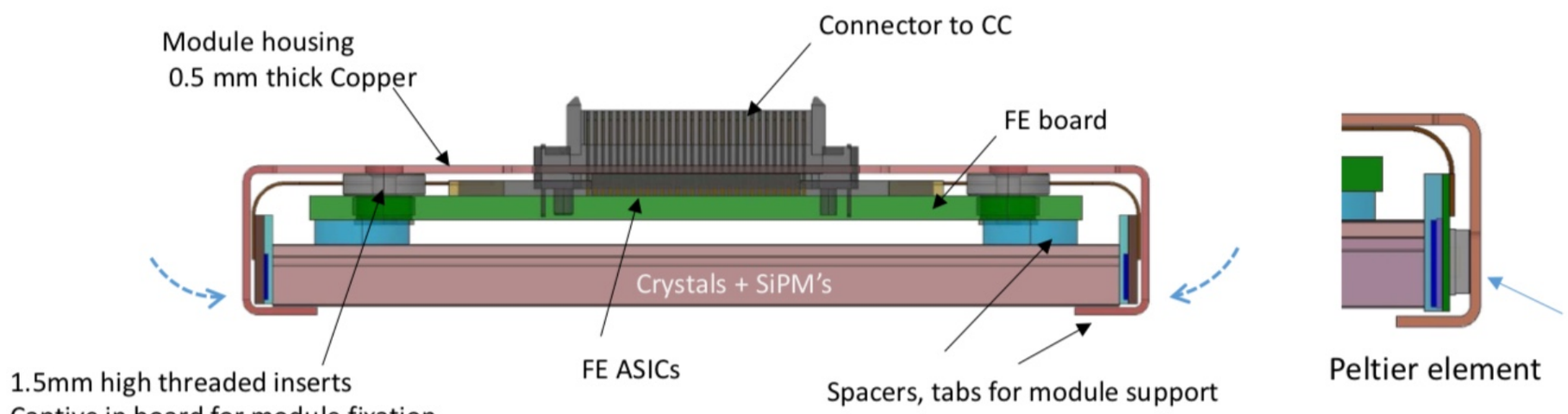
Using Climate chamber (with dry air) set to -30°C and -50°C

Total power consumption for full array at 1 V over voltage

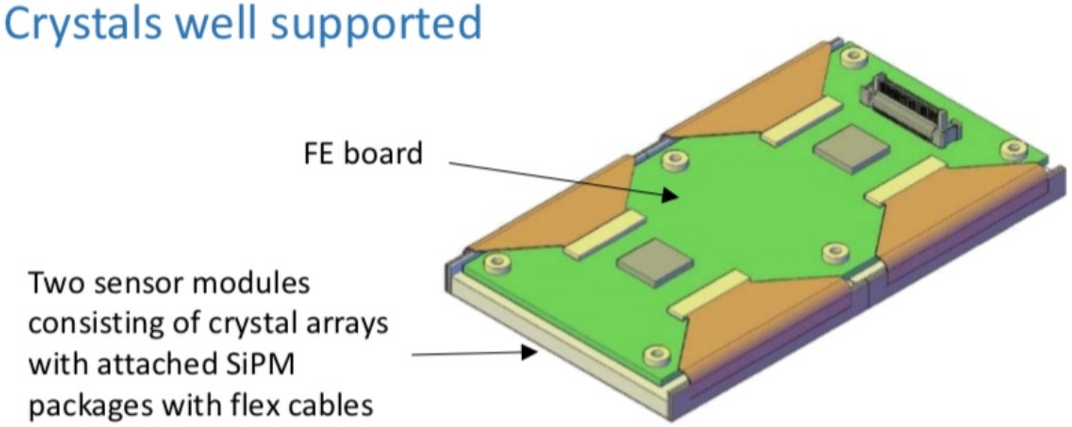


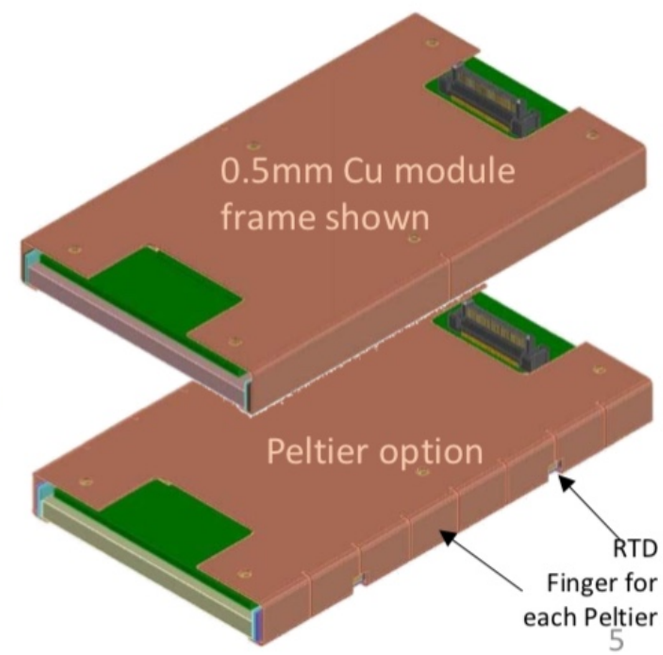
BTL Basic Detector unit

In real detector unit we expect larger thermal leakage due to LYSO (3W/m.K) and flex cable



- Spring force from housing guarantees thermal interface always under compression
- Absorbs tolerance and CTE effects
- Dimensions do not require tight tolerances
- Crystals well supported





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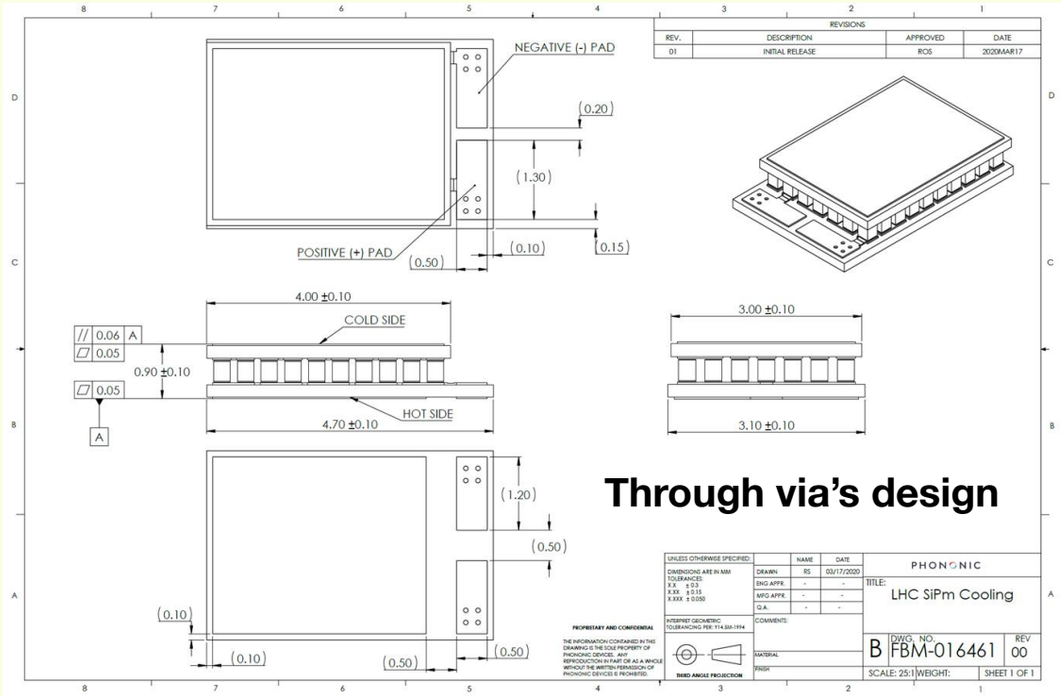
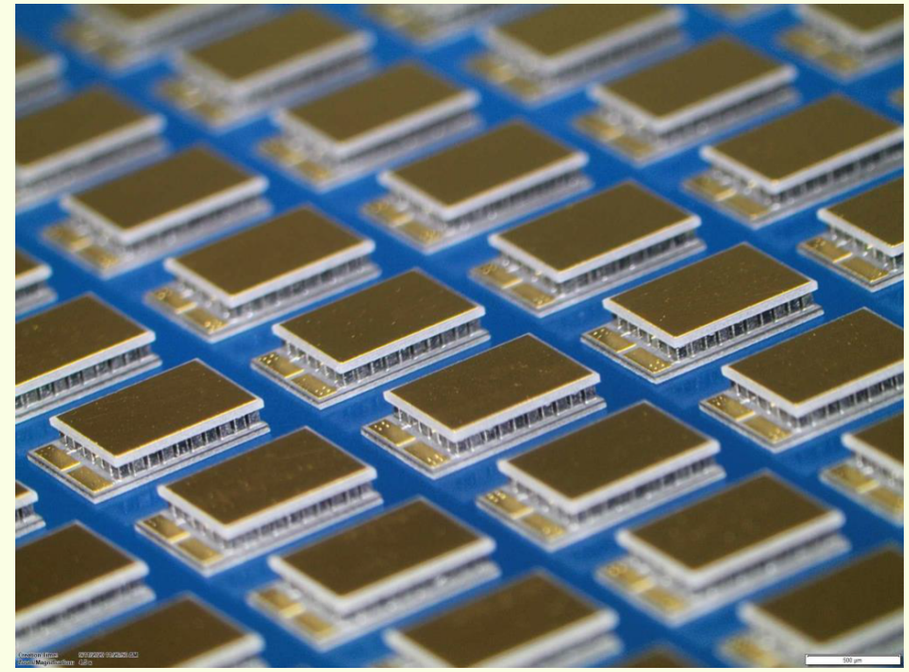
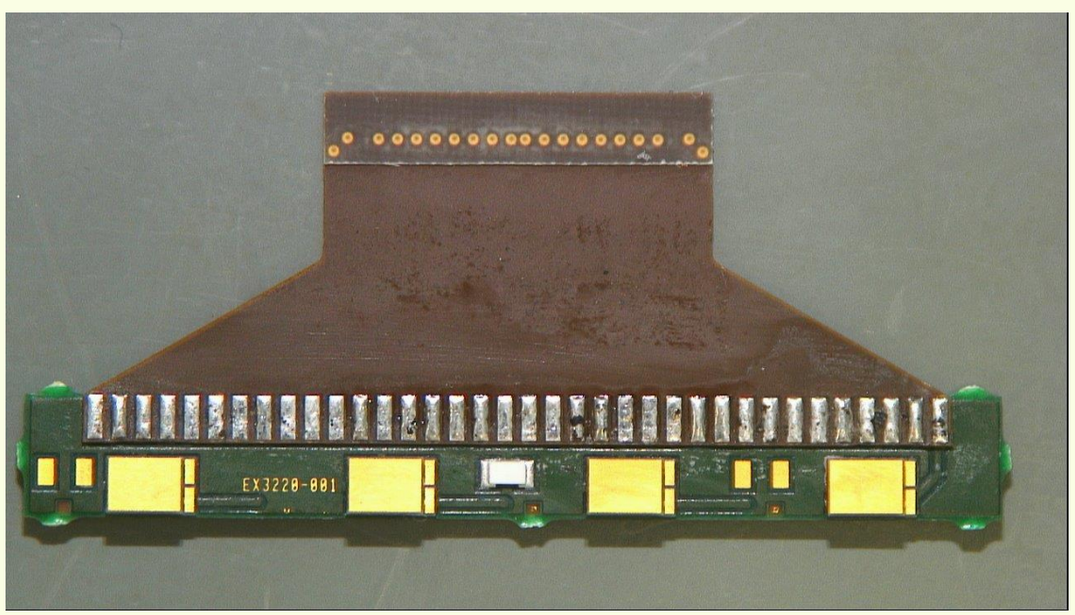
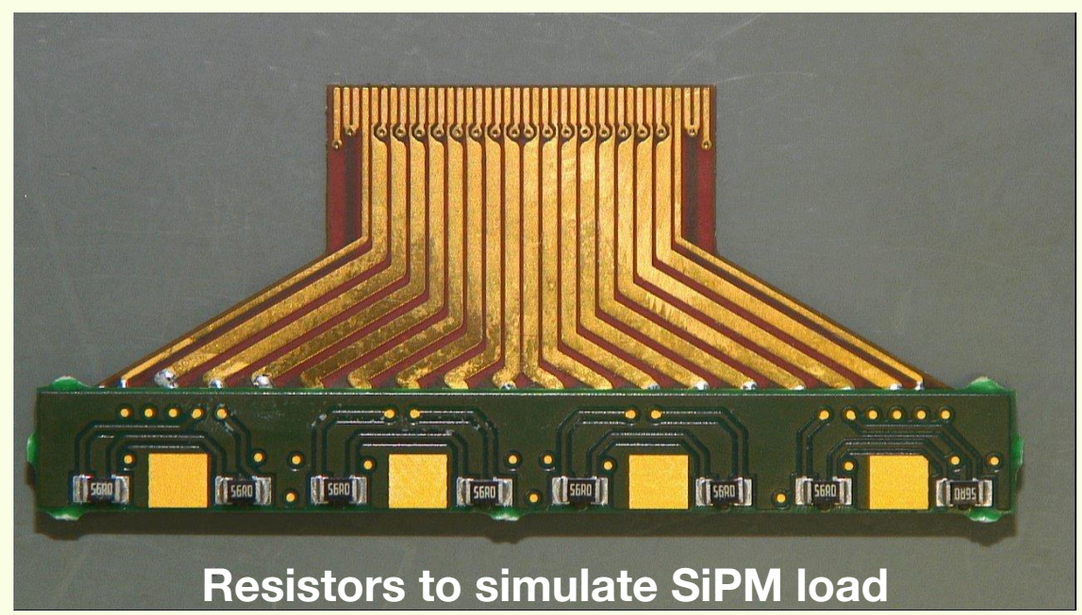
Phononic custom TECs of 3x4x0.9 mm

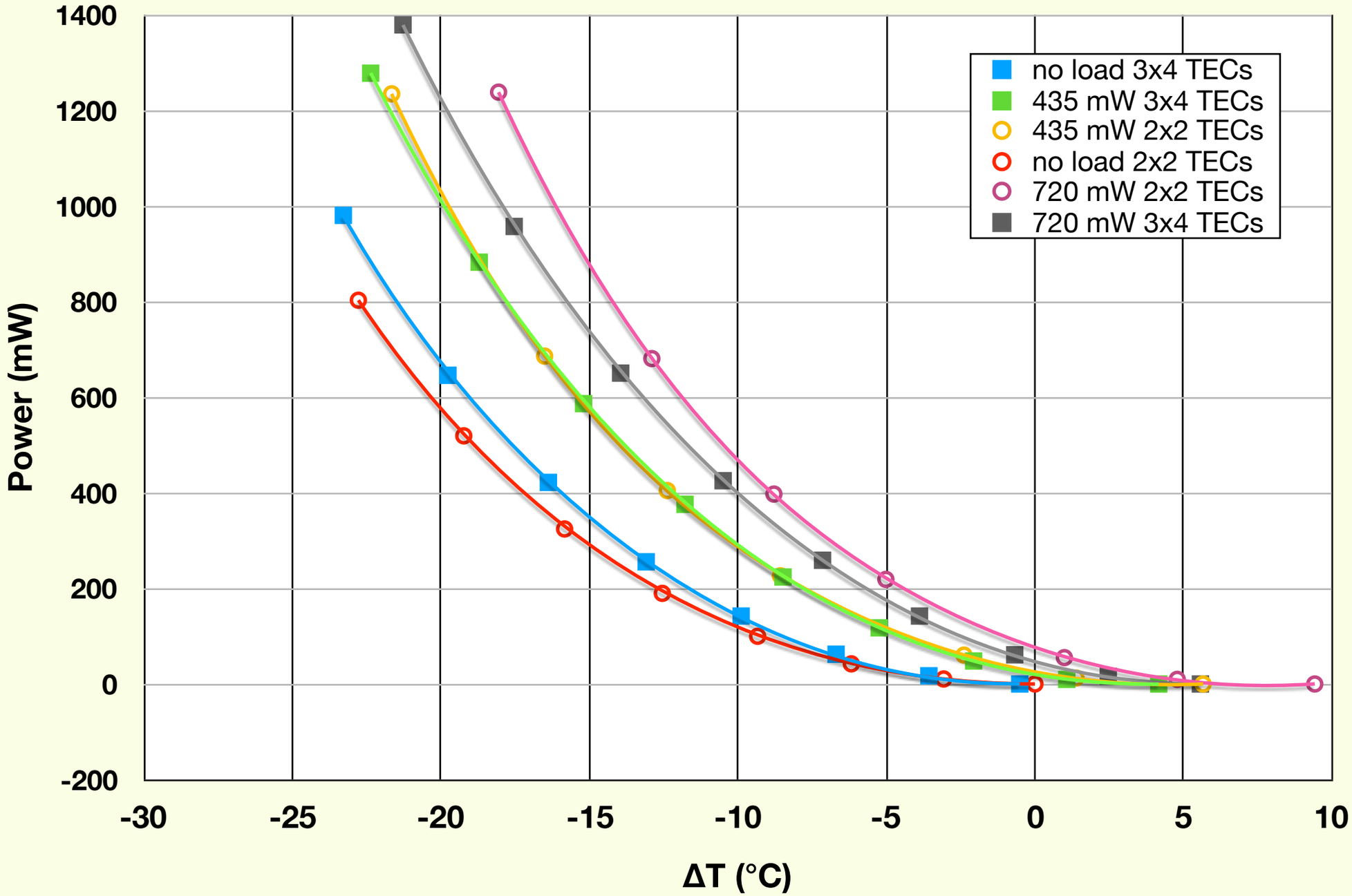






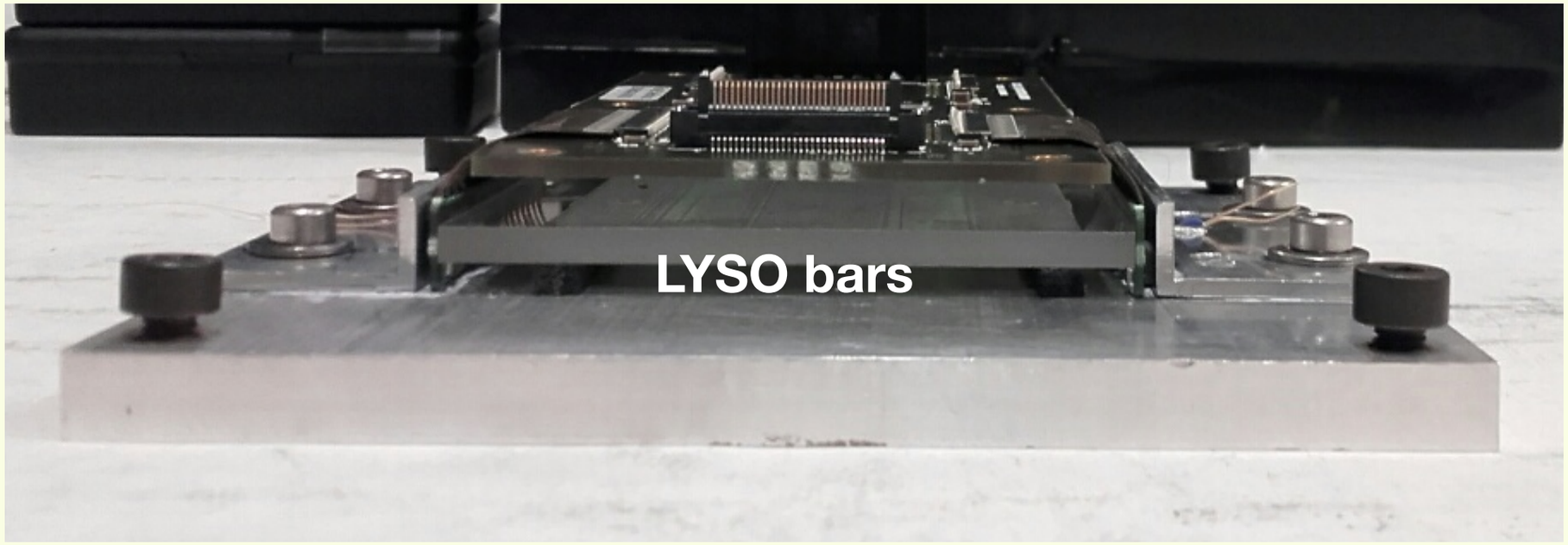


First 3x4 mm TECs data in LAB setup

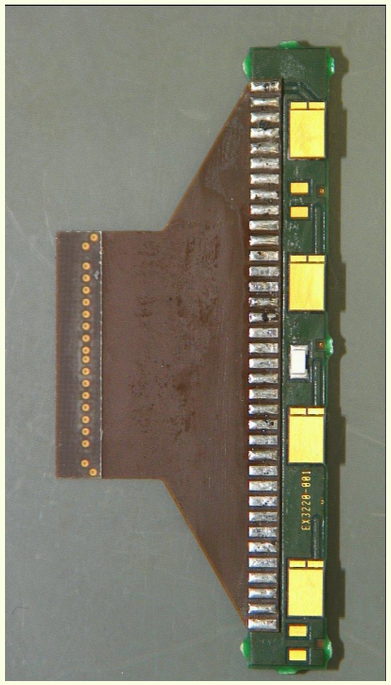


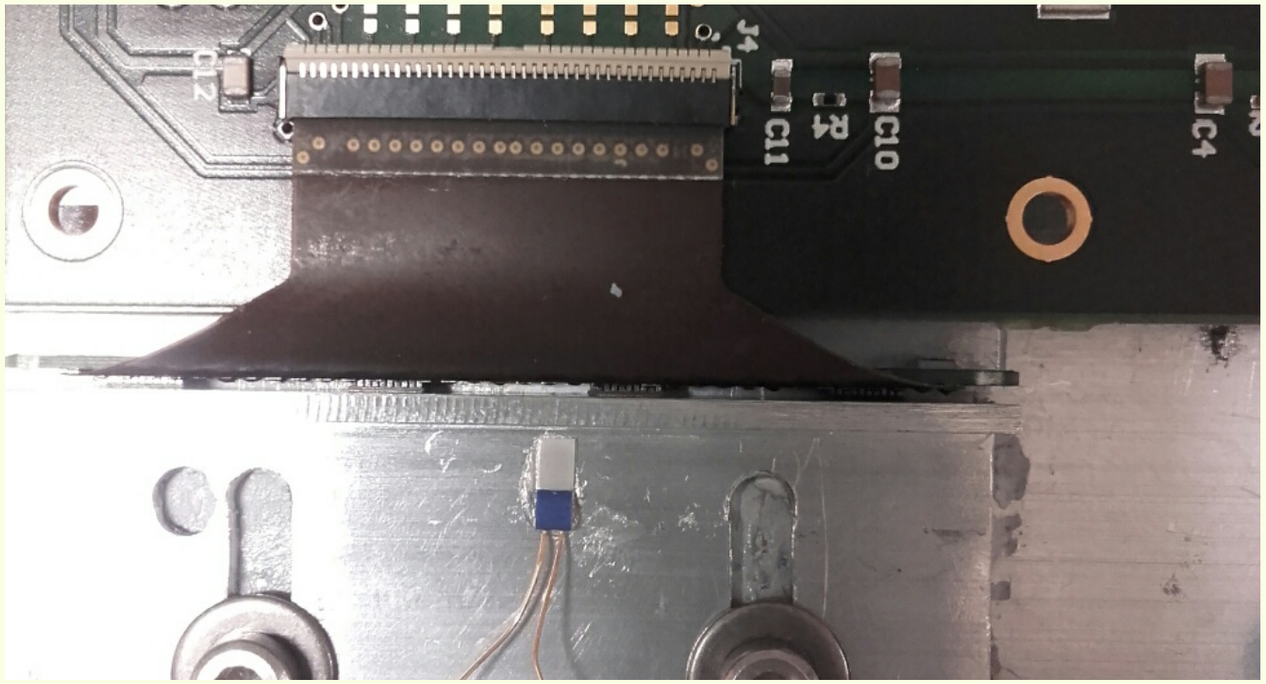
Performance is as expected lower power consumption for 3x4 mm vs 2x2 mm at high load

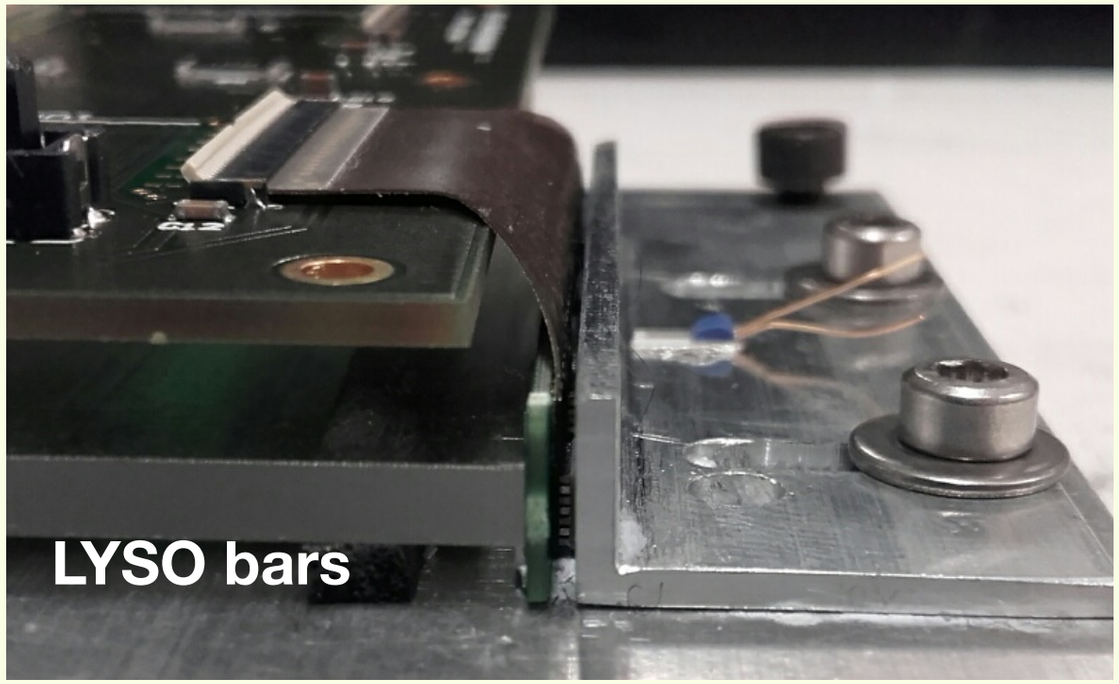
Mock-up with Flex and LYSO



Flex cable with gnd plane







Two packages are hooked up in parallel (package Flex 2 and Flex3, right and left)

Data with No load (Q_{sipm}=0)

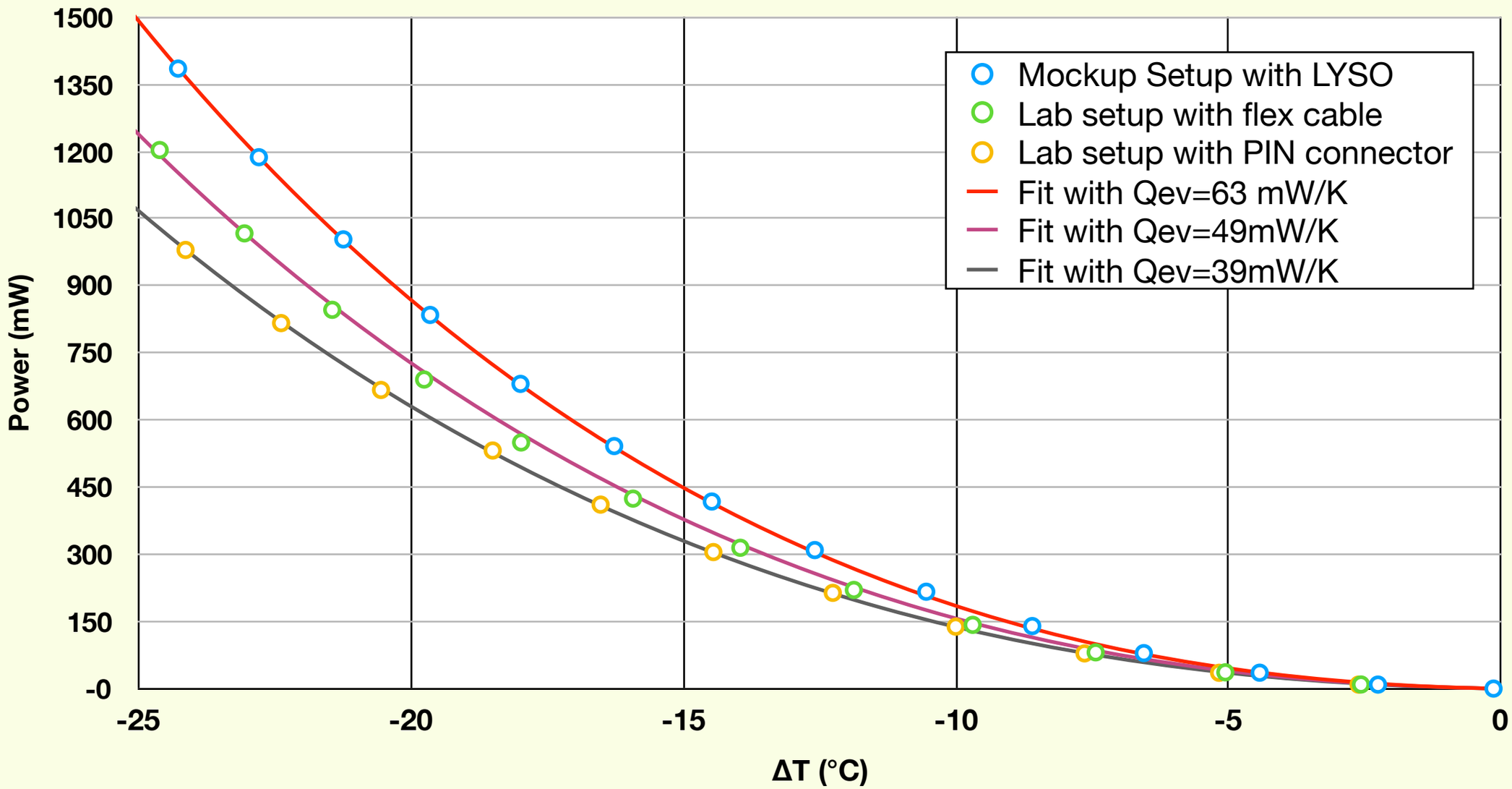
$$Q_c + Q_{ev}\,\Delta T = \alpha\, I\, T_c - 0.5\, I^2 R - K\,\Delta T$$

$$V = \alpha\,\Delta T + I\, R_{AC}$$

α = 4 * 14.7 mV/K

K = 4 * 0.0222 W/K

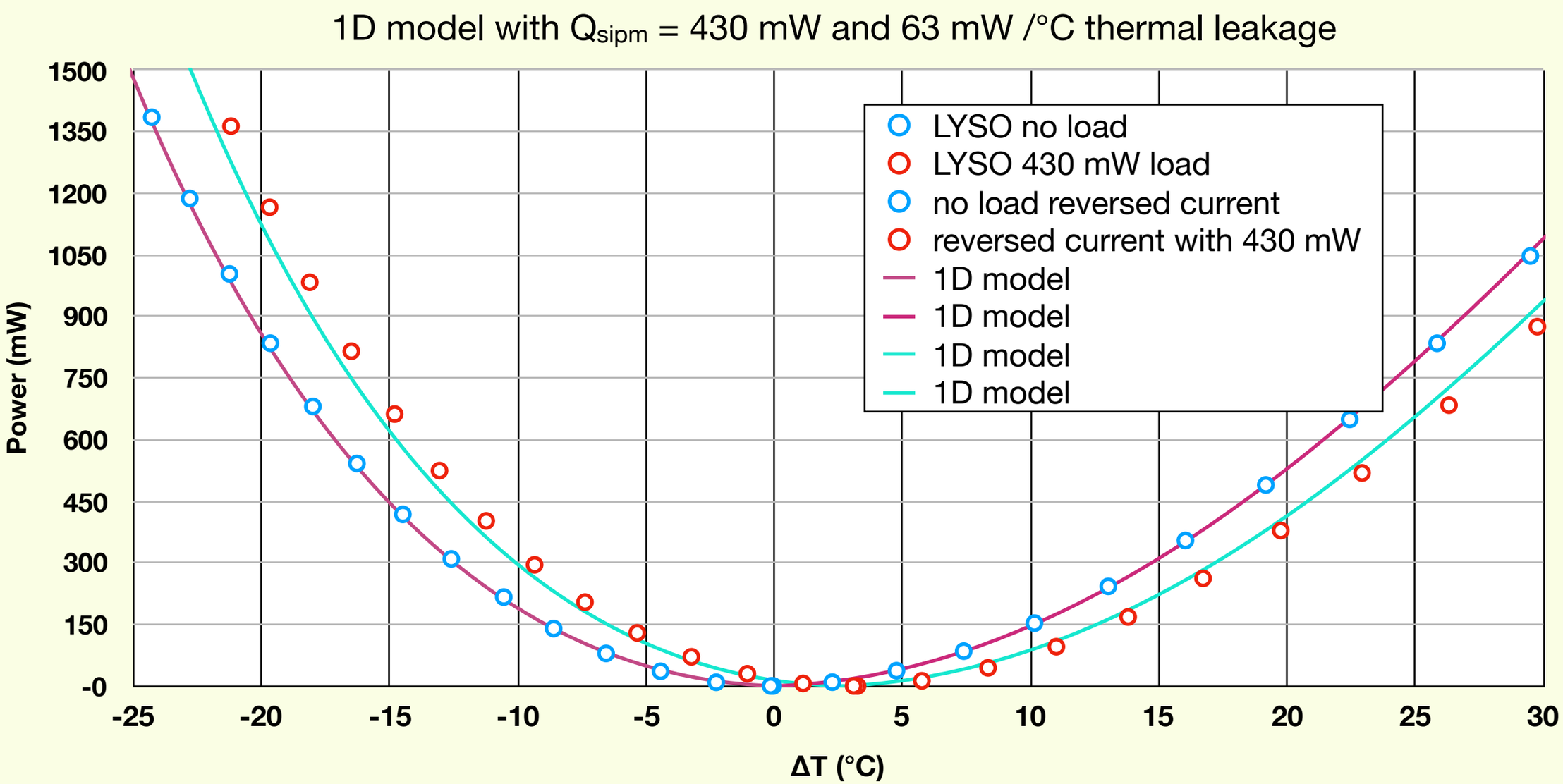
Rac = 4 * 3.73 Ω



Most important aspect:

We measure increase of the thermal leakage due to flex cable and LYSO vs simple lab setup

Mockup LYSO setup at +24C

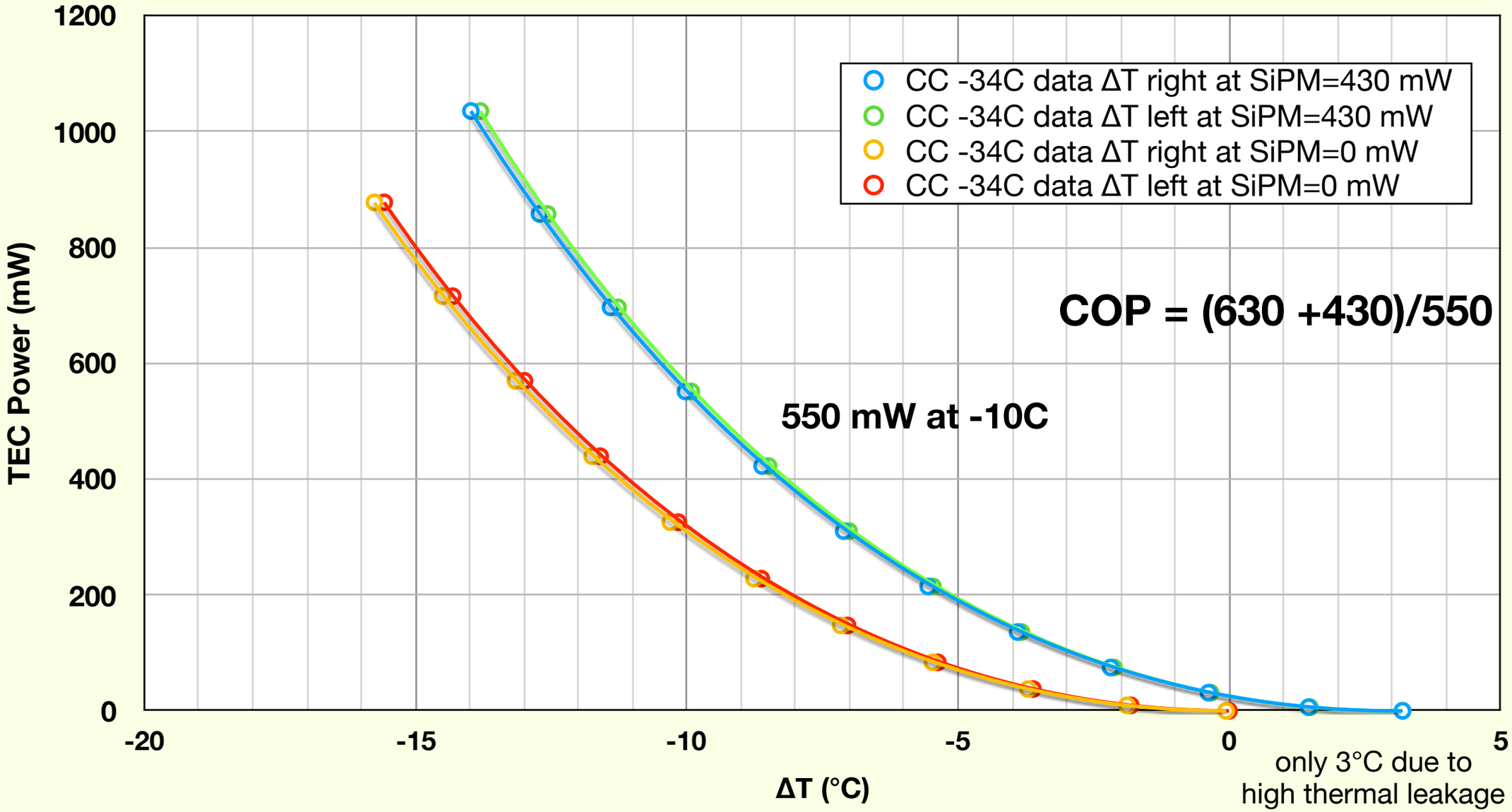


Small 50 mW discrepancy with the 1D model for 430 mW load

Most important aspect:

TEC is more efficient to heat than to cool ; ΔT of +25C above RT can be reached for 600 mW

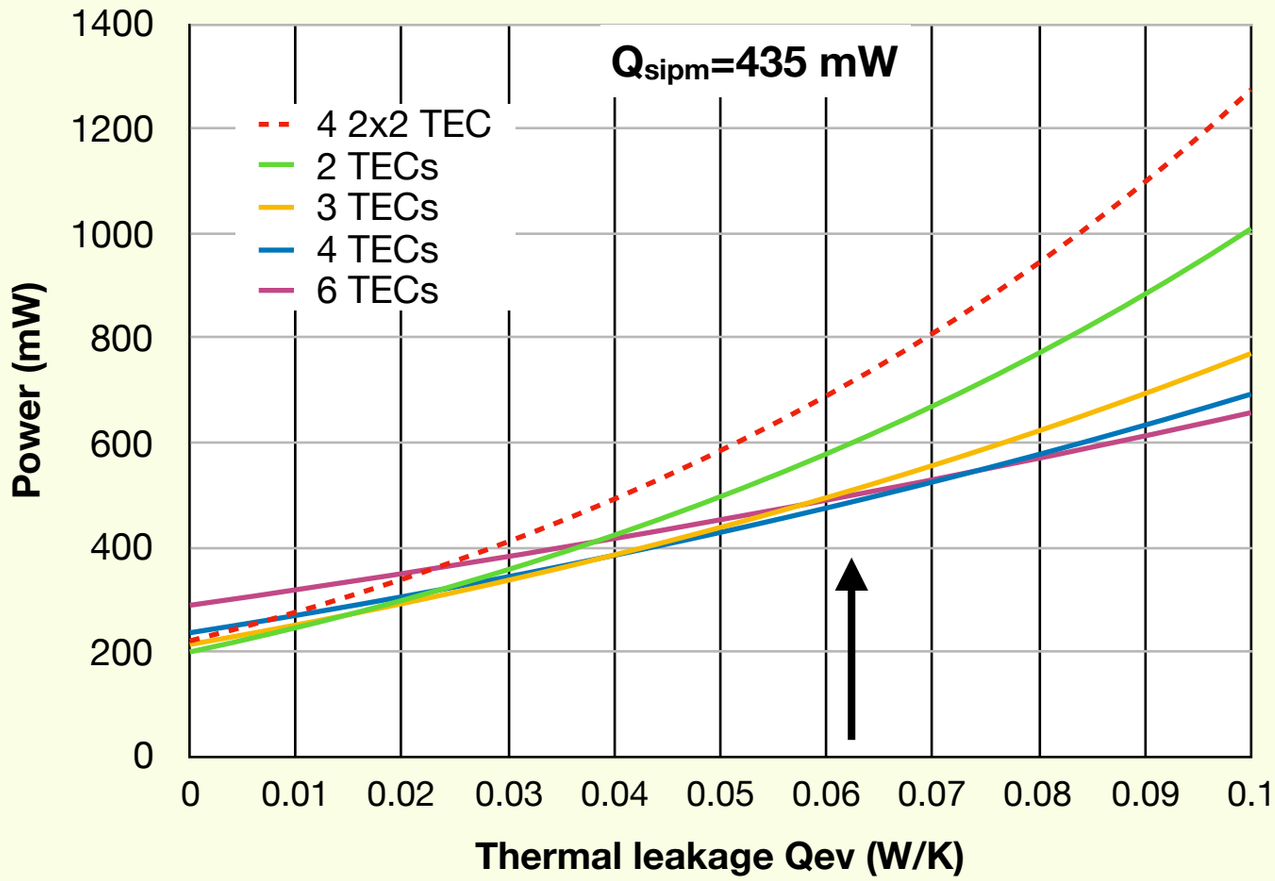
LYSO setup at -34C with 430 mW SiPM

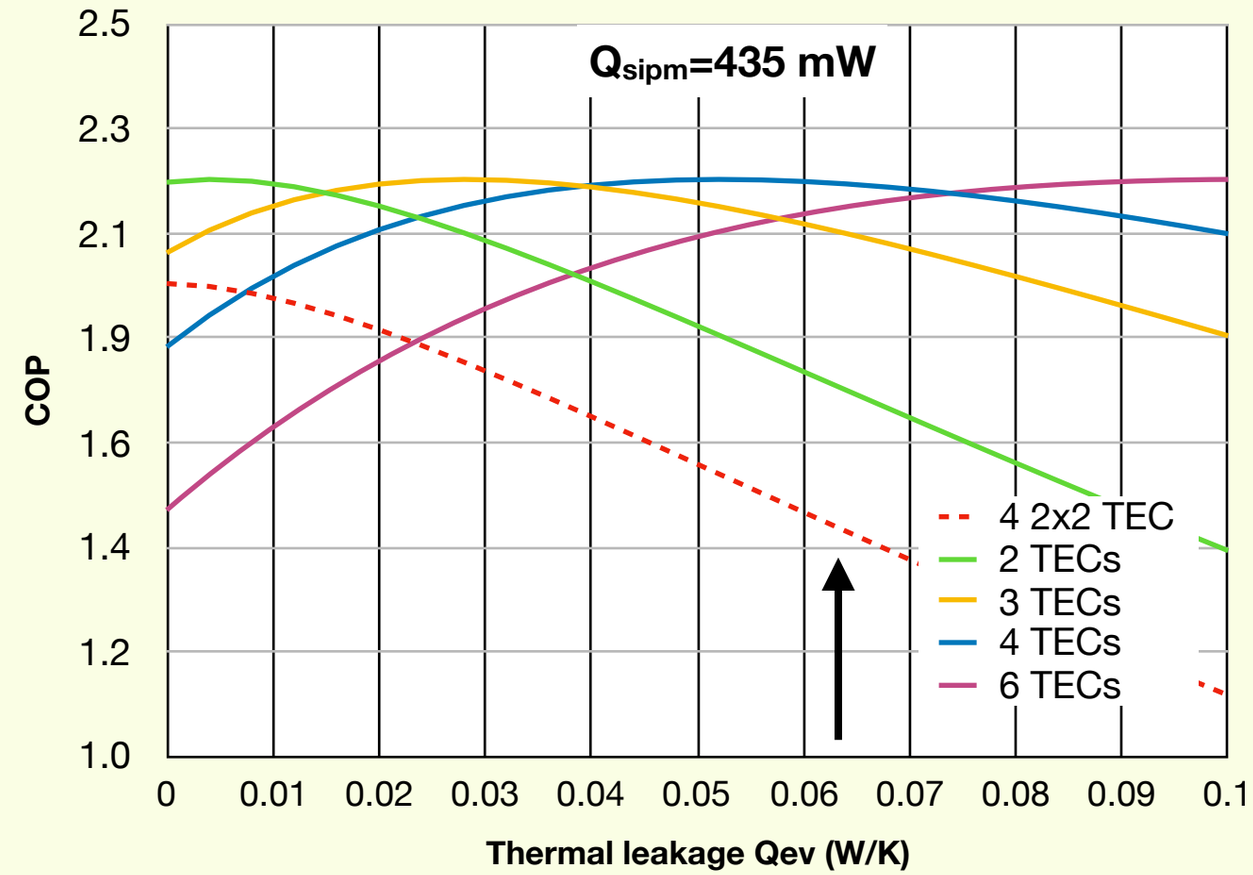


Most important aspect:

- We find a power consumption of 550 mW (not totally power neutral) but SiPM DCR reduced by 2x
- Expected COP of **2** at -10C very close to design parameter of manufacturer (same 50 mW discrepancy)

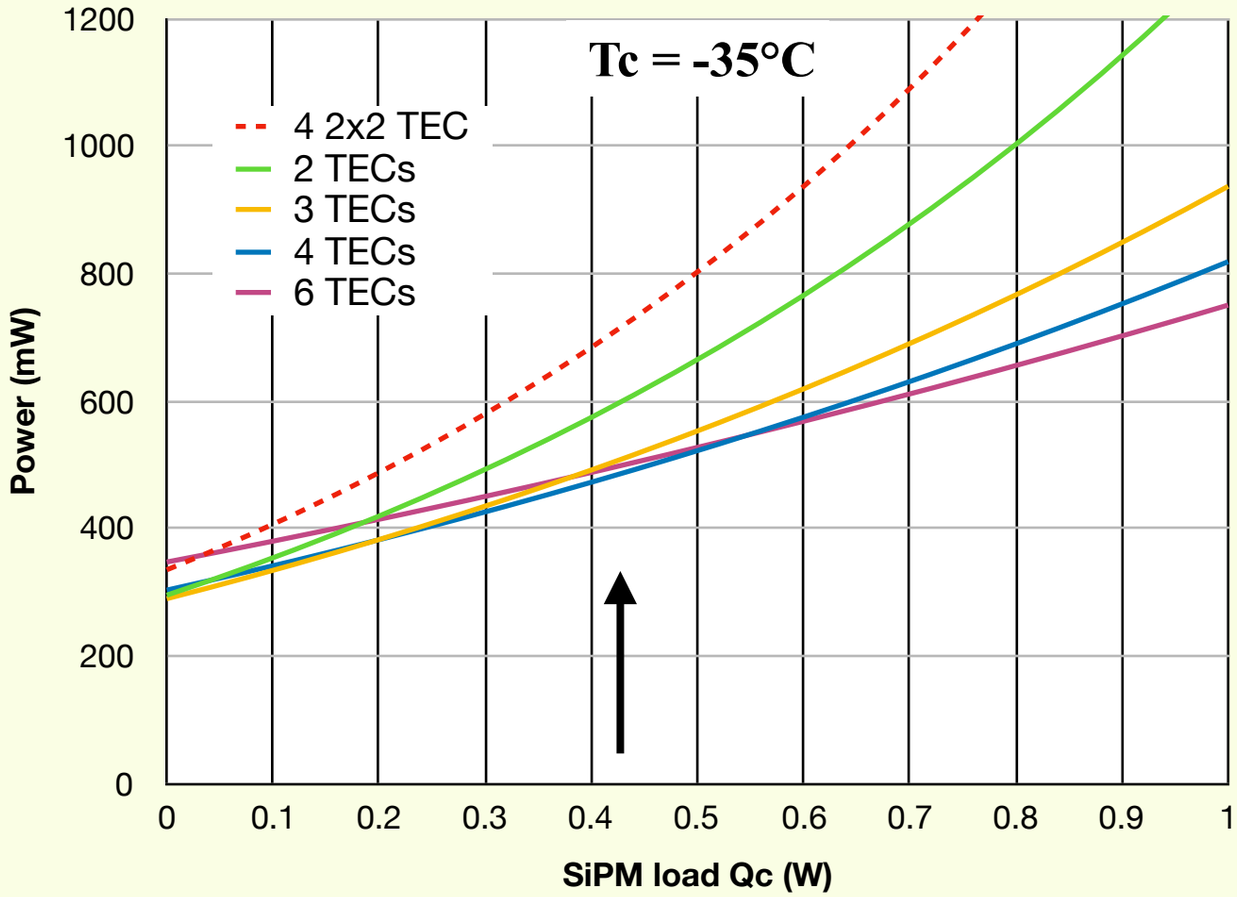
Simulation of thermal leakage at Th = -35°C , Tc = -45°C

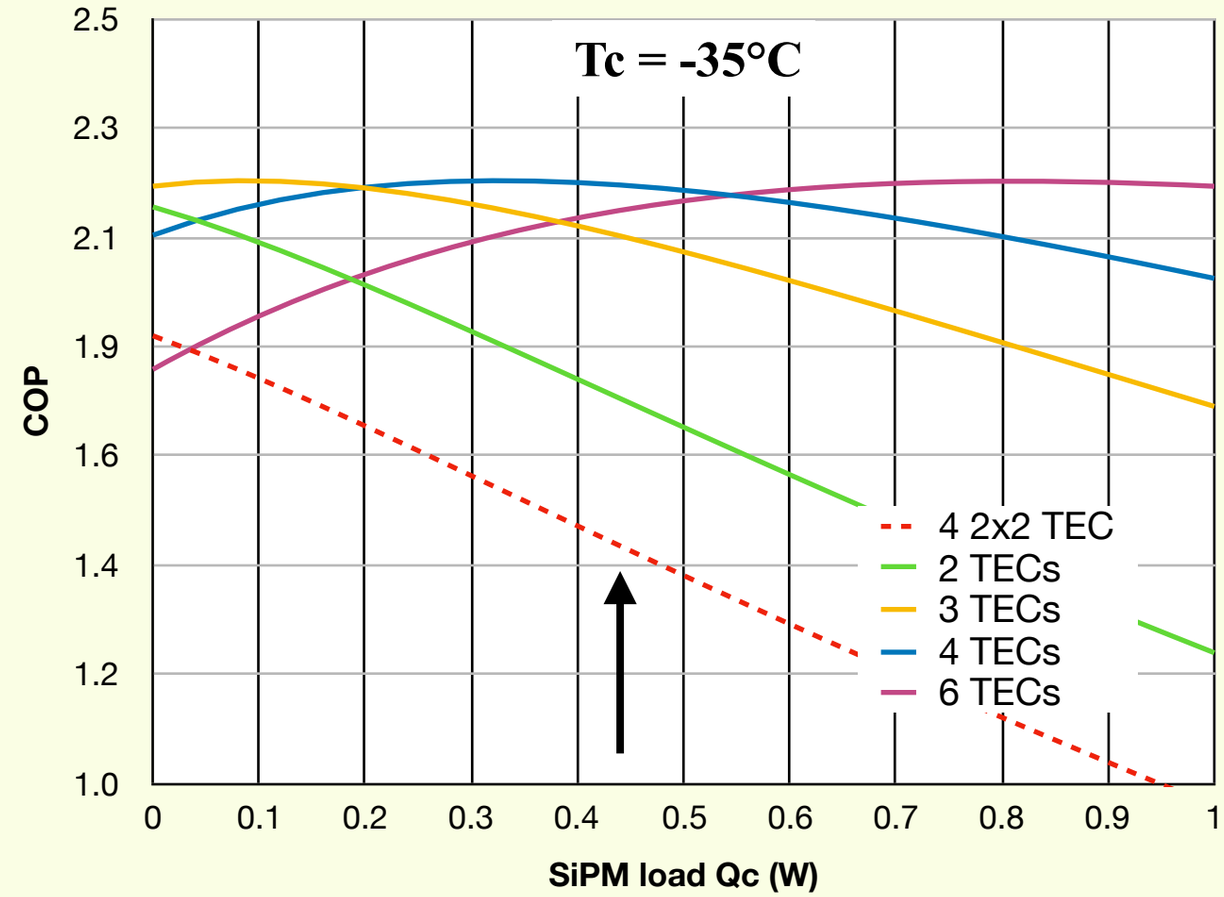




- Simulation of power consumption for different TEC configurations vs Qev
- The expected thermal leakage is 63 mW/°C
- A design with three or four 3x4 mm TECs is optimal to run at COPmax (more TECs will not help)

Qev = 0.063 W/K, ΔT=-10°C vs SiPM load





- Simulation of power consumption for different SiPM load
- A design with **four** 3x4 mm TECs more optimal when running at higher SiPM over voltage

Conclusions

- Due to high gain and power consumption of the SiPMs the use of TECs is a potential solution in a high irradiation environment.

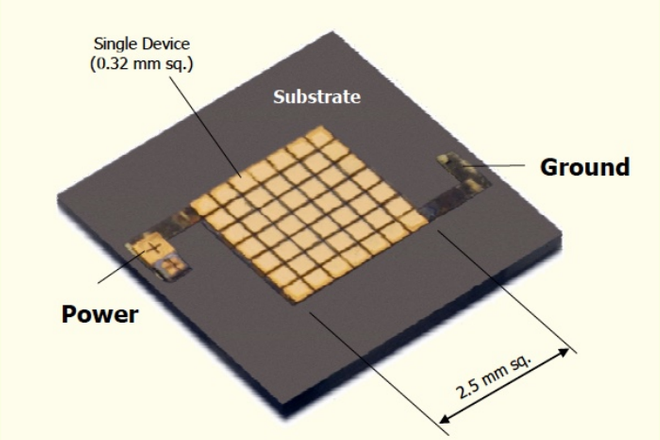
- R&D shows that a factor of 1.9 reduction in DCR for an additional -10C can be reached (Not completely but almost total power neutral using TECs)

- Some additional benefits and flexibility in annealing scenario's can be exploited by reversing the TEC current to create local heating at SiPMs to even further reduce the DCR.

- The TEC option is being seriously considered in the BTL (200 SiPM arrays with TECs have been ordered to build real modules)

- Further reduction of TEC size to nano structures could be explored

R&D should continue !



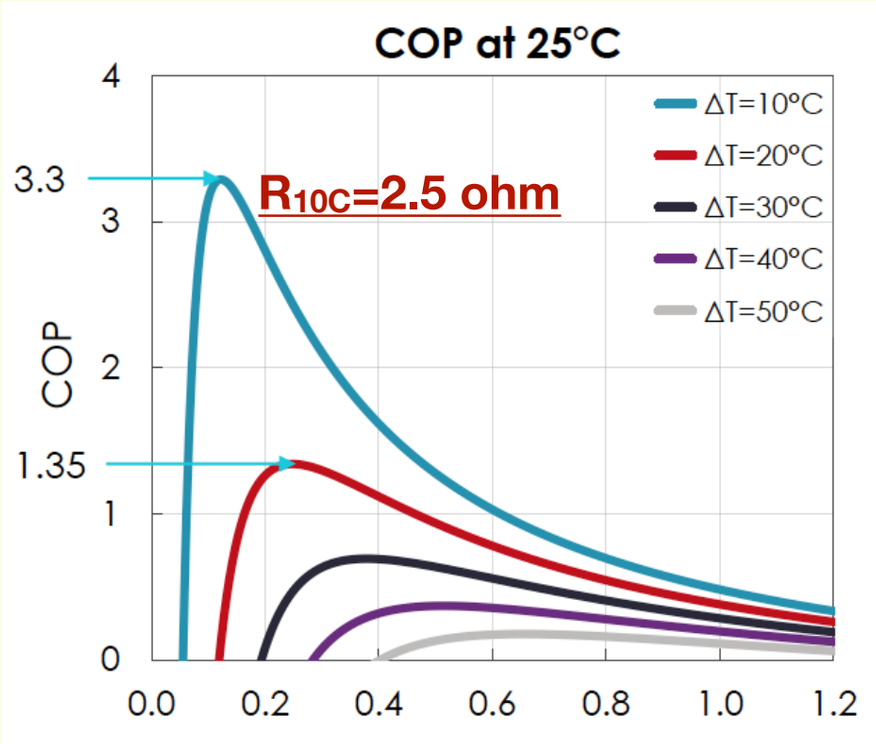
Nextreme micro-Cooler (7x7)

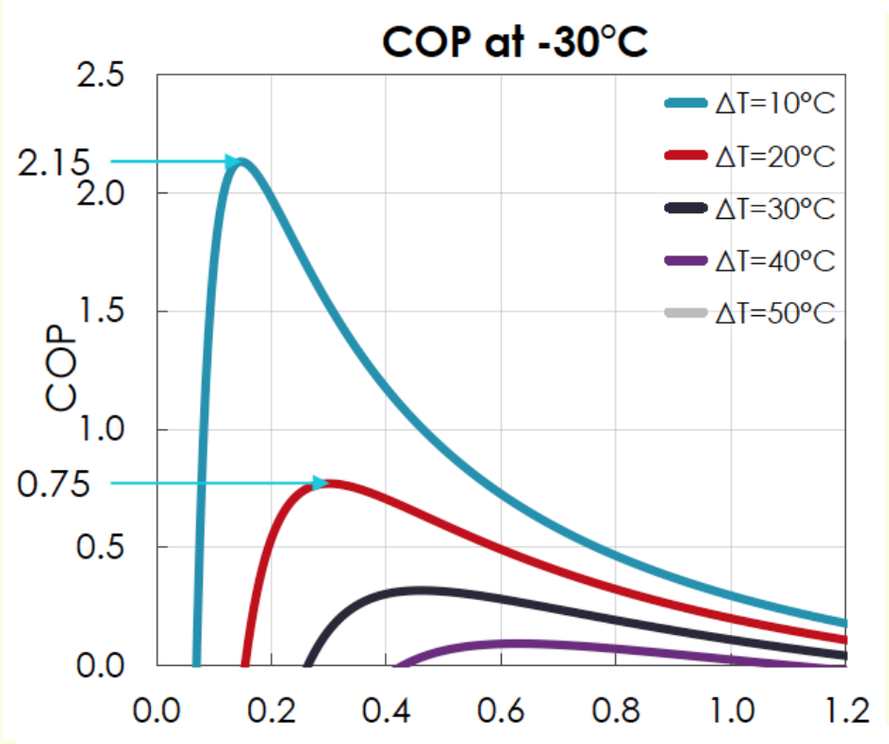
Backup

Phononic's simulation performance graphs

2x2 mm TEC

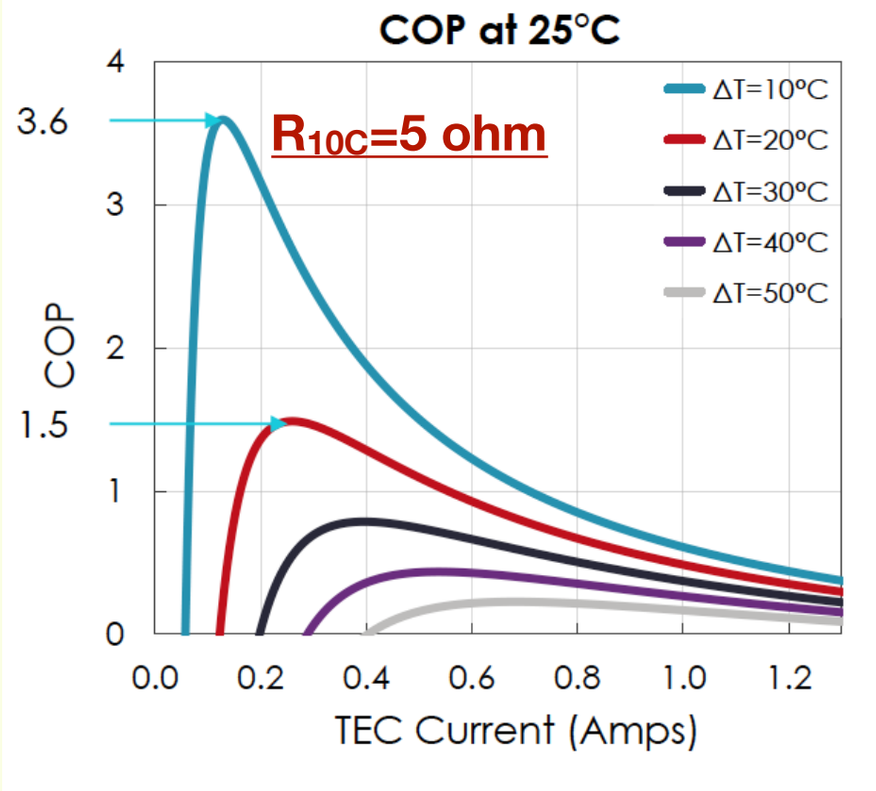
COP_{max} at 50mW/TEC

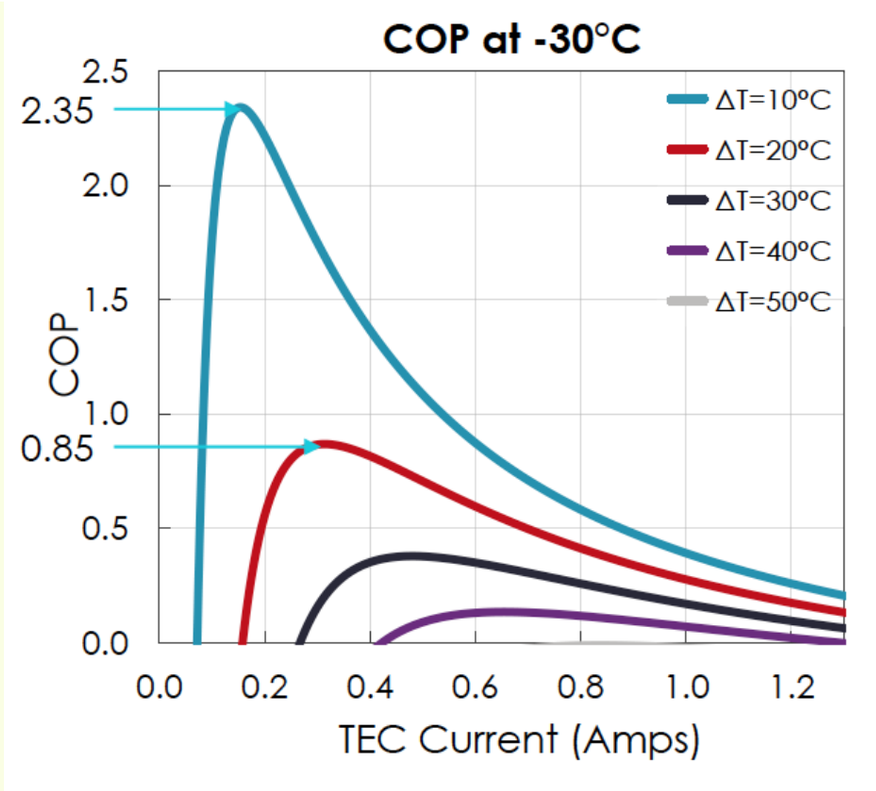




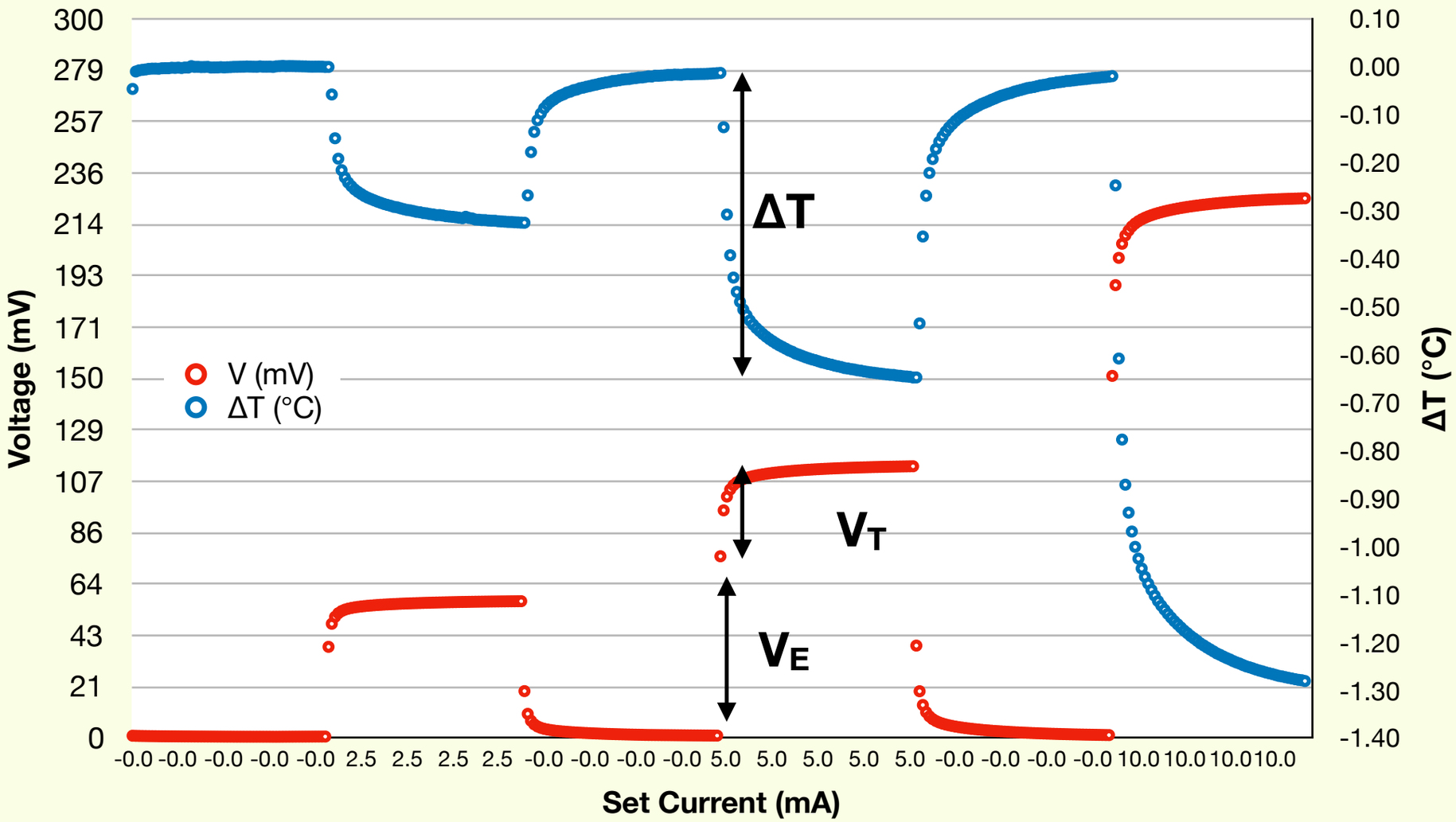
3x4 mm TEC

COP_{max} at 100mW/TEC





TEC Parameter scan done for 12 packages



$$V = \alpha\,\Delta T + I\,R_{AC}$$

α and R_{AC}

are Th dependent

12 package with 4 TEC measured

Package#	Rac / TEC	Seebeck /TEC
2	3.70	14.47
3	3.73	14.74
4	3.70	14.71
5	3.70	14.57
6	3.78	14.79
7	3.74	14.71
8	3.71	14.66
9	3.71	14.81
10	3.77	14.77
11	3.71	14.71
12	3.75	14.72
Average	**3.73**	**14.72**
sigma	**0.03**	**0.07**

$$Z.T = V_T/V_E \qquad Z = \alpha^2 / R_{AC}.(K+Q_{ev})$$

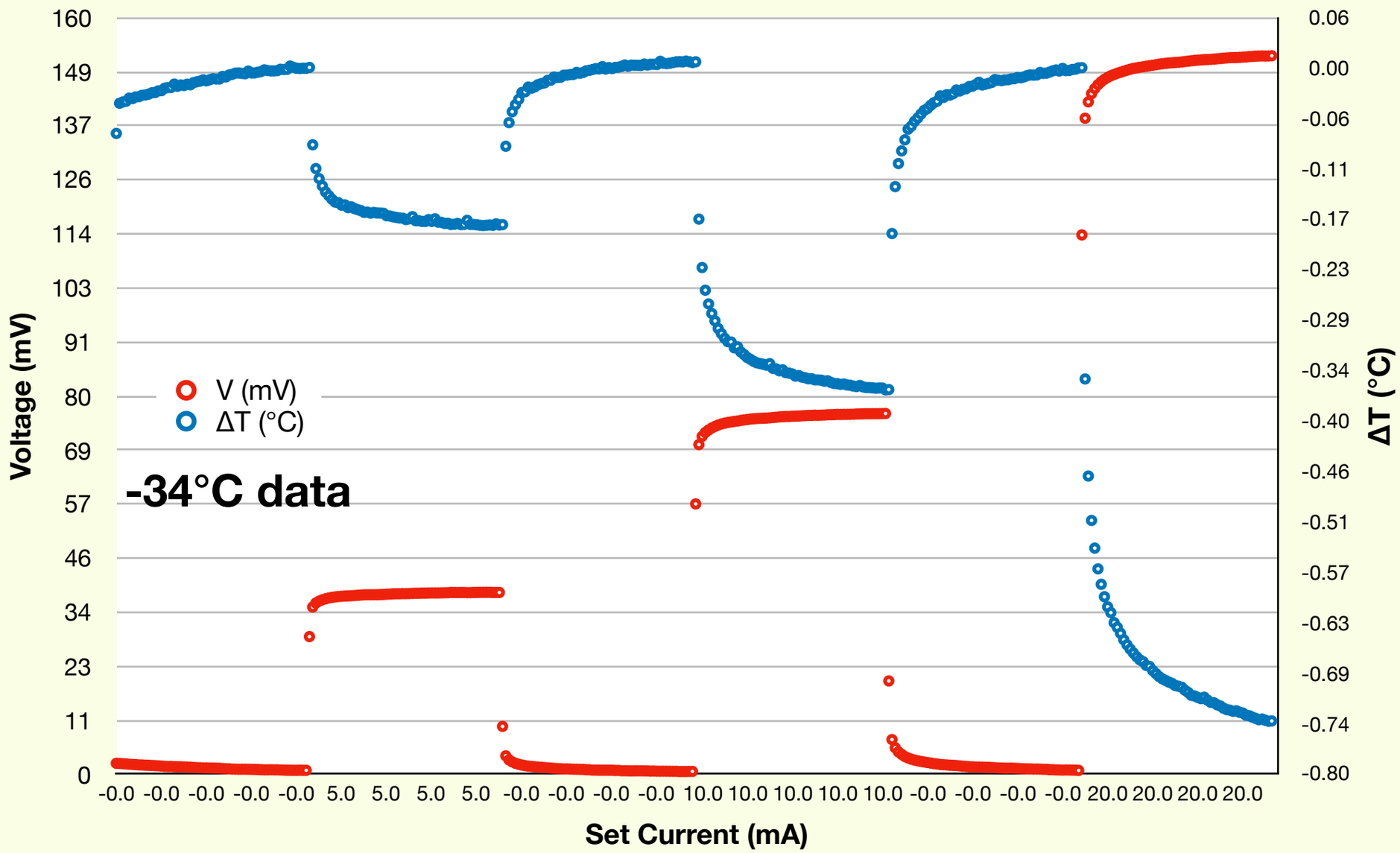
Temperature dependence of K
can be measured by direct measurement of VT/VE
then calculated assuming Qev is constant

3x4 parameter scan at -34C and -5C

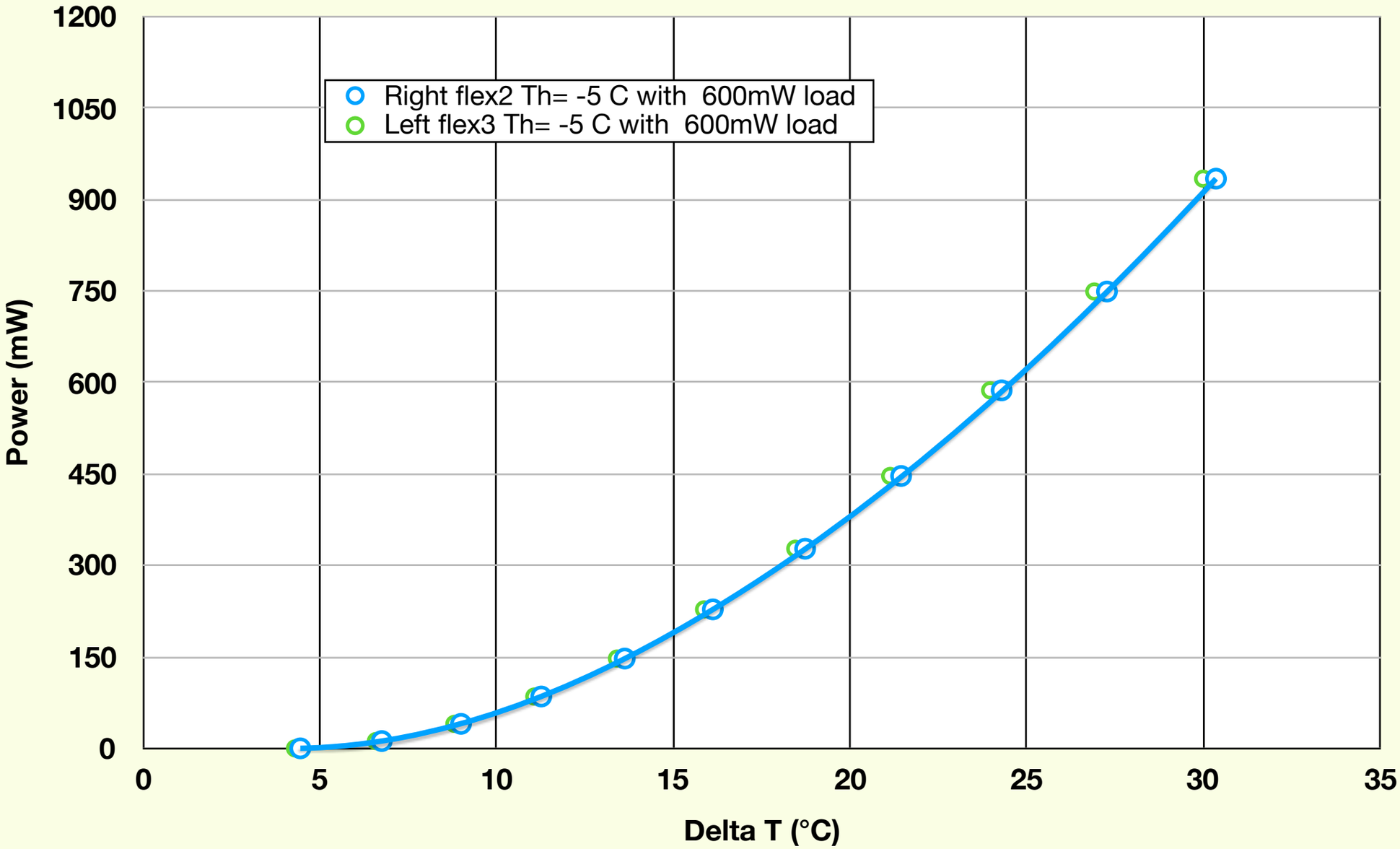
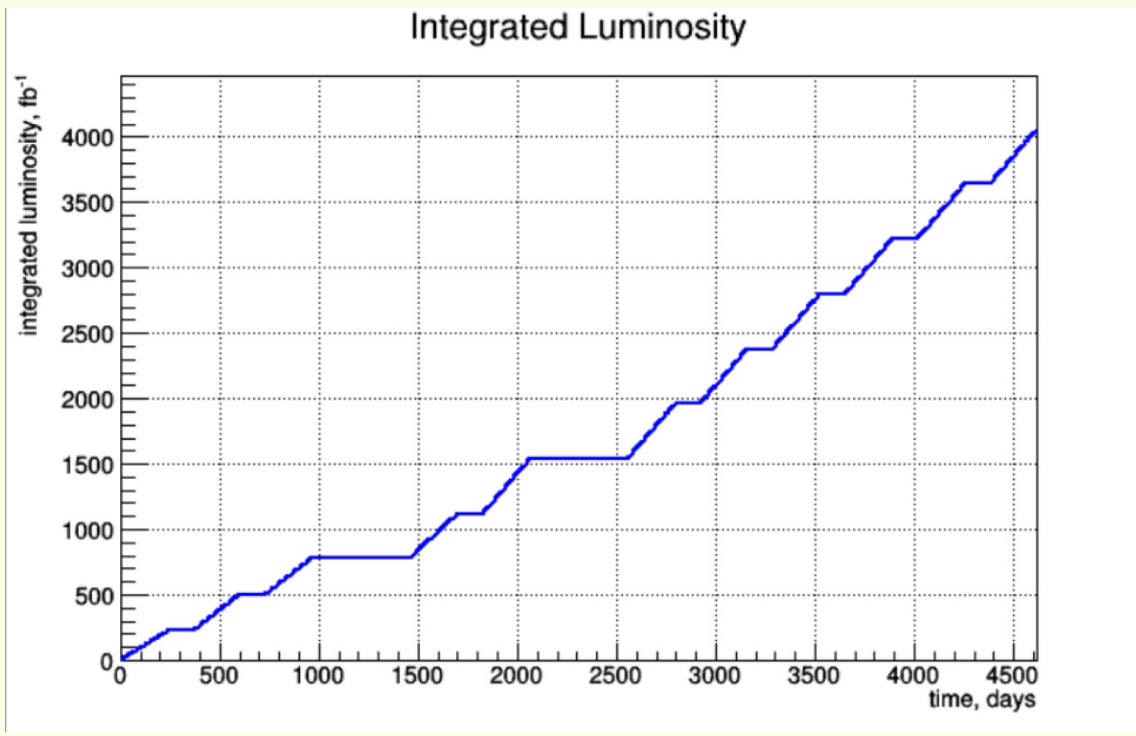
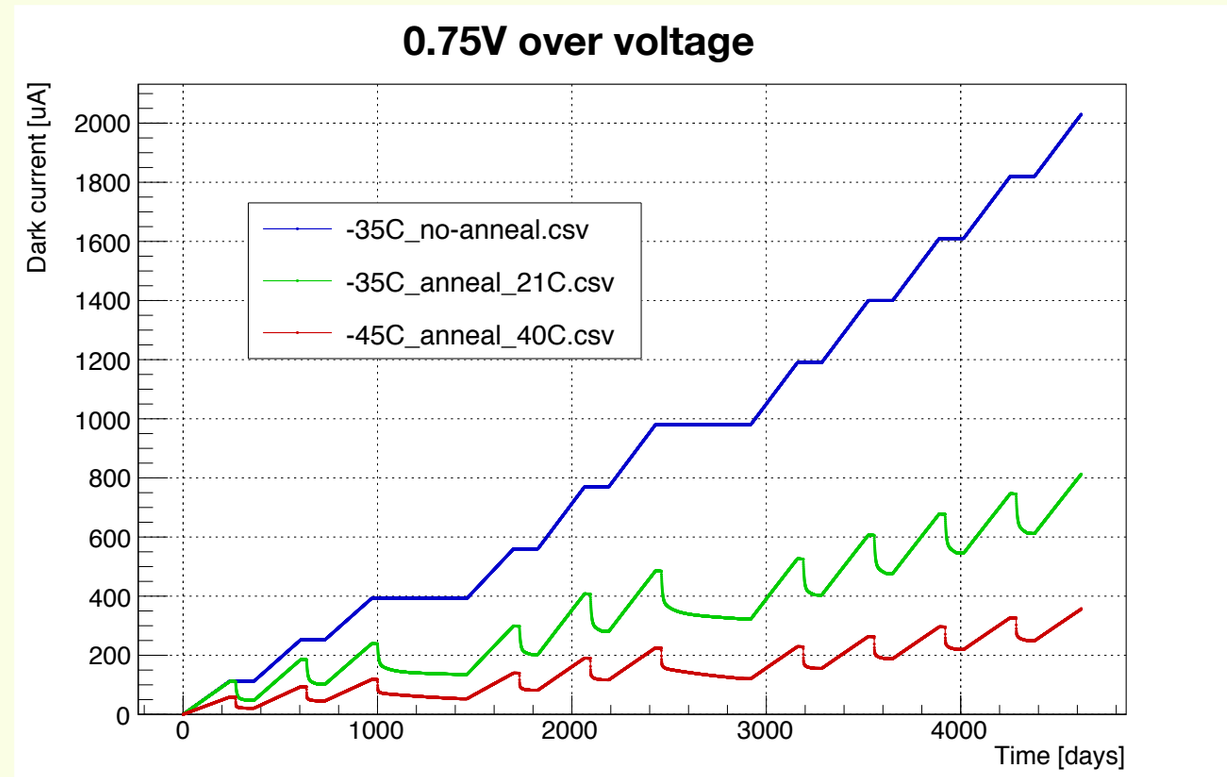
Parameter change per TEC / degree

$\Delta\alpha$ = 0.0395 mV/K

ΔRac = 0.0192 Ω



Reverse TEC with climate chamber at -5C



SiPM dark current