CPAD Instrumentation Frontier Workshop

SUNY Stony Brook

March 18-22, 2021

New Approaches to High Granularity Timing Detectors

Rafiqul Islam

Cactus Materials, Incorporated

Bruce A. Schumm

Santa Cruz Institute for Particle Physics
University of California, Santa Cruz

Representing SCIPP, Cactus Materials, and Brookhaven National Laboratory

and acknowledging the support of the US Department of Energy

Contributors

Gabriele Giacomini, Wei Chen

Brookhaven National Laboratory

Sager Ayyoub, Rafiqul Islam, Sujyot Mony

Cactus Materials Inc.

Carolyn Gee, Simone Mazza, Bruce Schumm, Yuzhan Zhao

Santa Cruz Institute for Particle Physics

Outline

Deep Junction LGAD

- Deep Junction (DJ) LGAD Concept
- Developments in DJ-LGAD Design
- DJ-LGAD Fabrication Progress

High-Density Interconnect

- Towards high-granularity readout
- High-Density Interconnect Plans and Progress

Conventional LGAD Coverage Gaps

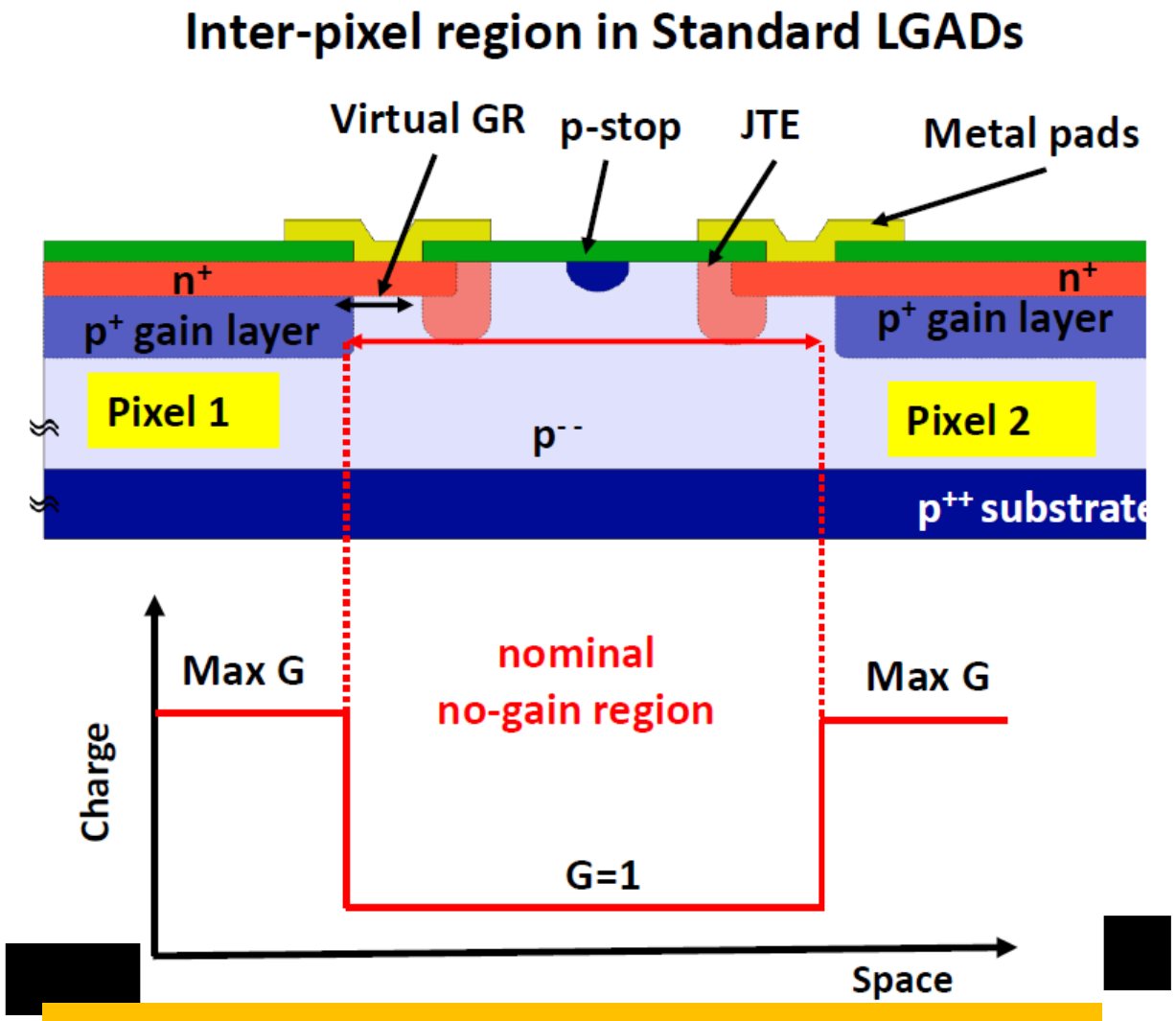
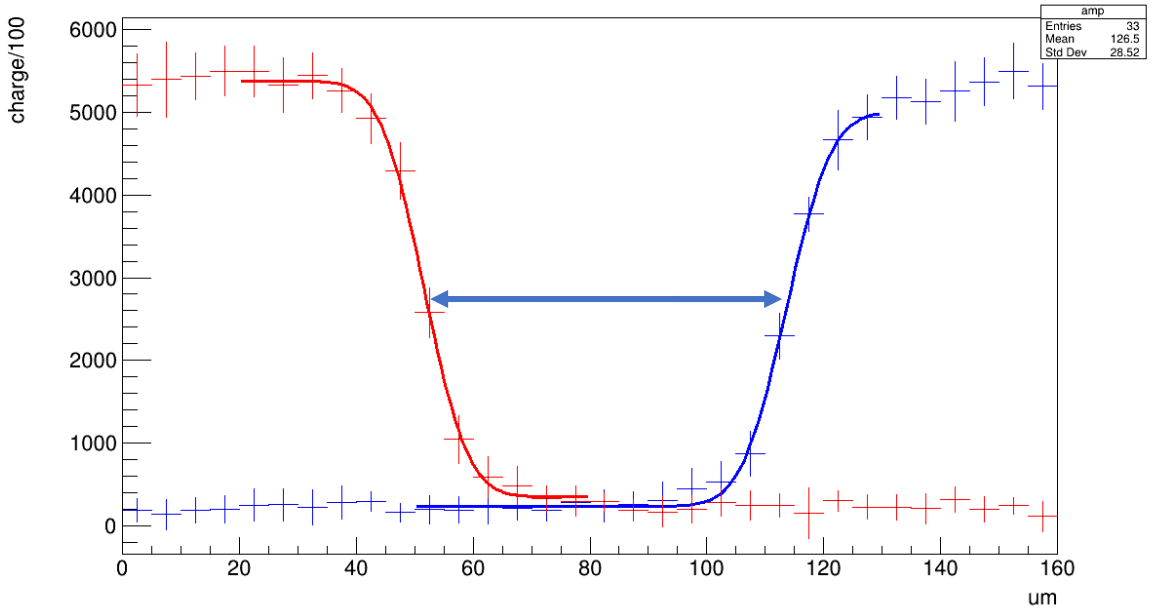


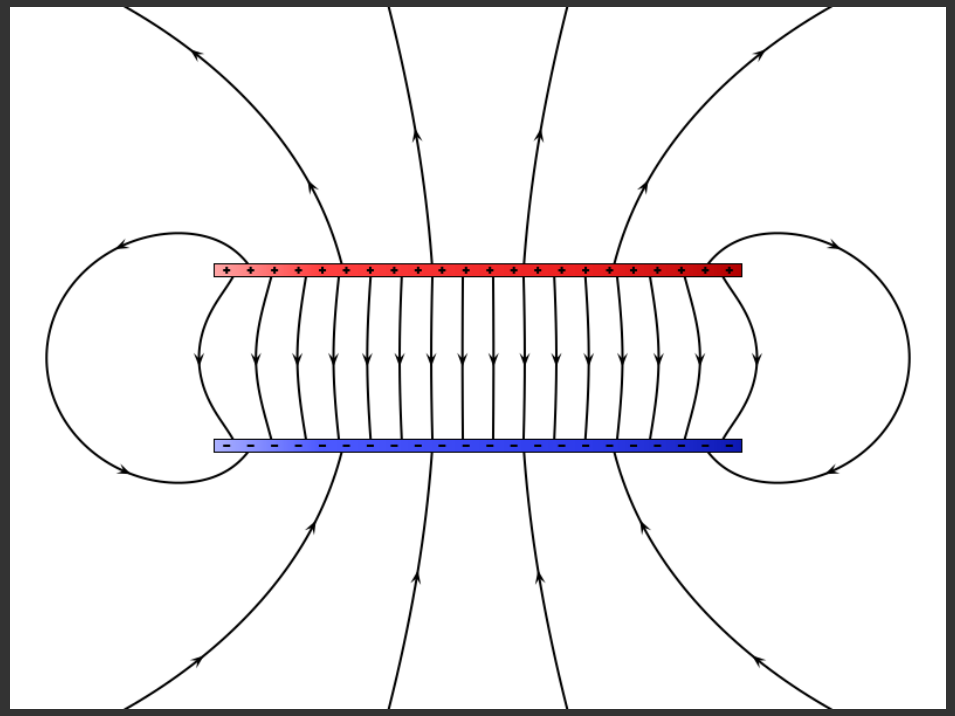
Diagram credit: FBK, Trento, Italy

Diagram credit: INFN, Torino



- Smallest safely achievable gap (50% criterion) is 60 µm
- Limits granularity to ~mm scale

The Deep Junction (DJ) LGAD Concept



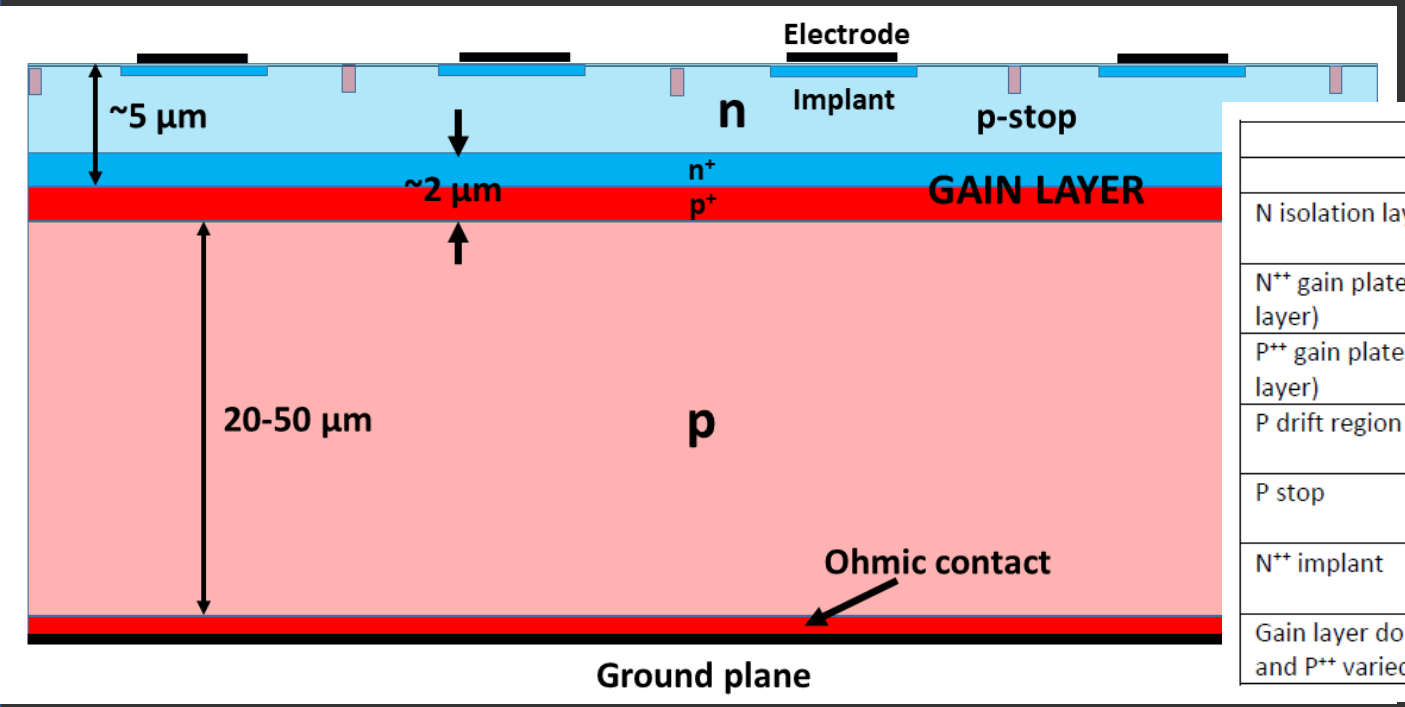
Basic inspiration is that of the capacitive field: Locally large, but surrounded by low-field region beyond the plates.

Idea:

- Use symmetric P-N junction to act as an effective capacitor
- Localized high field in junction region creates impact ionization
- Bury the P-N junction so that fields are low at the surface, allowing conventional granularization

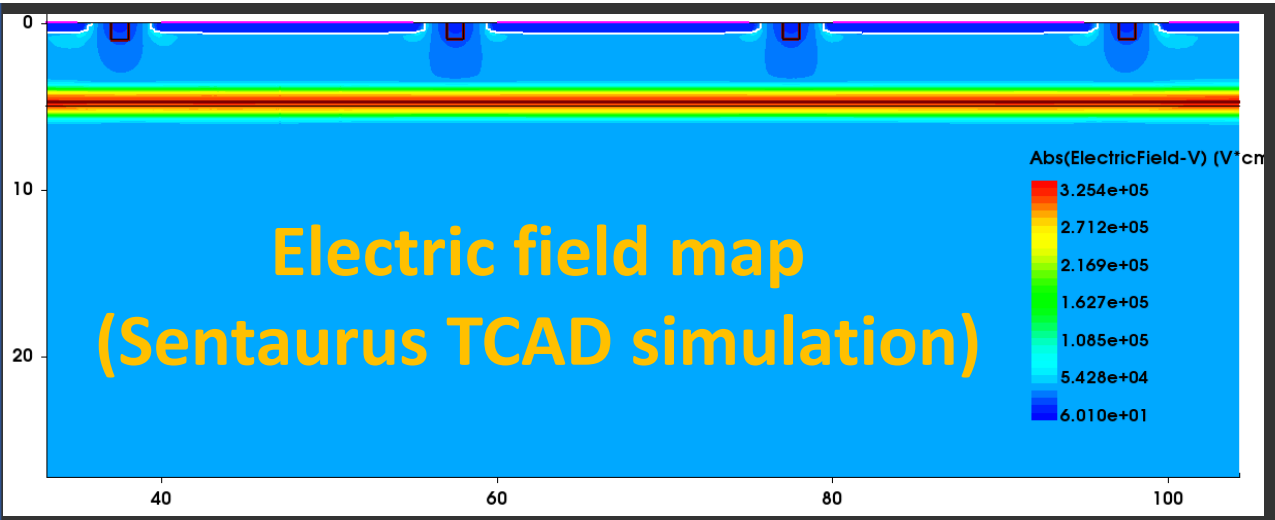
➔ **"Deep Junction" LGAD (DJ-LGAD)**

DJ-LGAD Conceptual ("Baseline") Design

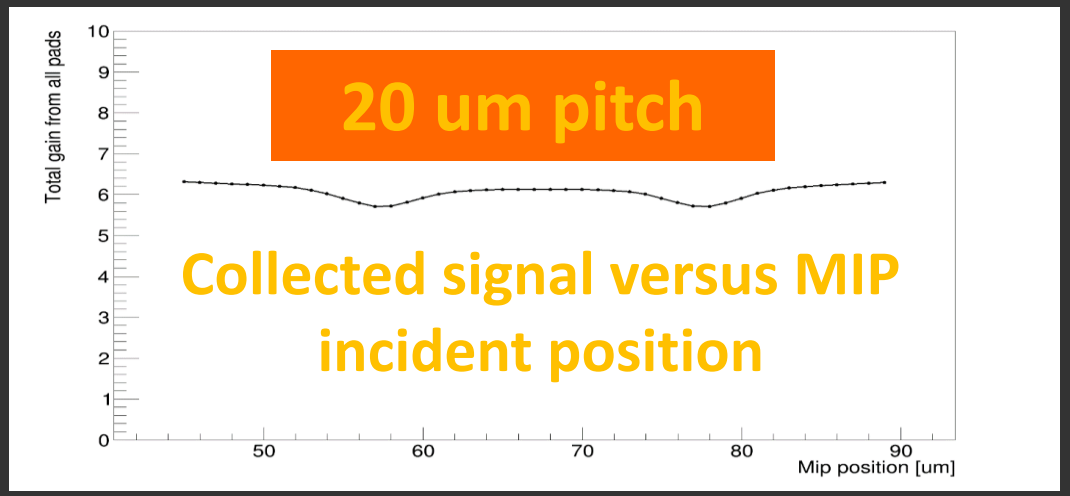


DJ-LGAD Baseline Design

Element	Doping Level	Extent in Depth
N isolation layer	Constant doping of density 3e12 N/cm^3	From 0 µm (surface) to beginning of N^{++} "gain plate" layer
N^{++} gain plate (upper half of gain layer)	Gaussian doping, peak of 3.0e16 N/cm^3	Peak at 4 µm, Gaussian width of 0.17 µm
P^{++} gain plate (lower half of gain layer)	Gaussian doping, peak of 3.0e16 N/cm^3	Peak at 5.5 µm, Gaussian width of 0.17 µm
P drift region	Constant doping of density 3.0e12 N/cm^3	End of P^{++} "gain plate" layer to 50 µm
P stop	Constant doping of density 1.0e13 N/cm^3	1 µm deep, 1µ wide
N^{++} implant	Constant doping of density 1.0e19 N/cm^3	At surface
Gain layer doping tolerance (N^{++} and P^{++} varied together)	Effective operation between 2.9e^16 and 3.5e^16	



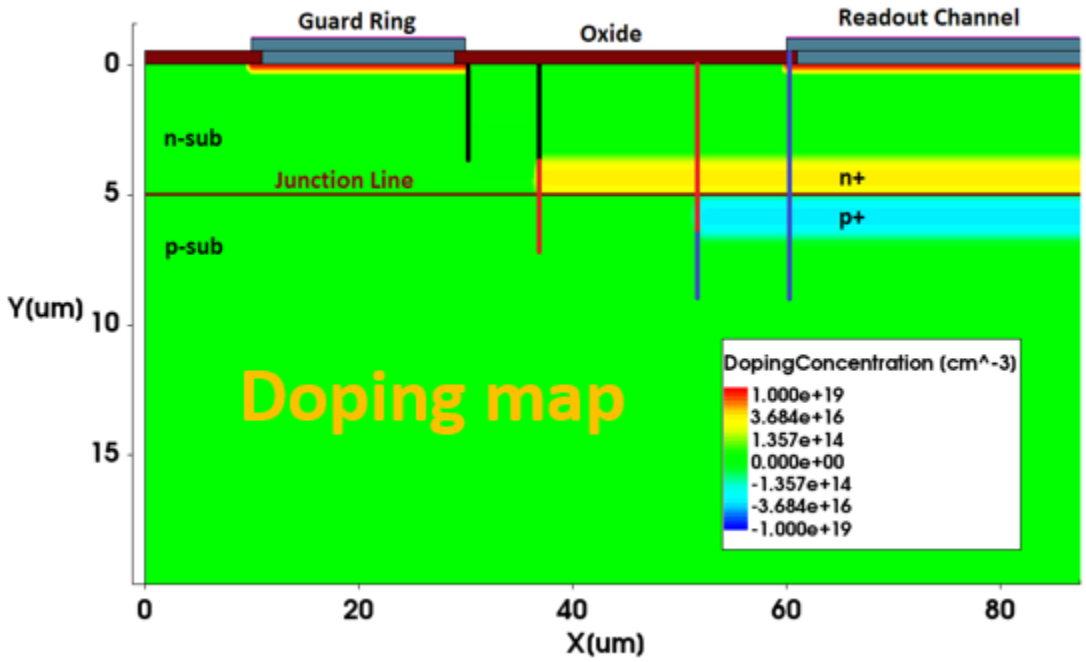
Electric field map
(Sentaurus TCAD simulation)

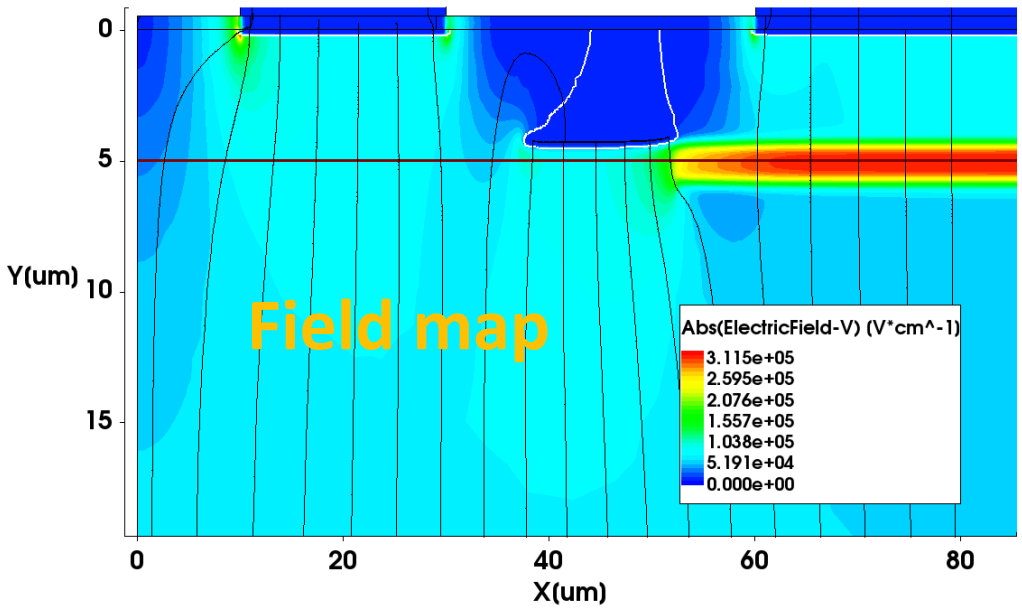


20 um pitch

Collected signal versus MIP incident position

Deep Junction LGAD: Junction Termination

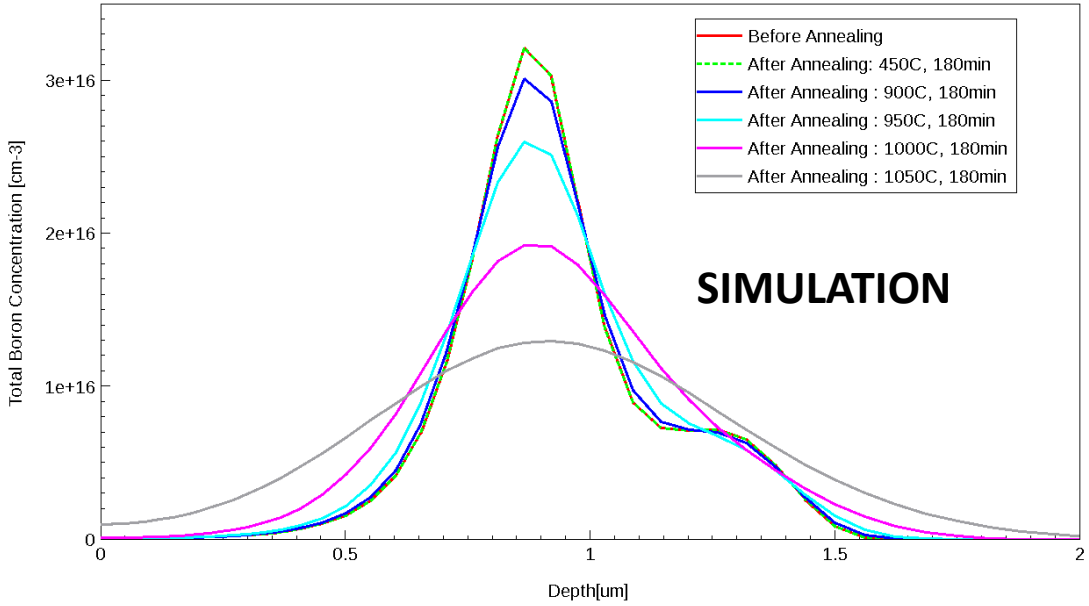


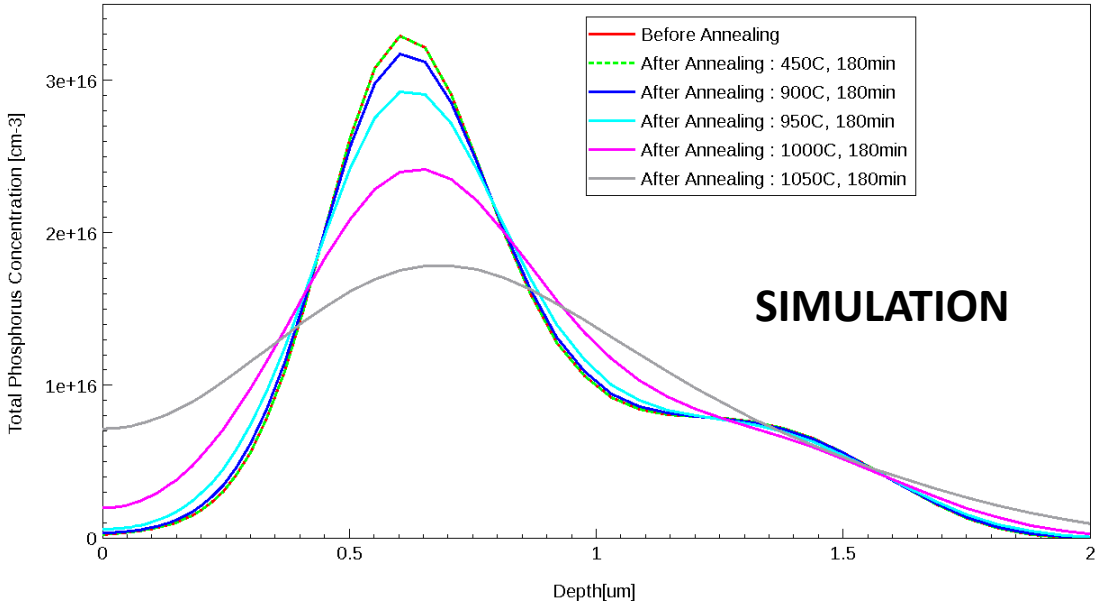


- Junction termination at periphery of structure needed to avoid breakdown
- Guard ring mediates field a periphery
- Insensitive region of about 50 µm only at edge of sensor (not between channels!)

Wafer/Wafer Bonding Approach: Doping Profiles

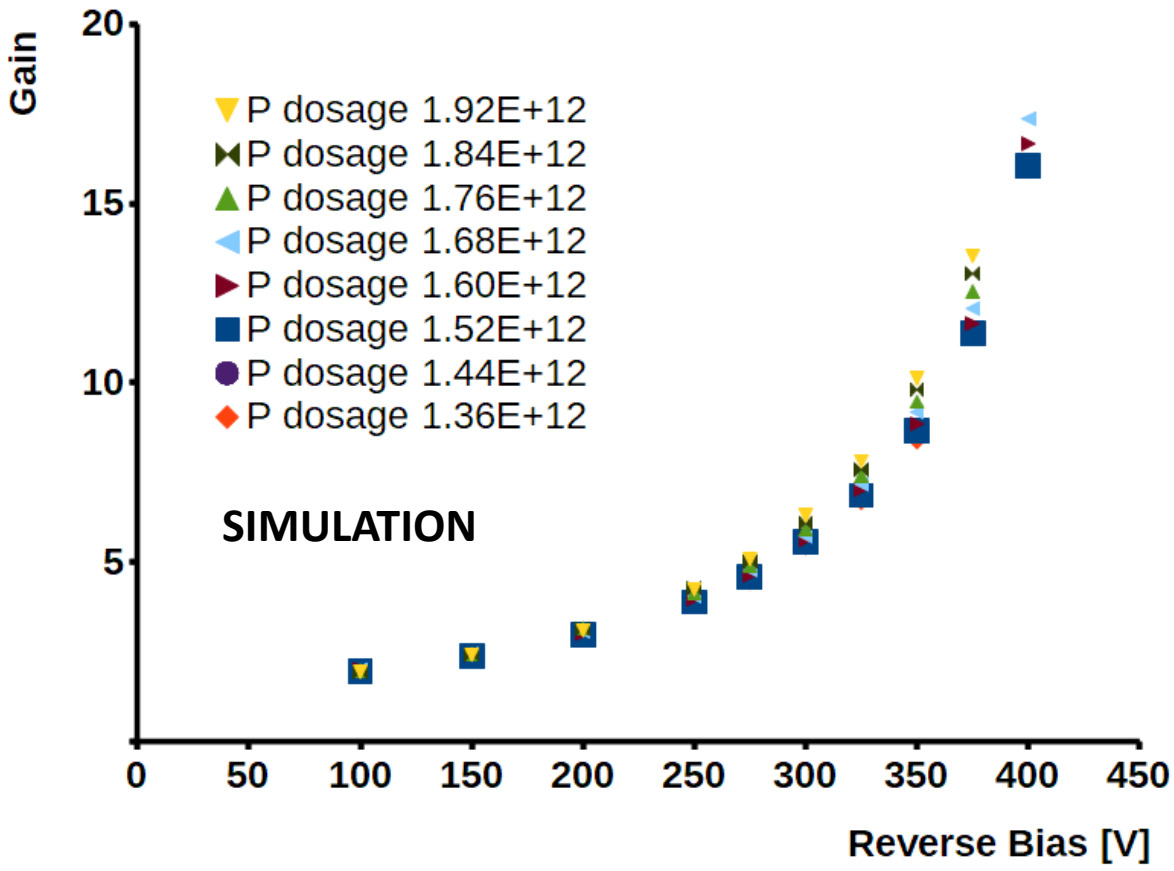
- Boron (p) and phosphorus (n) implantation on separate wafers
- Fused and annealed to form deep junction
- Maximum annealing temperature 900^0C





Implantation energies: **Boron:** 735 keV **Phosphorus:** 450 keV

DJ-LGAD Gain (Simulation)



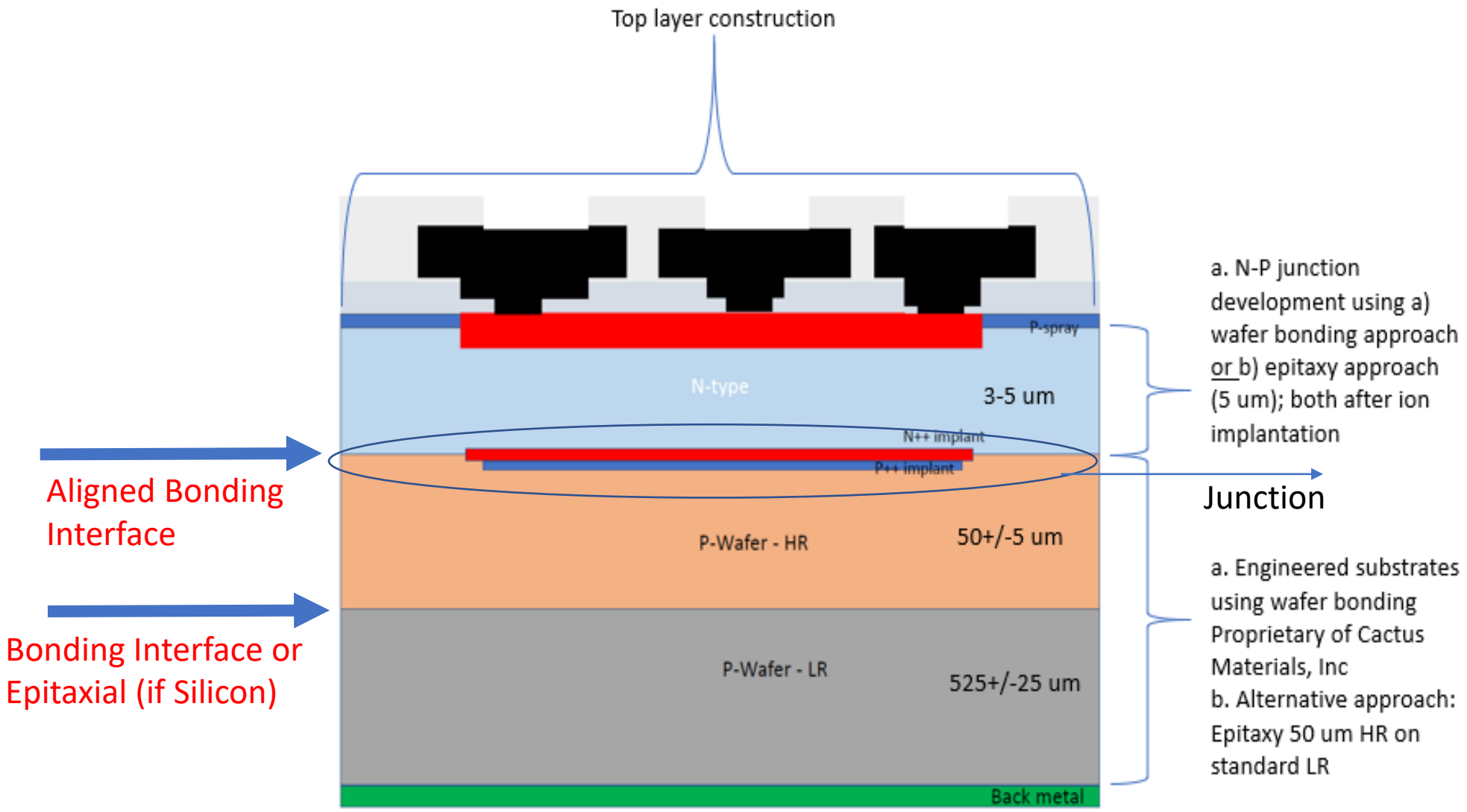
- Gain shown as a function of boron beam fluence (cm^{-2})
- Phosphorus fluence fixed at 1.52×10^{12}
- Stable operation over a range of doping levels

DJ-LGAD Fabrication Approaches

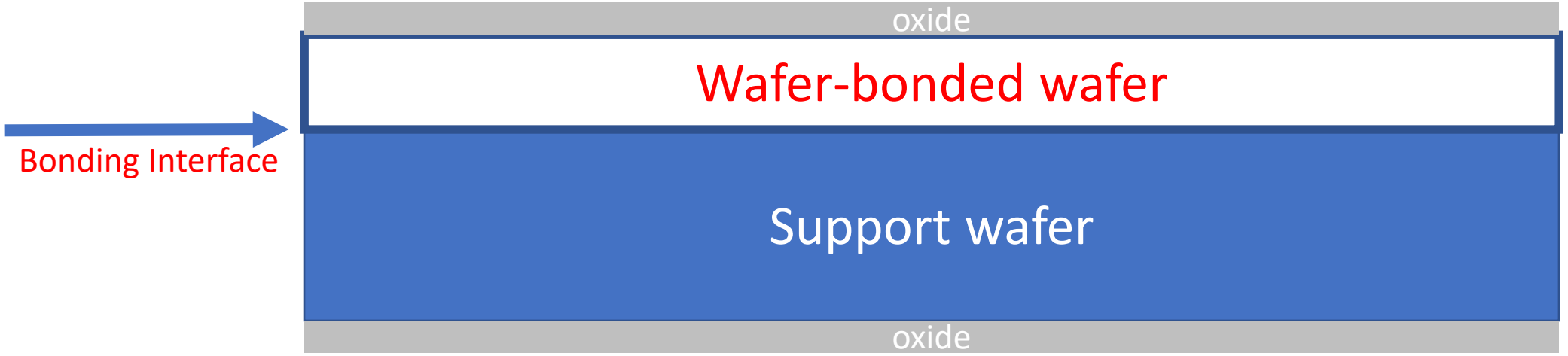
Two approaches will be employed:

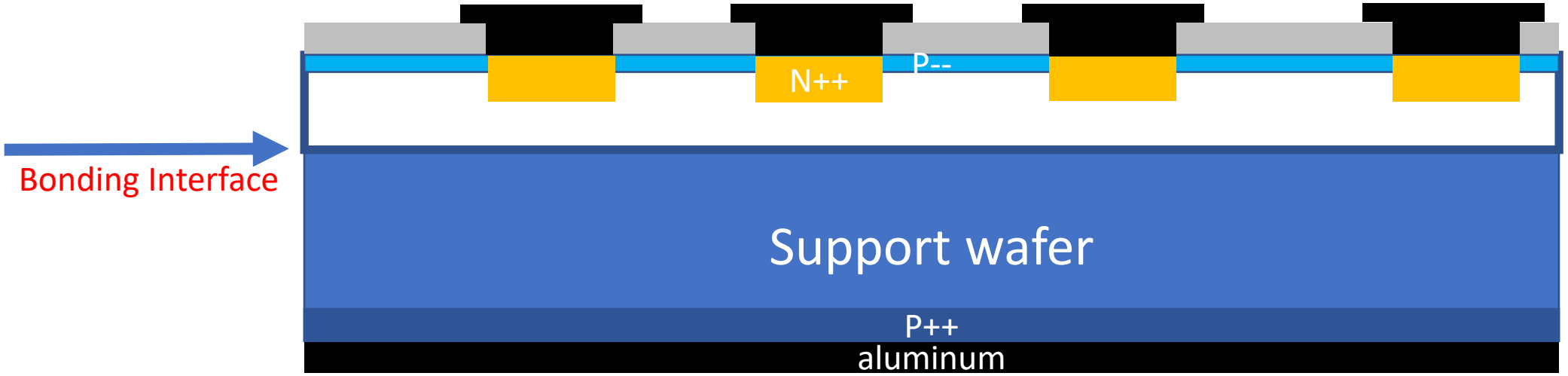
- Wafer Bonding method (transformational for many types of detectors)
- Epitaxial method

Wafer Bonding Approach



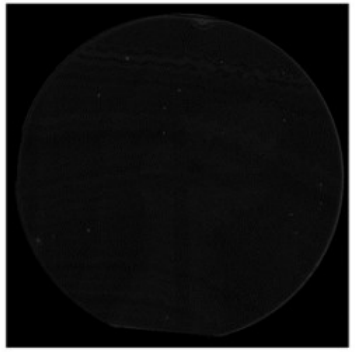
Bonded Test Diode



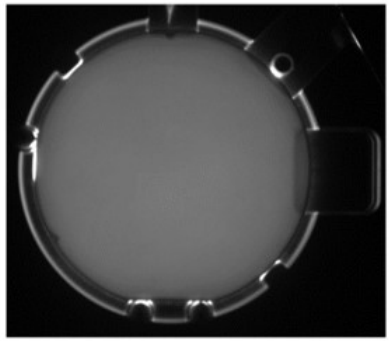


Fabrication

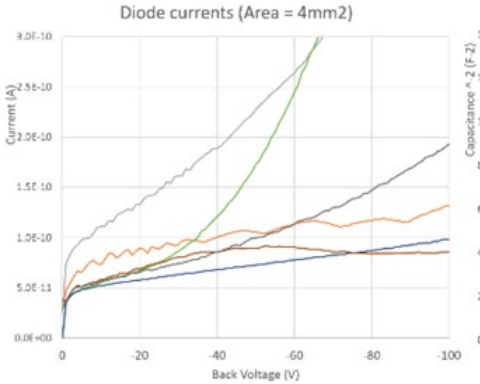
Surface Acoustic microscopy

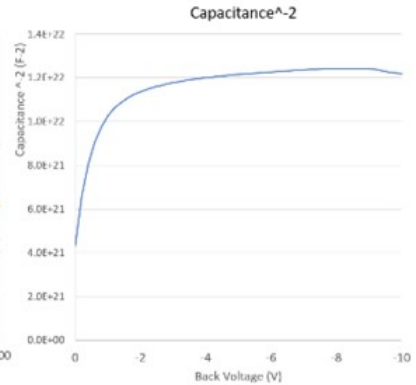


IR microscopy



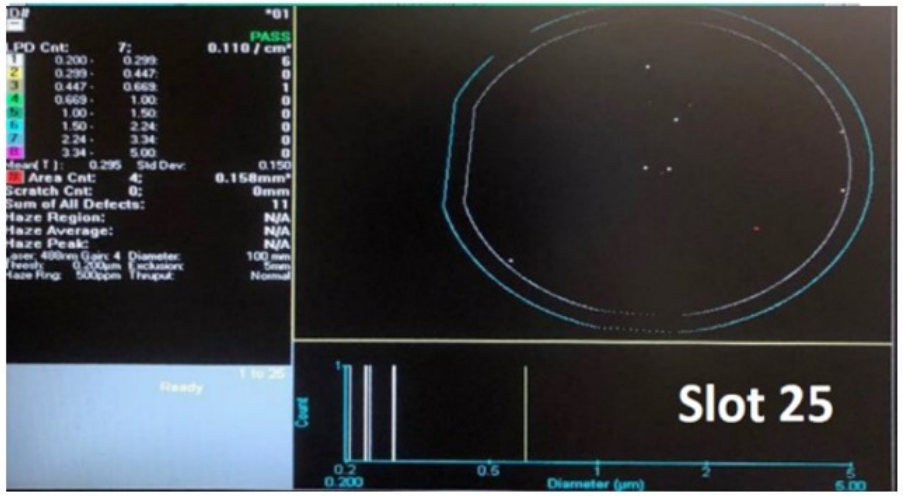
. SAM and IR Characterization shows absence of void



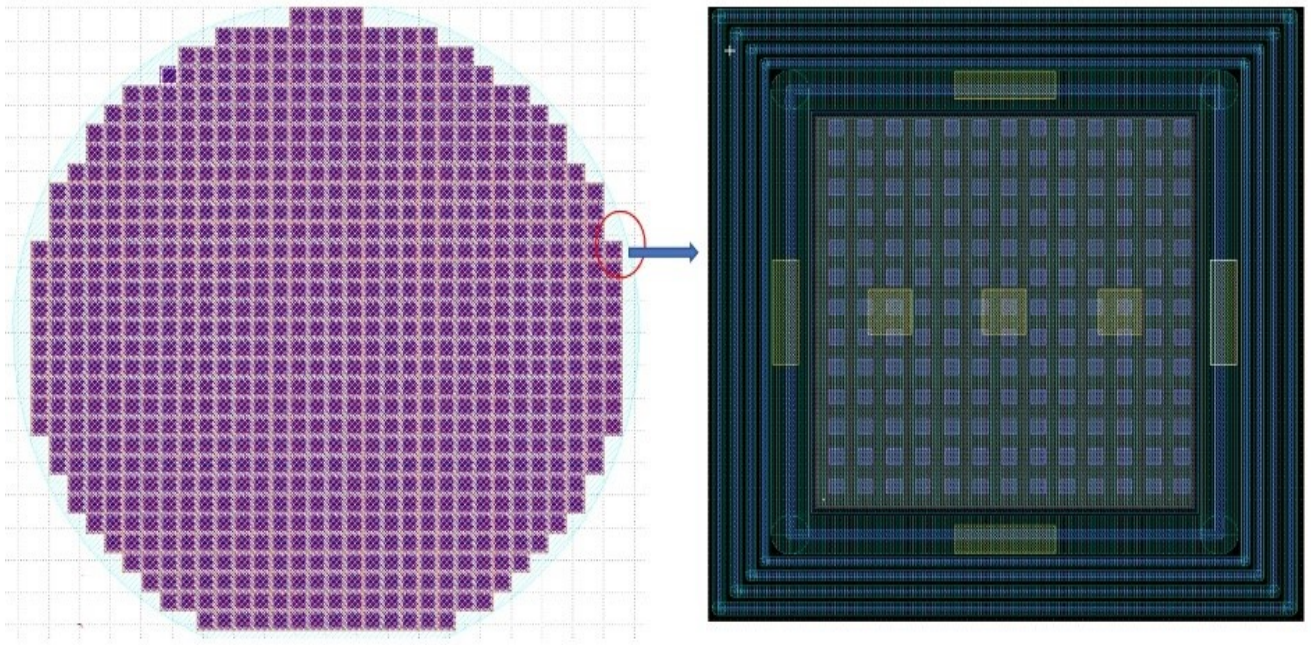


I-V and $1/C^2$-V from process A

Wafer ID	Processed Side Thickness (um)*	Light Point Defect Count	Sum of All Defects	Median Surface Roughness Ra (A)
Wafer 1	50.6	28	31	3.1
Wafer 2	48.0			
Slot 5	51.2			
Slot 7	49.4			
Slot 11	52.6	31	37	2.5
Slot 13	53.4			
Slot 15	49.6			
Slot 21	49.0			
Slot 23	52.4			
Slot 25	49.8	7	11	3.8
Average:	50.6	22	26	3.1



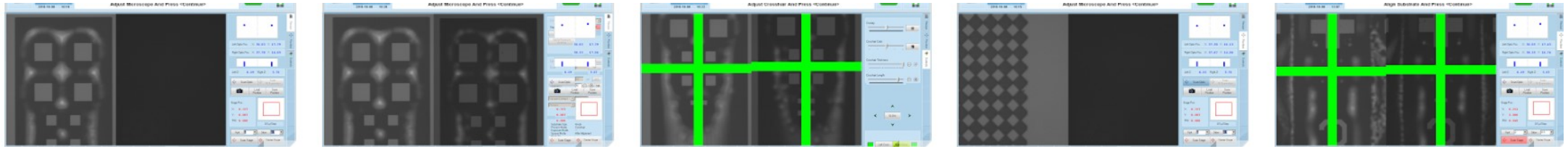
DJ-LGAD Fabrication Approaches



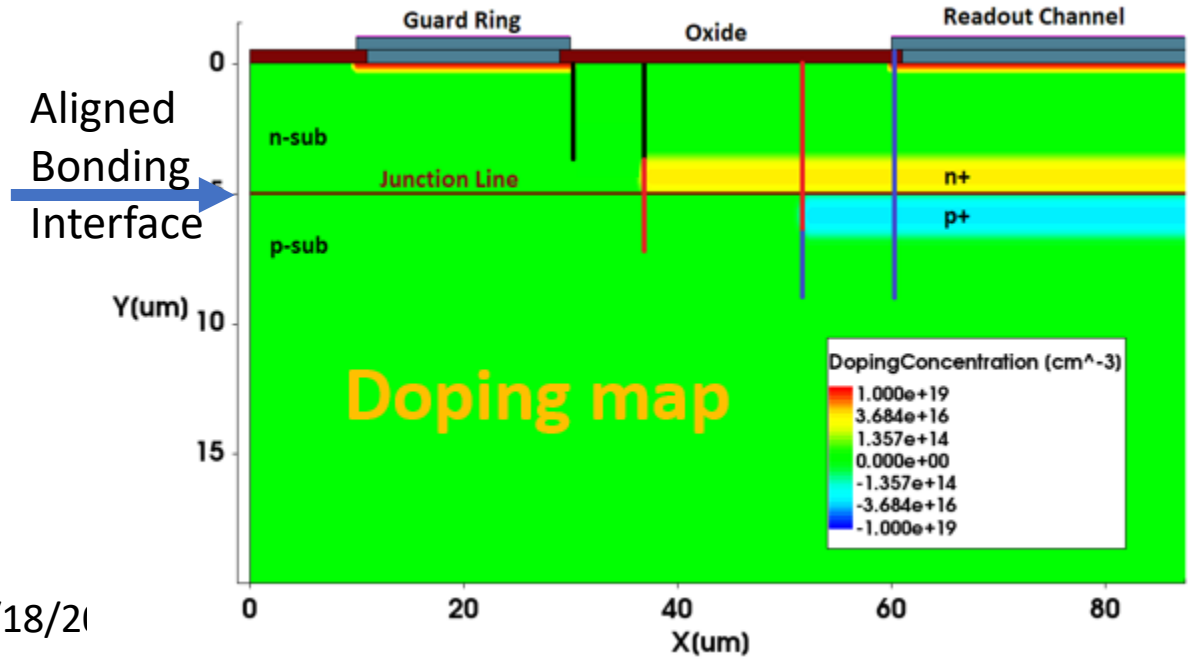
Design of planar DJ-LGAD in mask layout during Phase I development

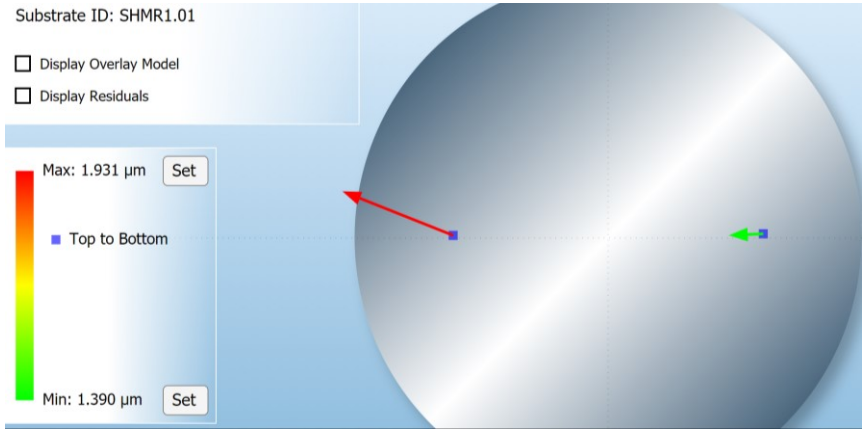
Aligned Wafer Bonding between p+ and n+ type wafers for deep junction development

- Pre-bonding alignment



- Bottom Right 2 Bottom left Alignment front to back misalignment ~1.5 um



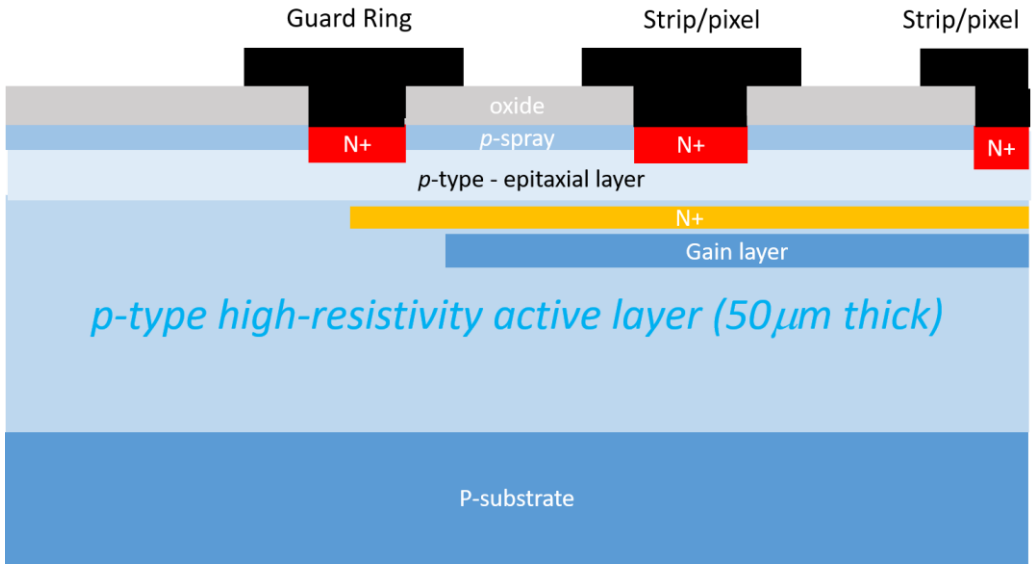


Under Process..

- CMP
- Implantation (Innovion)
- Lithography
- Sputtering for contacts
- Oxide passivation (PECVD)

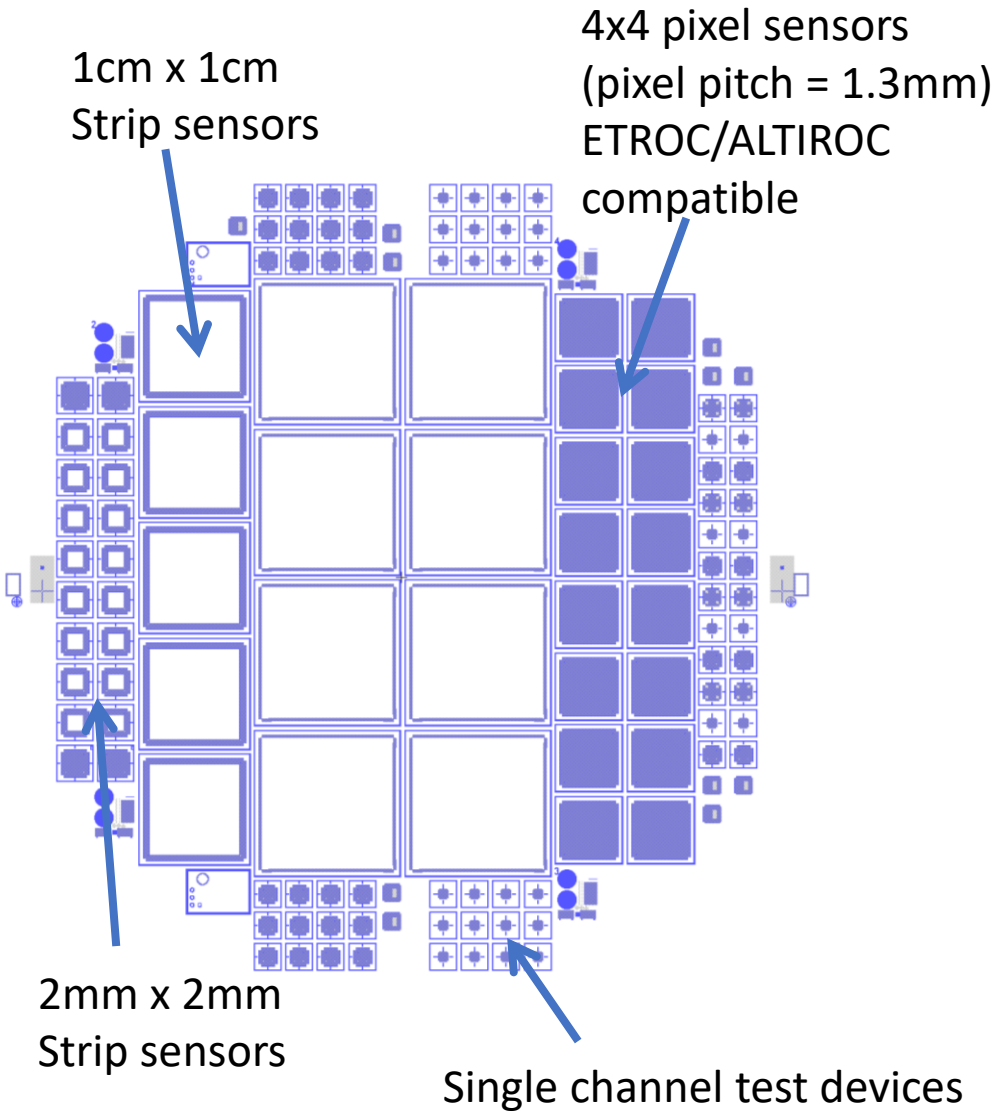
Epitaxial Approach

Deep junction created on conventional wafers used for LGADs.
Over the junction, a 5-µm thick p-type HR epitaxial layer has been grown (Cactus Materials).
n+ electrodes (strip and pixels) are then implanted and DC-contacted by aluminum.

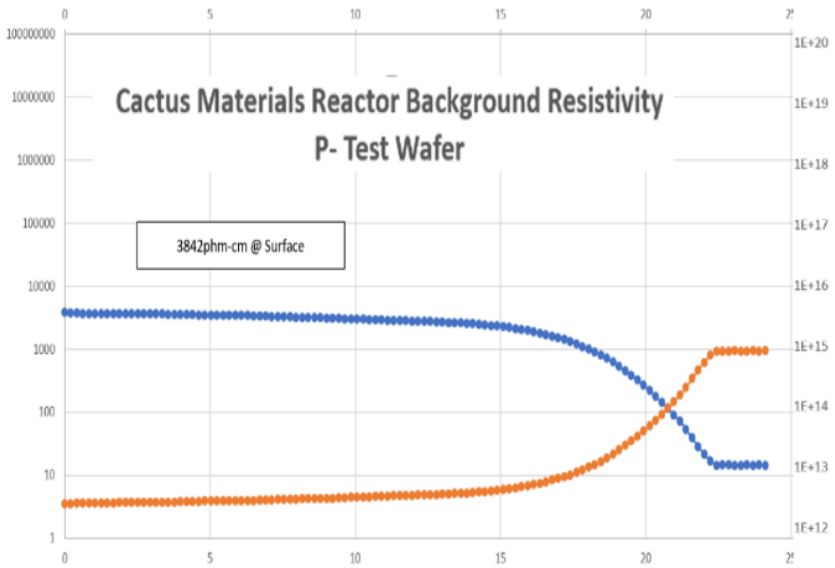


Under process…

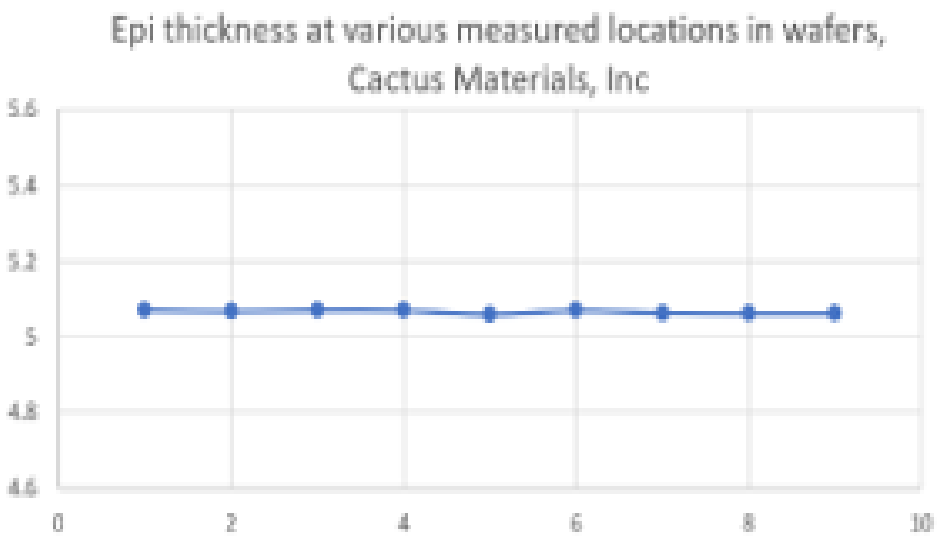
Mask layout – 4” wafer



Epitaxial Approach



Spreading resistance profile on epilayer



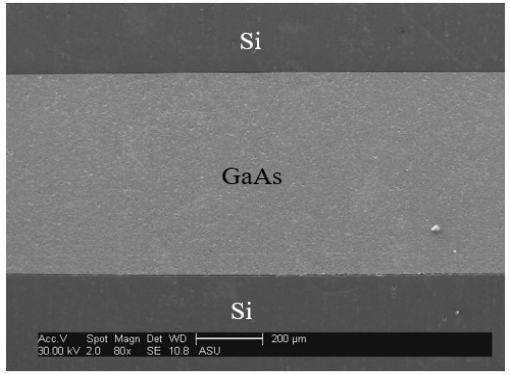
Thickness by FTIR after deposition

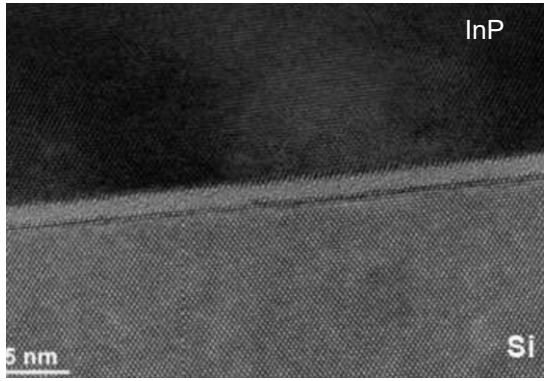
Under Process..

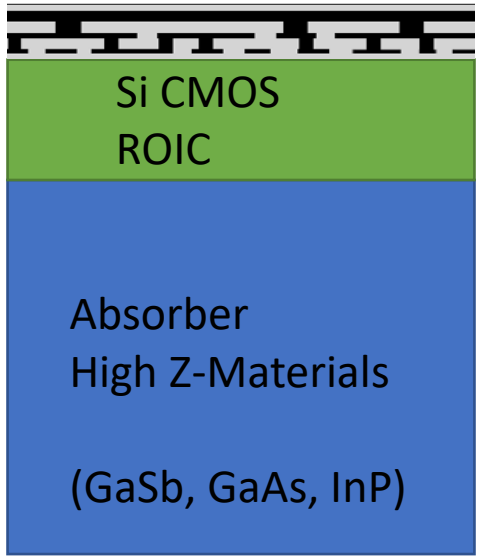
- CMP
- Implantation (Innovion)
- Lithography
- Sputtering for contacts
- Oxide passivation (PECVD)

Wafer Bonding Capability for other high Z-absorber pixel detectors

- This wafer bonding capability can be extended to other absorber High-Z materials (III-V materials; GaSb, GaAs, InP)







3D Integration

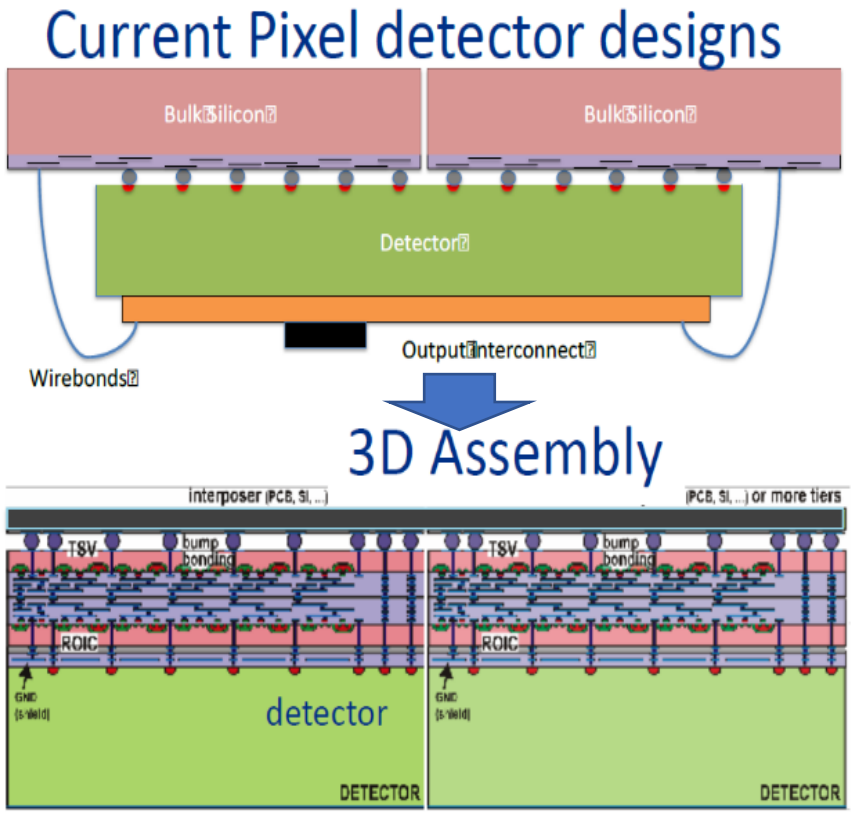
3D integration Driver

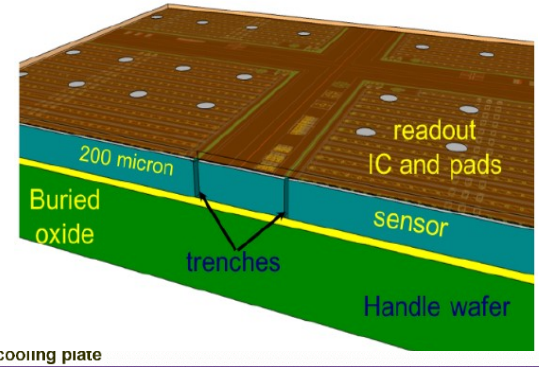
Key Questions:

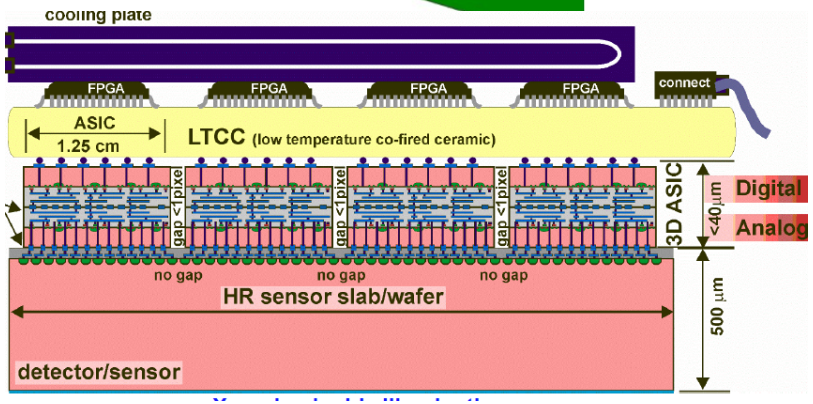
- How to minimize data movement while maximizing information transfer?
- What novel electronic/optical states of matter can be manipulated to design non-traditional interconnects at the atomic, micro, and macro scales?

- Enabling of new forms of self-supporting structures
- Highly-packed in-situ processing (on focal plane), bringing together hetero-material device interfaces
- Significant data reduction

3D integration Schematic

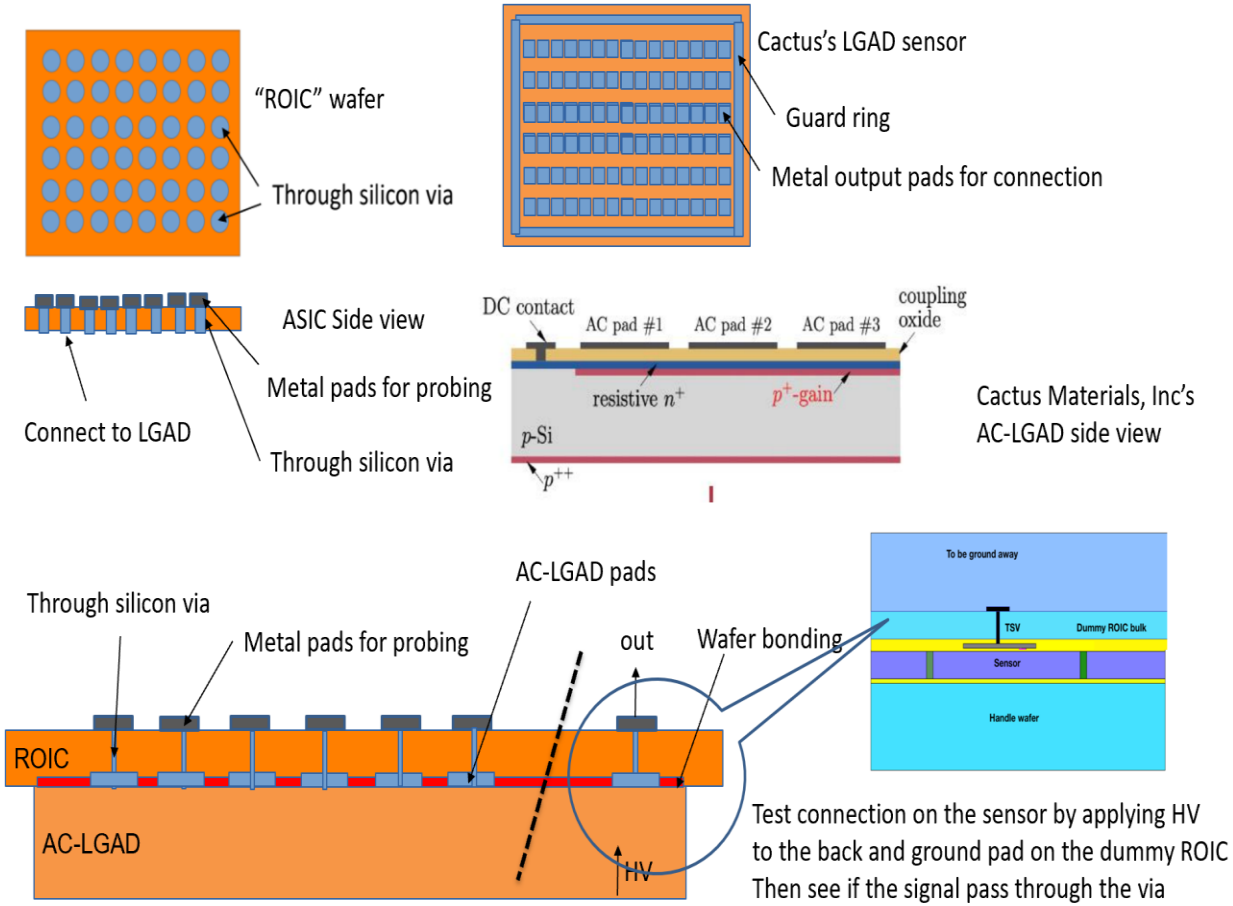






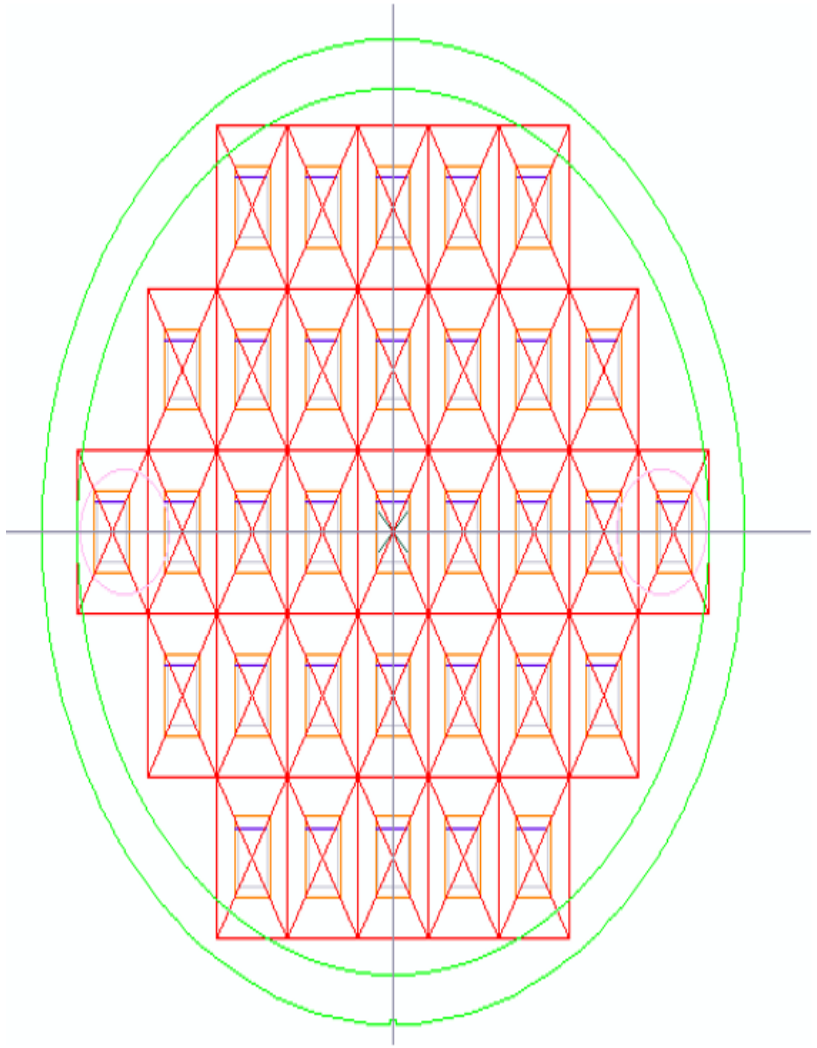
3D integration Schematic

- W2W/C2W bonding of ROIC Chip to sensor wafers
- Electrical yield and reliability
- Near-cryogenic testing of 3D integrated bonded sensors to ROIC substrates
- Fine pitch (<4 um) 3D integration; Phase I design ~10 um pitch

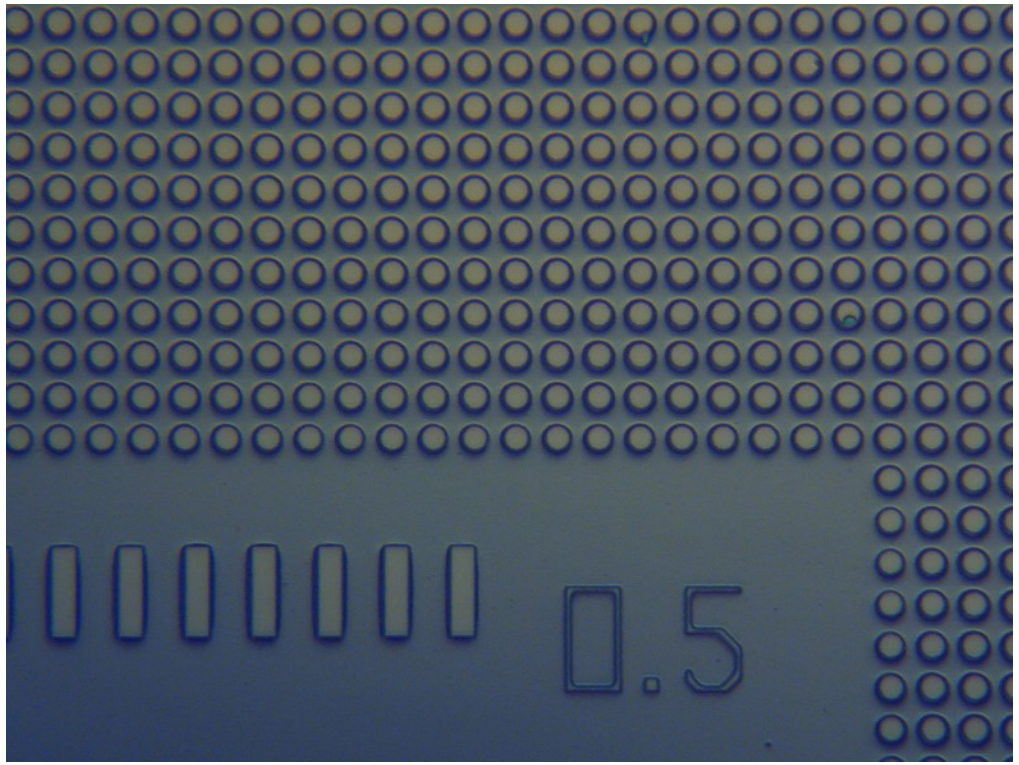


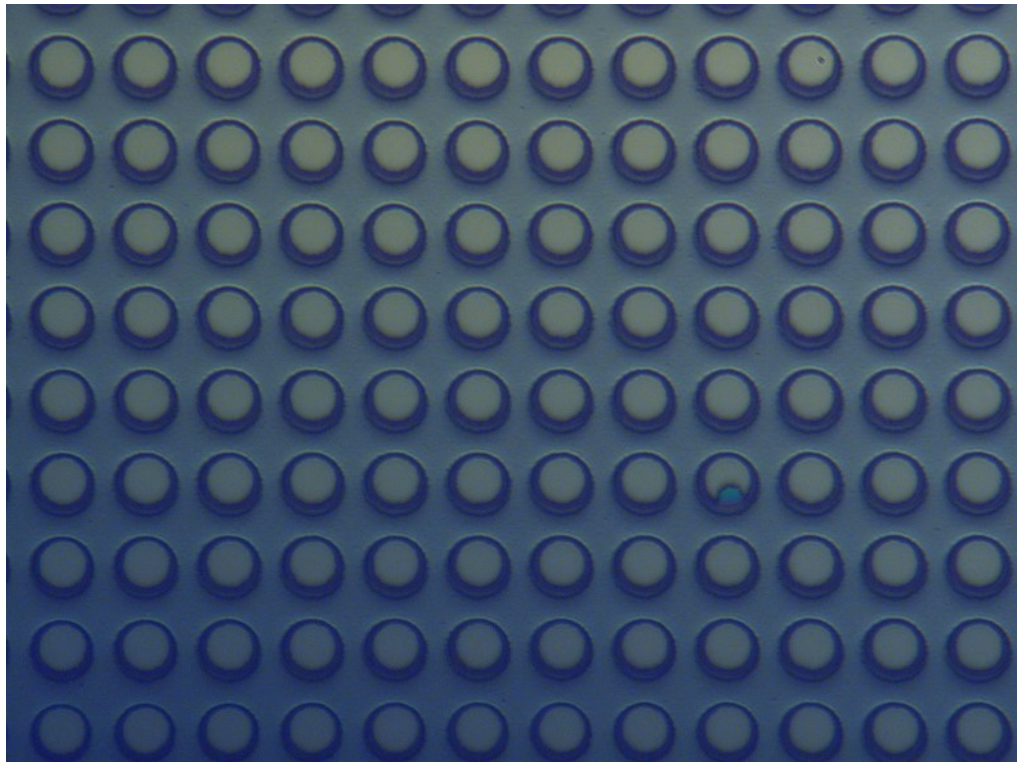
Design – Daisy chain design (confidential)

- 33 Die Array.
- Die Size: 10x16.5 mm.
- Step/Repeat: 20x, 33y mm.
- Die intersects at 0,0 on wafer.
- 5 litho masks, 60+ process steps
  - Key steps: Blue colored steps are completed.
    - Oxide PECVD
    - Mask set 1 lithography (for Key)
    - Oxide Dry etch (RIE)
    -
    - 2nd mask set of post layers
    - DRIE for TSV formation
    - Barrier layer -> Metal deposition (i.e. sputtering), Ti and Cu.
    - Plating – Outside service
    - Etching Ti and Cu wet process
    - Oxide passivation
    - CMP
    - Bonding
    - Patterning saw lane mask for electrical testing



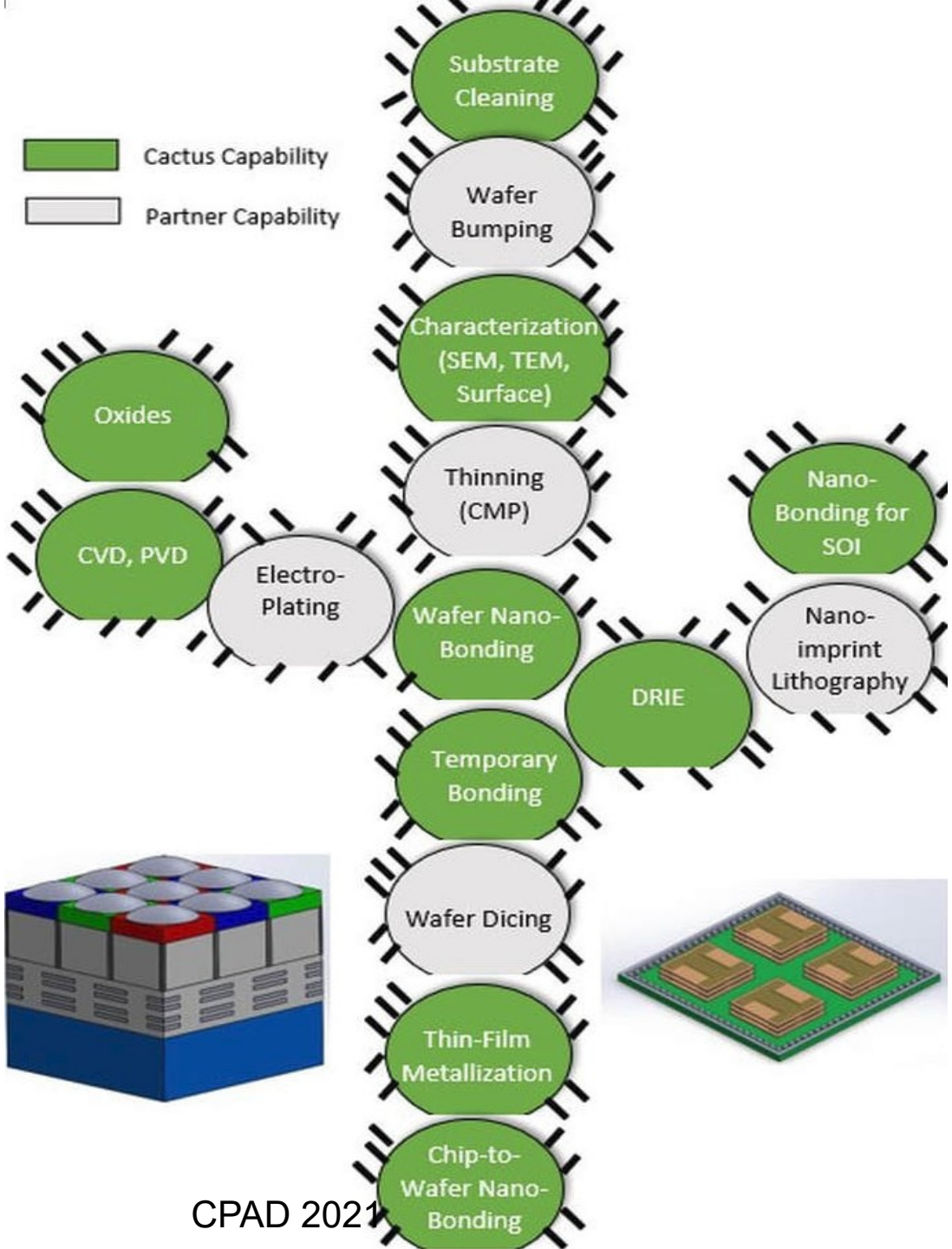
Si Plated Post for DRIE TSV for 3D Integration



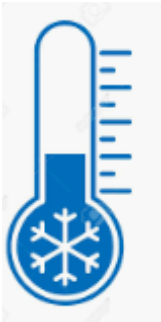


Post (um): 4.99

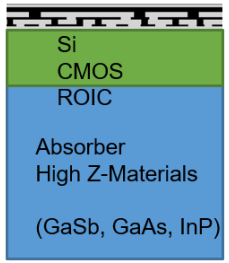
Core Capabilities
(Foundry Service)



Value Proposition



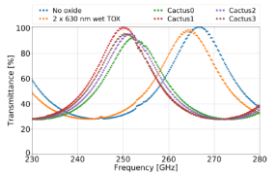
- ✓ Room temperature bonding
- ✓ Hybrid bonding (w or w/o TSV)
- ✓ annealed < 250^0C (Si, III-V, $LiNbO_3$)



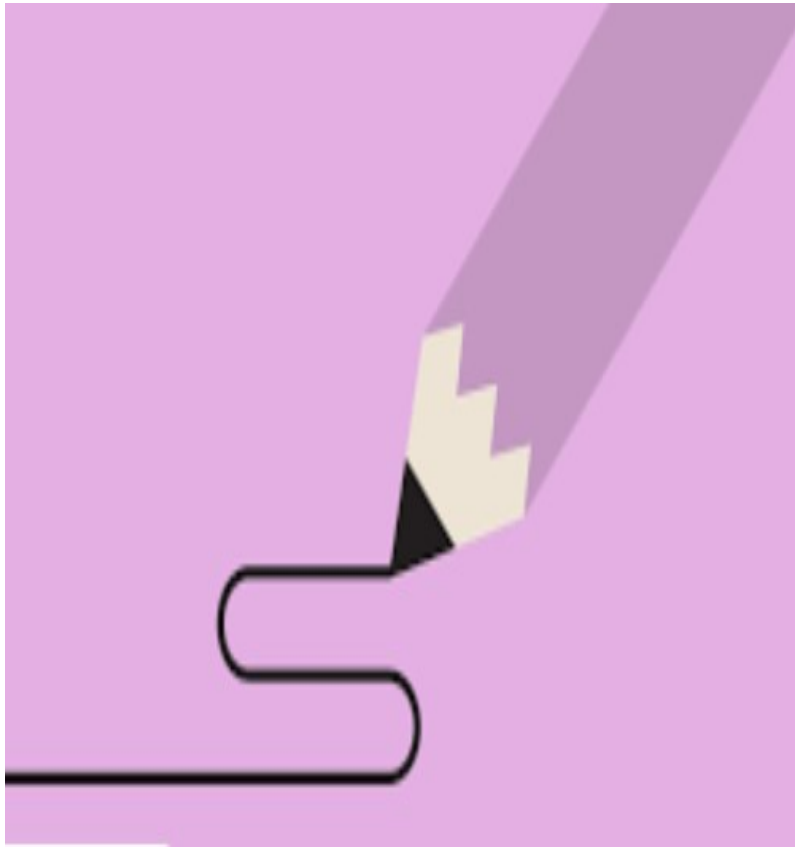
- ✓ SiSi Wafer with high charge collection

Readout Chip CMOS

Absorber High-Z Material or Si



- ✓ Oxide bonded interface with <u>no or low</u> optical absorption
- ✓ Add on to existing bonding equipment

Conclusions

- DJ-LGAD is an enabling technology for high granularity detectors.
- Cactus's materials's wafer bonding capability can be extended to other absorber High-Z materials (III-V materials; GaSb, GaAs, InP)
- 3D integration through wafer bonding is an enabling techniques for many applications, high density integration of ROIC CMOS to sensors, high density high frequency RF IC device packaging, and others.