Trigger and Data Acquisition for the Mu2e-II experiment

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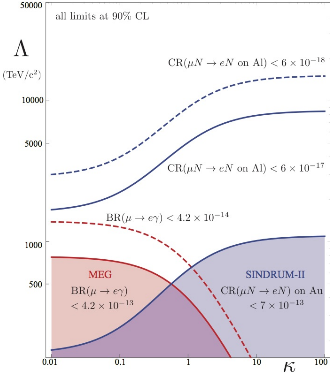
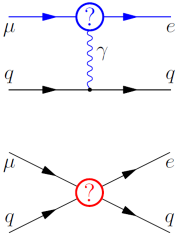
Mu2e-II Physics Motivation

Aims to improve sensitivity to charged-lepton flavor violating (CLFV) neutrino-less conversion of a nuclear bound muon into an electron by an order of magnitude over Mu2e

Derived from A. de Gouvea, P. Vogl, Prog. Part. Nucl. Phys. 71 (2013) 75





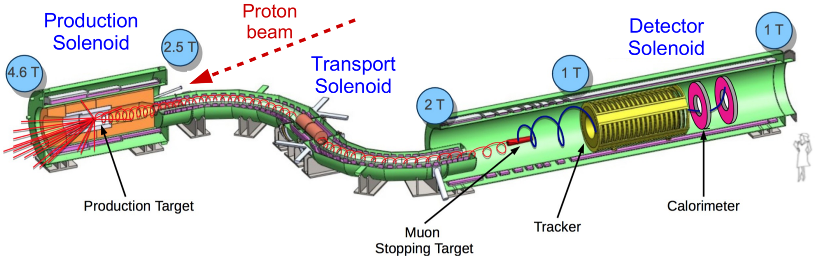
- No observation in Mu2e: extend search to higher mass scale
- Observation in Mu2e: precision measurement, explore models with different targets

Interest in Mu2e-II

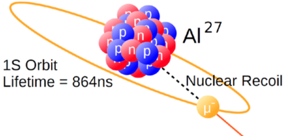
https://mu2eiiwiki.fnal.gov/wiki/Mu2e-II

- Expression of interest: arXiv:1802.02599
  - 130 signatories, 36 institutions, 6 countries
- 11 SNOWMASS LOIs
  - Several working groups performing studies that will lead to future white papers

Mu2e / Mu2e-II general design

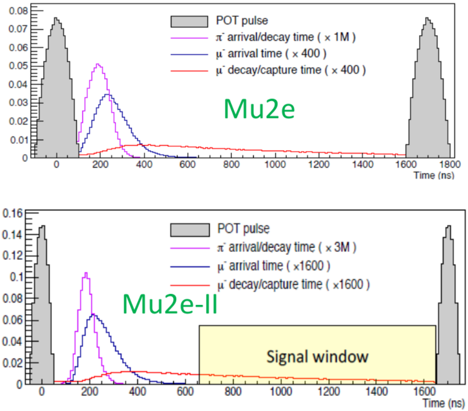


- Muons stop on stopping target, muonic decay or convert
- CLFV signal is 105 MeV electrons
- Main detectors are tracker, calorimeter, plus cosmic ray veto



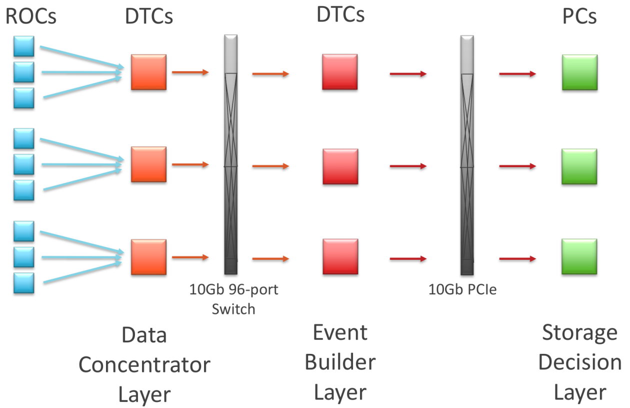
$$E_e = m_\mu c^2 - (B.E.)_{1S} - E_{recoil} = 104.96\,\mathrm{MeV}$$

Mu2e-II upgrade overview



- Take advantage of the PIP-II beam upgrade
  - Higher intensity and duty factor to get 10x more muons
  - Narrower pulses, less pulse to pulse variation
- Detectors and TDAQ upgraded to handle higher rate
- Timescale: Start around 2030 with 3 years of data taking

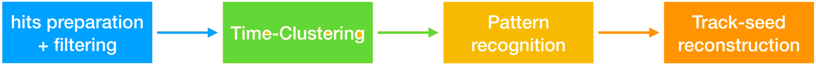
Mu2e-I Readout and trigger scheme

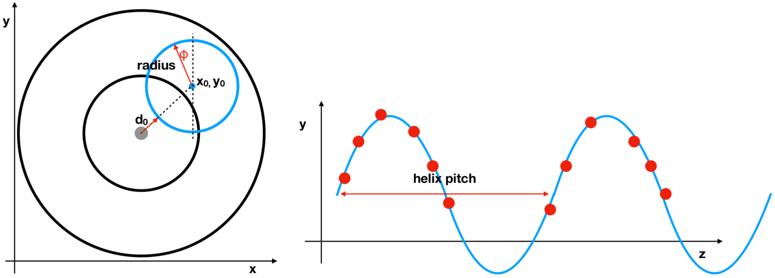


- Large front end buffers to average over long offspill time
- $\sim$40 GB/s data read out to storage decision layer, $\sim$280 MB/s written to disk
- 69 DTCs (Kintex-7) for data readout and event building
- 800 threads on 40 nodes for HLT $\rightarrow$ $\sim$5 ms per event

Mu2e-I Readout and trigger scheme

Software high level trigger design:





- Can be constrained with calorimeter information
- Filtering between each stage
- Final stage is χ^2 helix fit

Mu2e-II TDAQ requirements

- Beam dutyfactor increases by ∼4x
  - Mu2e uses 25%, large off spill components of every 1.4 s beam spill
  - With PIP-II, DUNE will only use 1.1%, allows Mu2e-II to have ∼97% dutyfactor
- Instantaneous proton rates ∼3x higher than Mu2e
- Assume 2x more detector channels

Mu2e-II TDAQ requirements

- Total data rate ∼20x higher
  40GBps → 800 GBps from front end
  200 KB → 1 MB event size (@600 KHz)
- Mu2e has 7 PB/year tape capacity, assume 2x for Mu2e-II
  → Storage level decision trigger rejection >3000x
- With near 100% beam dutyfactor large front end buffers no longer useful
  - May need low latency trigger

Radiation concerns

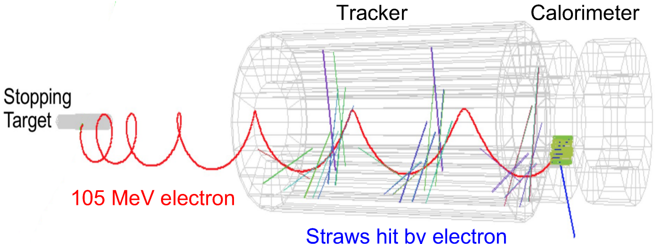
- Radiation levels at the front end will also be $\sim$10x that in Mu2e
- Mu2e ROCs use Microsemi Polarfire FPGAs
  - Configuration memory immune to SEU effects
  - Tested up to 2e12 n/cm^2
  - may be sufficient for Mu2e-II as well
- Mu2e also uses rad-hard VTRx transceivers (374$\times$ 0.6 GBps $=$ 224 GBps), will need more / higher speed links
  - Again hope to use LHC technology

Overview of SNOWMASS LOIs: options being explored

- Option 1: A trigger-less TDAQ system based on software trigger
- Option 2: TDAQ based on GPU co-processor
- Option 3: A 2-level TDAQ system based on FPGA pre-filtering
- Option 4: A 2-level TDAQ system based on FPGA pre-processing and trigger primitives

Option 1: A trigger-less TDAQ system based on software trigger (Scale up current Mu2e approach)

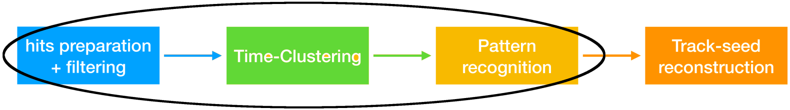
- Requires 10x more hardware than Mu2e, even assuming 2x performance improvement
- Non-linearity of combinatorics may mean this is an underestimate
- Could use calorimeter for initial time pre-filtering
- Could use partial event building
  - Mu2e tracks make multiple loops
  - May be possible to segment tracker, trigger on reconstruction of only smaller part, greatly reducing combinatorics



Option 2: TDAQ based on GPU co-processor

- Reduce hardware requirements for HLT by parallelizing work on GPUs
- Can we parallelize Kalman Filter helix fit?
- Use GPU co-processor as a service?
  (M. Wang et al., arXiv:2009.04509)

Option 3: A 2-level TDAQ system based on FPGA pre-filtering



- L1 hardware trigger implemented on FPGAs
- Utilize HLS
  - First stages of Mu2e trigger require MVAs, histograms
- Events that pass L1 move on to software HLT
- Requires concentrating event data onto one board

Option 4: A 2-level TDAQ system based on FPGA pre-processing and trigger primitives

- Front end FPGAs build trigger primitives (e.g. track stubs) and have short buffer for full event data
- Design new L1 trigger algorithms running on these primitives, greatly reducing amount of data required to be concentrated on L1 FPGA boards
  - Possible to change readout configuration at front end to better allow local reconstruction
  - Still exploring upgraded tracker design
- Full data stream send directly from front end to HLT layer

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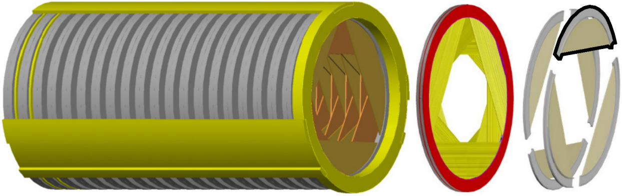
- Fu



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Conclusion

- Mu2e-II will increase sensitivity to muon conversion by an order of magnitude over Mu2e
  - Extend mass scale reach or
  - Help discriminate between new physics models
- Expect 20x data rate, 10x radiation dose
- Several options for increasing speed of software high level trigger or implementing hardware L1 trigger
  - We have just begun exploring these options
- Possibility of running prototype of any L1 trigger during Mu2e second phase
- Comments welcome!

Backup

Example trigger primitive building: Tiny Triplet Finder

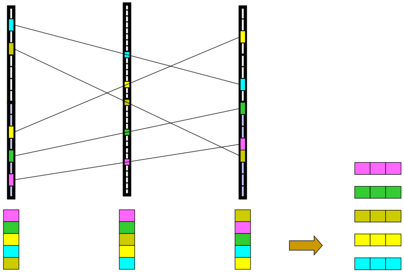
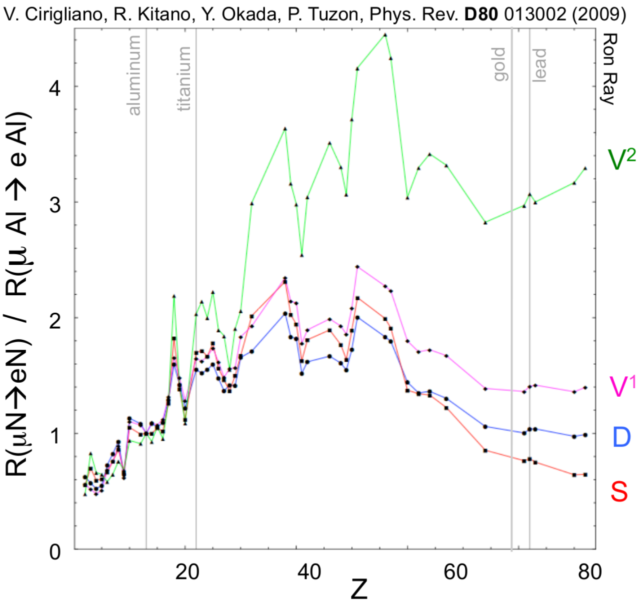


Figure from Jinyuan Wu

- Example: hit triplets from Tiny Triplet Finder (J. Wu, et al., FERMILAB-CONF-04-270-E)
  - Finds and reorganizes hits by track segment coincidences
  - Fast / efficient resource usage using bit shifters + bitwise logic units
  - Can handle about 20 hits per layer every 100 ns
- Works for curved tracks and different detector geometries

Mu2e-II Physics Motivation

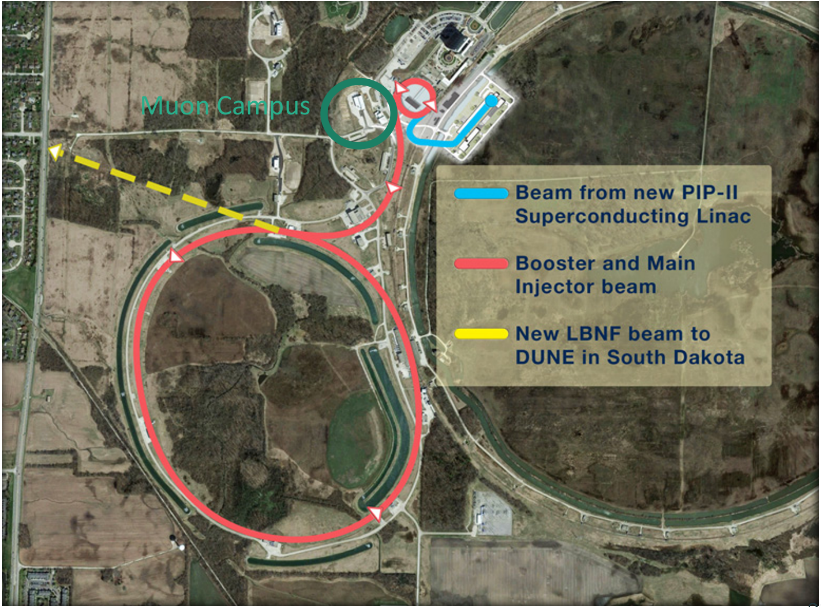


FPGA scaling

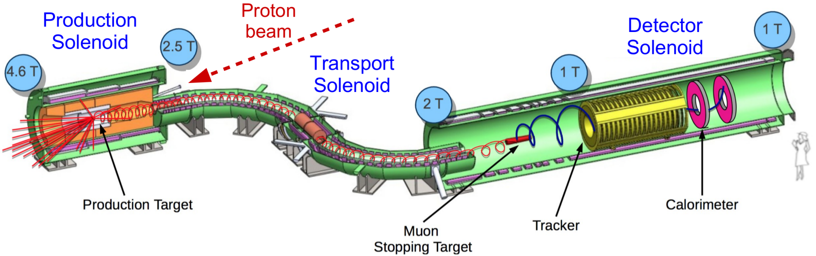
Mu2e-I DTC → KINTEX 7

	KINTEX 7	KINTEX UltraSCALE	VIRTEX 7	VIRTEX UltraSCALE
Logic Cells (LC)	478	1,161	1,995	4,407
Block RAM (BRAM) (Mbits)	34	76	68	132
DSP-48	1,920	5,520	3,600	2,880
Peak DSP Performance (GMACs)	2,845	8,180	5,335	4,268
Transceiver Count	32	64	96	104
Peak Transceiver Line Rate (Gb/s)	12.5	16.3	28.05	30.5
Peak Transceiver Bandwidth (Gb/s)	800	2,086	2,784	5,886
PCI Express Blocks	1	6	4	6
Memory Interface Performance (Mb/s)	1,866	2,400	1,866	2,400
I/O Pins	500	832	1,200	1,456

PIP-II


Muon Campus
Beam from new PIP-II Superconducting Linac
Booster and Main Injector beam
New LBNF beam to DUNE in South Dakota

Mu2e / Mu2e-II general design



- Production solenoid
  - Proton beam hits production target
  - Magnetic mirror directs low momentum pions/muons to transport solenoid
- Transport solenoid
  - S-shape sign and momentum selects
- Detector solenoid
  - Muons stop on stopping target, muonic decay or convert
  - Look for 105 MeV electrons