Characterization of ITkPix-V1 pixel readout chip

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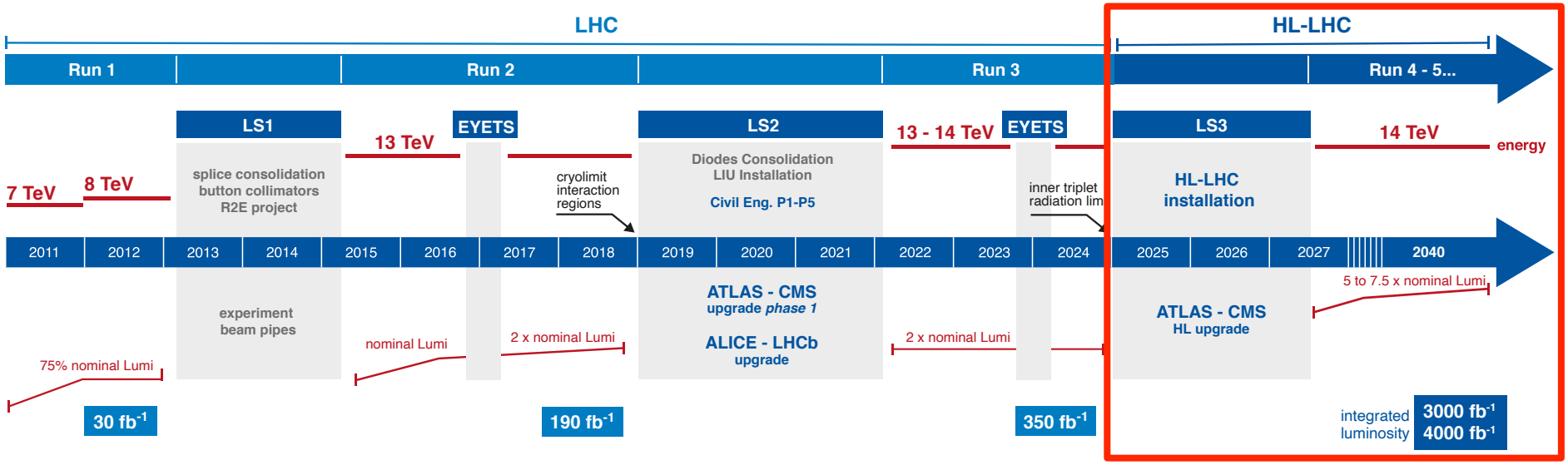
on behalf of ITkPix-V1 testing team

CPAD Instrumentation Frontier Workshop

March 18, 2021

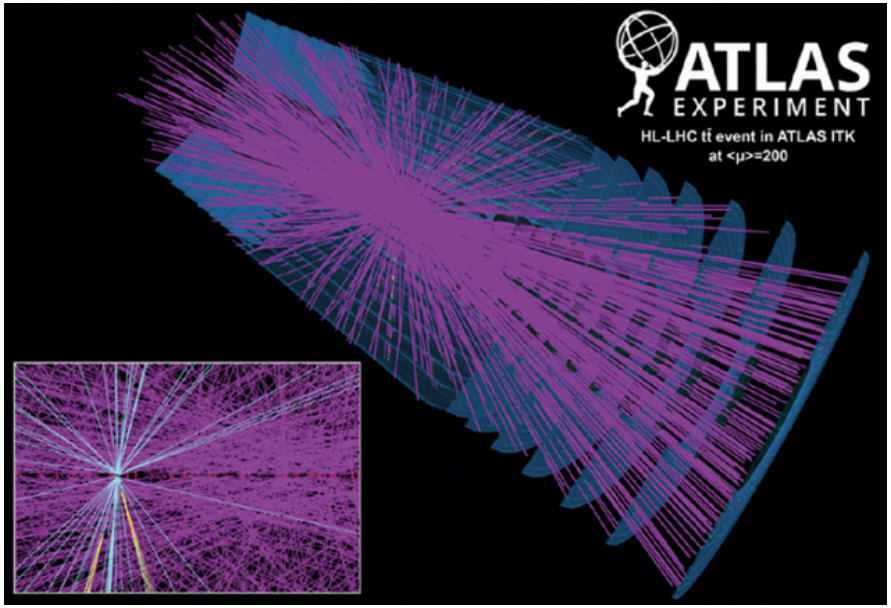
Introduction

- Pixel detector is at the center of ATLAS, surrounding the beam pipe. It is essential for vertex reconstruction and tracking
- At High-Luminosity LHC (HL-LHC), Pixel detector will be upgraded to cope with **extreme data rate and irradiation**
  - One of the greatest challenges is to design a readout front-end chip that meets the requirements



Operating conditions

- HL-LHC will operate with instantaneous luminosity up to **7.5×10^{34} cm^{-2}s^{-1}** (~**200** interactions per bunch crossing). Aiming to deliver up to **4000 fb^{-1}** *pp* collision data
- In the meanwhile, upgraded pixel detector is expected to deliver no worse performance compared with current one



Requirements

- Reduced pixel size
- Analog FE operates at lower threshold and has lower power consumption
- Highly compressed data stream
- Large enough output bandwidth
- Larger module size; serial powering
- Radiation hard

ITkPix-V1 pixel readout chip

- ITkPix-V1 is designed by RD53 collaboration for the **ATLAS Phase 2 Inner Tracker (ITk) Pixel detector** operating at **HL-LHC**
  - Based on **65 nm** technology
  - Significant improvements compared with FE-I4 used on current ATLAS Insertable B-Layer
- Characterizing ITkPix-V1 chip performance is crucial for ATLAS Phase 2 ITk Pixel upgrade

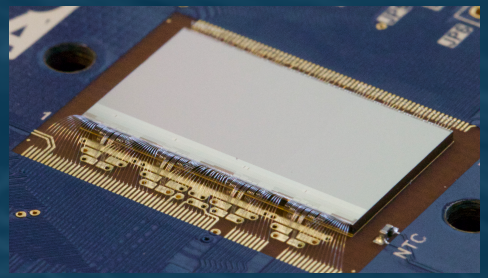
RD53 Collaboration:
22 collaborating institutes

Readout chip	Chip size	Pixel size	Pixel hit rate	Trigger rate
ITkPix-V1	2×2 cm^2	50×50 μm^2	3 GHz/cm^2	4/1 MHz
FE-I4	2×2 cm^2	50×250 μm^2	400 MHz/cm^2	100 kHz
Readout chip	**Trigger latency**	**Current consumption**	**Radiation tolerance**	**Min. stable threshold**
ITkPix-V1	12.8/51.2 μs	< 8 μA/pixel	0.5 Grad	600 e
FE-I4	6.4 μs	20 μA/pixel	300 Mrad	1500 e

ITkPix-V1 vs. FE-I4 specifics

Timeline

RD53A (400x192)



RD53 Collaboration LOI

02/2013

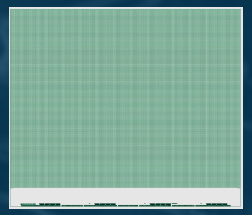
RD53A chip submission

11/2017

RD53B design finished

11/2019

CROC submission

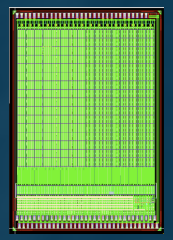


CROC (432x336)

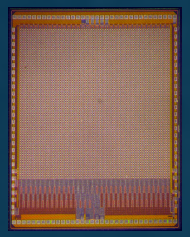
We are here

12/2015

FE65-P2 and CHIPIX prototype chips



CHIPIX (64x64)



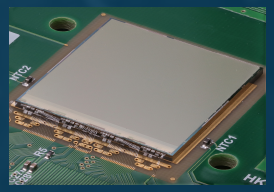
FE65-P2 (64x64)

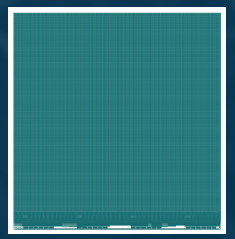
12/2018

RD53A AFE review & design validation finished

03/2020

ITkPixV1 submission





ITkPixV1 (400x384)

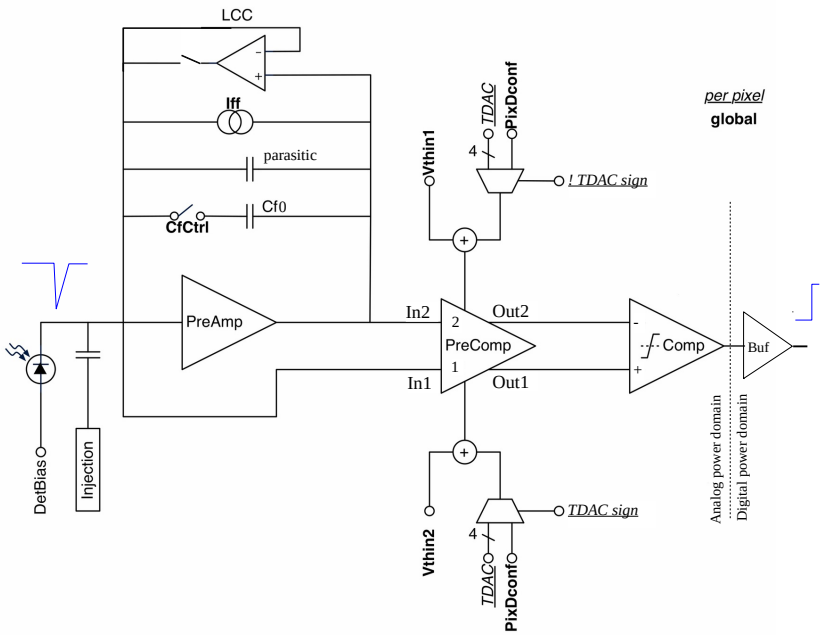
*10/2020

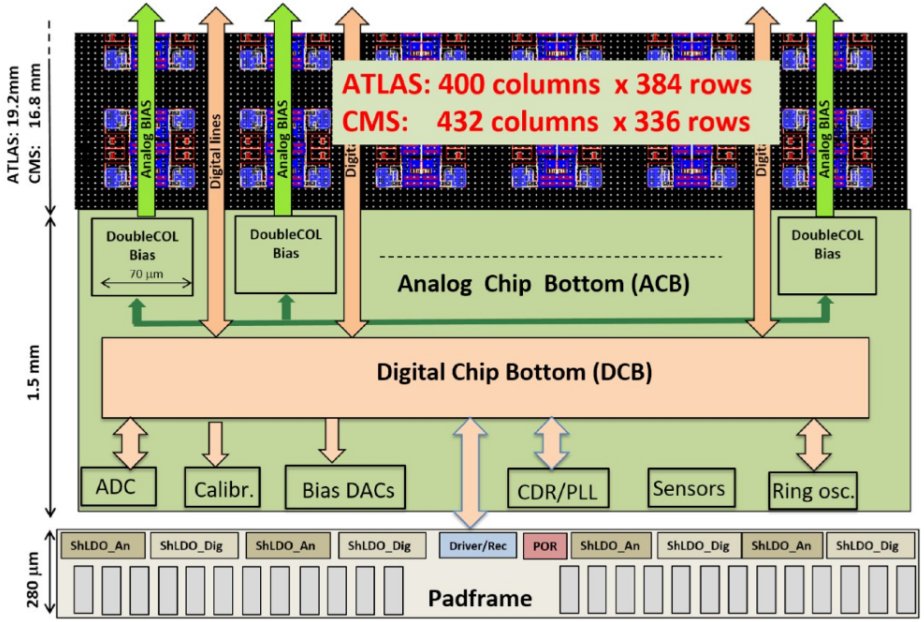
ITkPixV1.1 submission with patch for ToT memory issue in V1

ITkPixV2 submission

Courtesy of Timon Heim

ITkPix-V1 overview

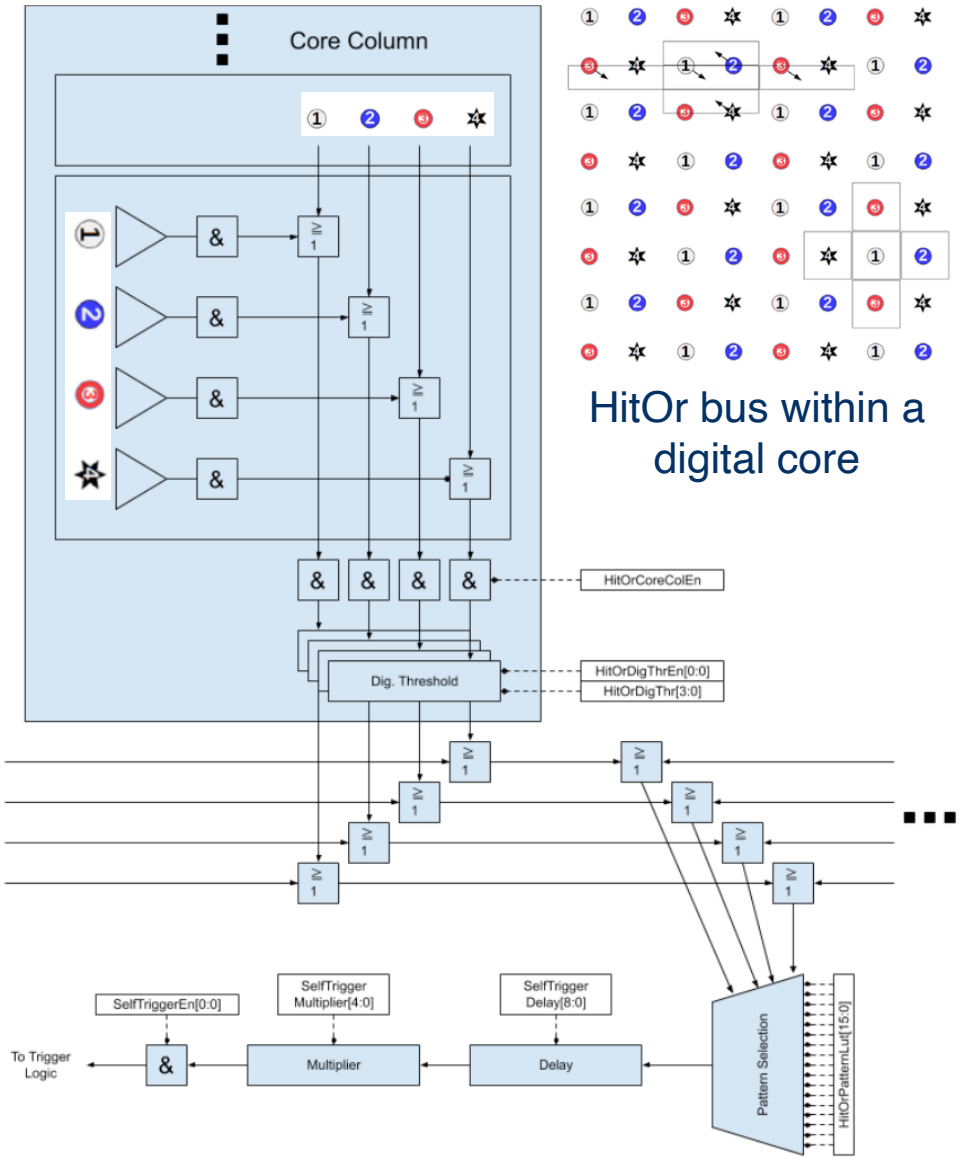




- **Novel differential analog FE** featuring low noise and fast time-walk, optimized for minimal power
- Analog islands embedded in flat digital synthesized sea
- In total 400×384 = 153600 pixels, organized in 2400 **8×8 digital cores**
- Multiple blocks integrated in chip bottom

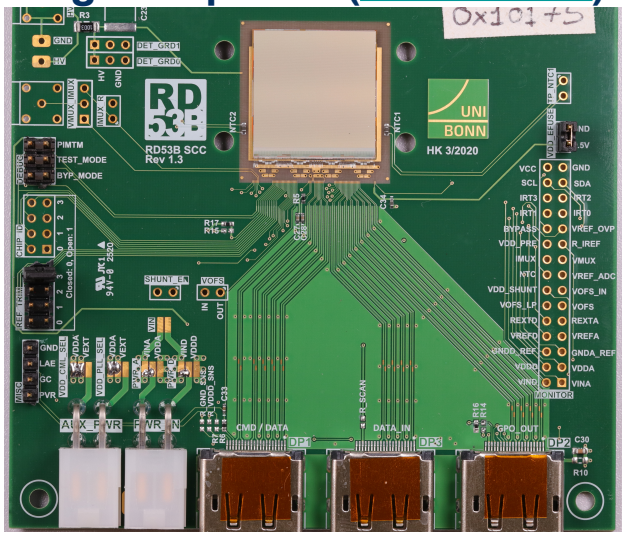
HitOR bus, self-trigger, and precision ToT

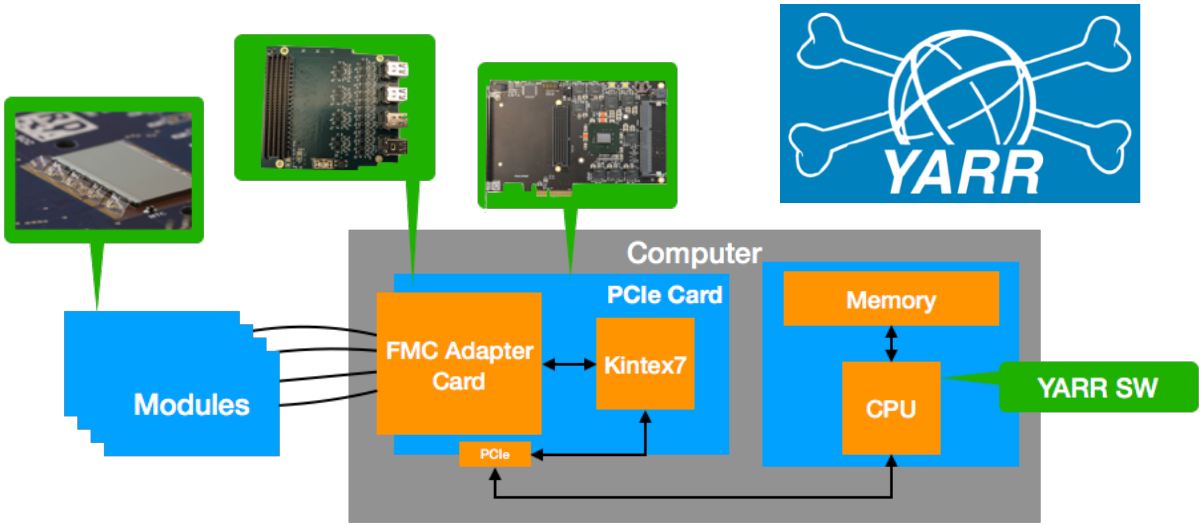
- There are **four HitOR nets** serial-chaining all pixels in each core column (8-pixel wide)
- HitOR signal is used to
  - Generate self-trigger: mainly used for source scans
  - Provide **precision time-over-threshold/time-of-arrival** (ToT/TOA) counted in **640 MHz** clock: **new feature!**
    - Extremely useful for calibration and diagnostics
    - Too slow for data-taking at (HL-)LHC with 40 MHz bunch crossing frequency



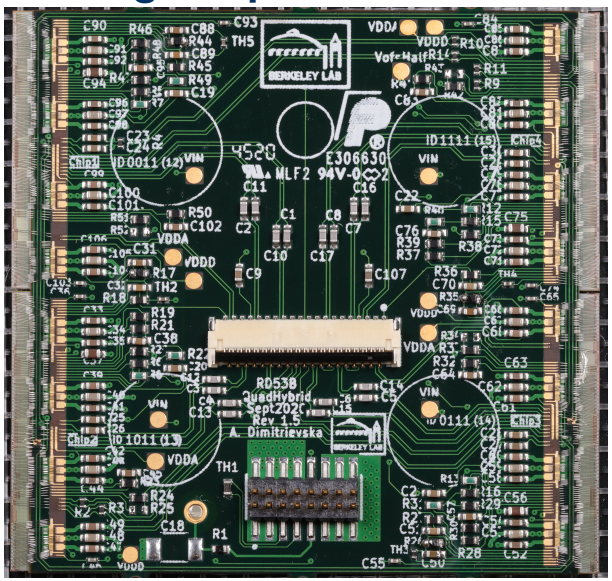
Test system

Single chip card (schematics)





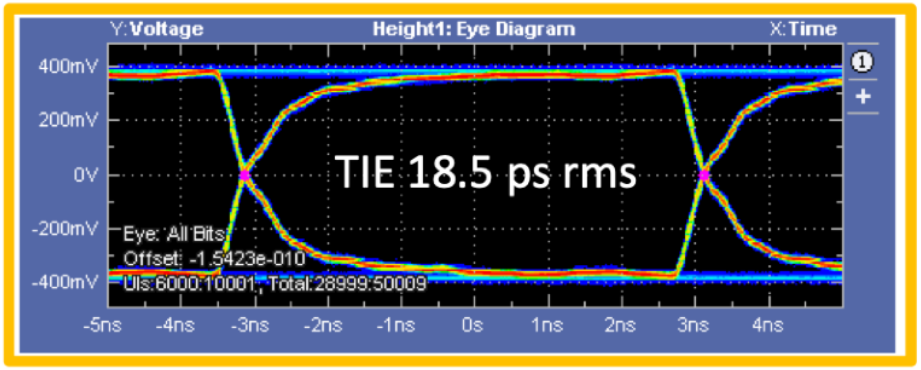
Digital quad module

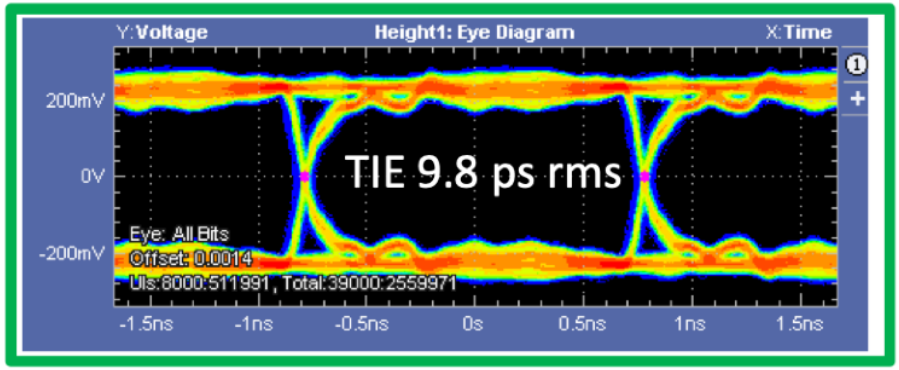


- ITkPix-V1 mounted on single chip card for testing
  - Chips will eventually be bump-bounded to sensor and assembled into modules (e.g. 4-chip quad module)
- Readout using YARR system (https://yarr.web.cern.ch/yarr/)
  - Commercial PCIe FPGA board with custom FMC adapter card
  - PCIe communication to PC
  - Hardware agnostic SW based on C++, aiming at growing from chip characterization all the way to detector operation
- Tests can also be performed with BDAQ53 system

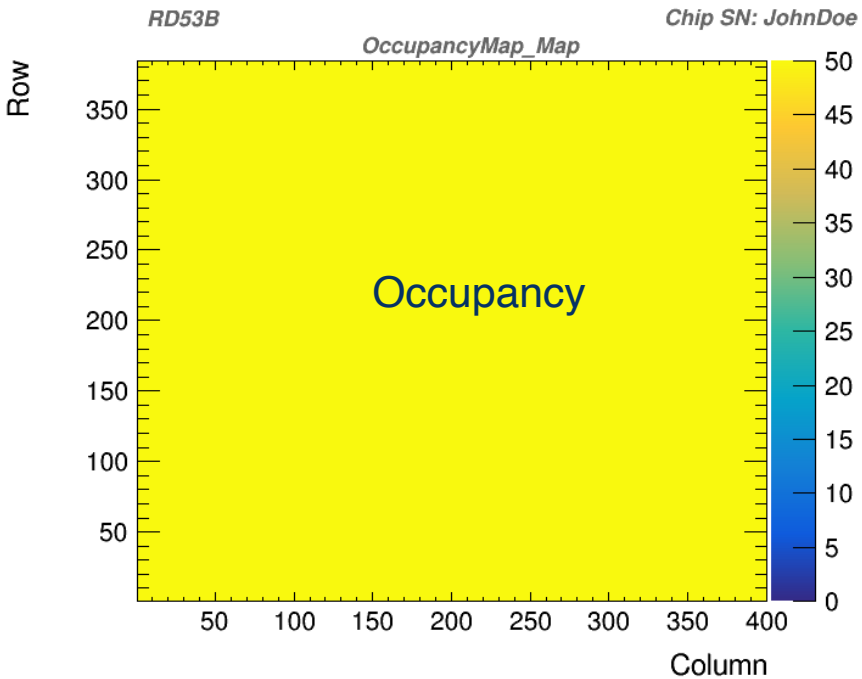
ITkPix-V1 validation

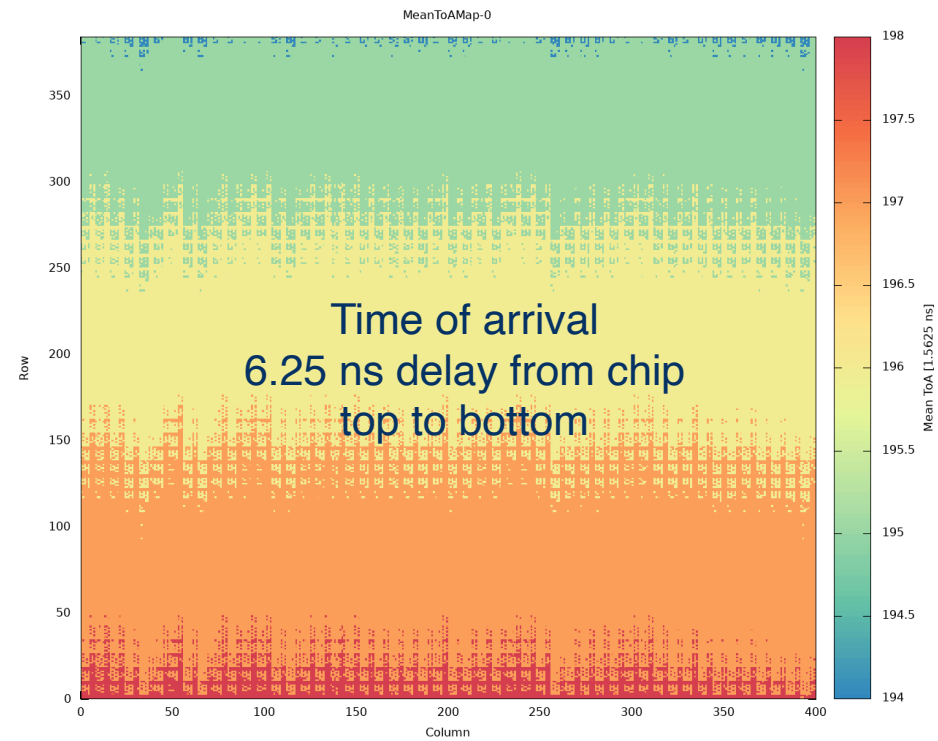
- **Most ITkPix-V1 functionalities are working as expected**
- In particular, the CDR circuit is performing within requirements
  - 160 MHz clock recovered from custom DC balanced CMD protocol. 40 MHz bunch crossing clock derived via special sync frames
  - Internal PLL multiplies 16 MHz up to 1.28 GHz clock, which is used to drive four 1.28 Gbps data output
    - **Small jitter**: significant improvement compared with RD53A
    - Important for long distance (>6 m) data transmission





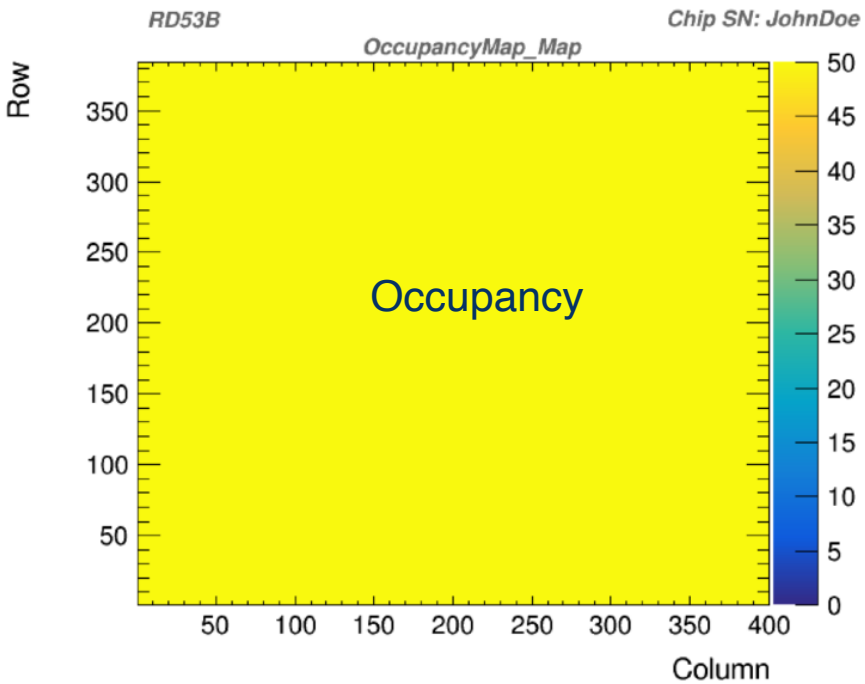
Digital tests

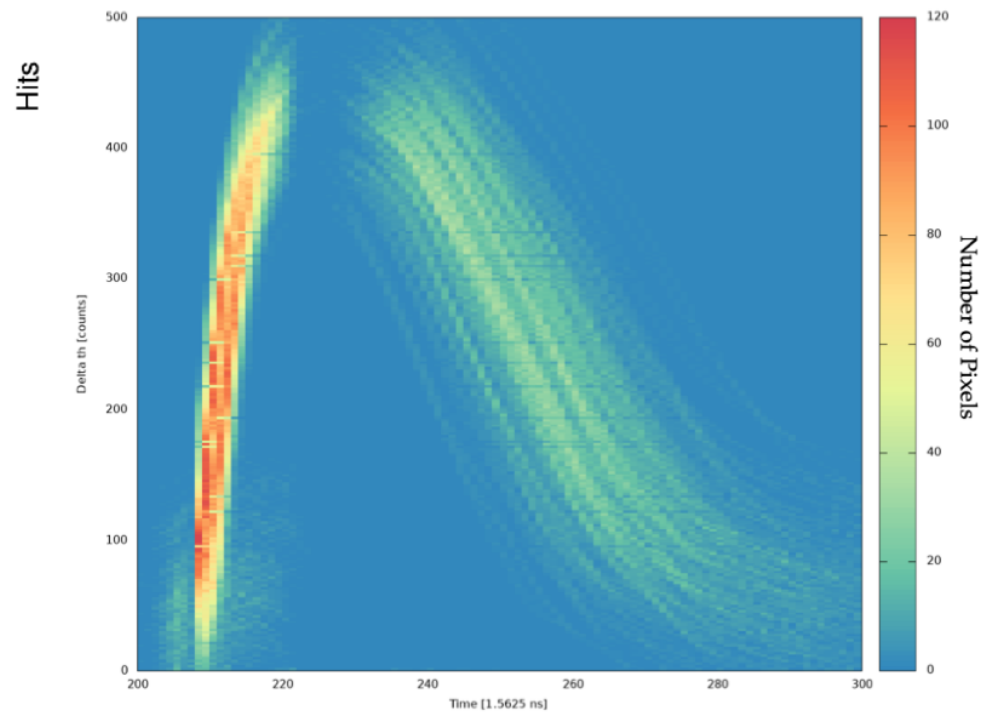


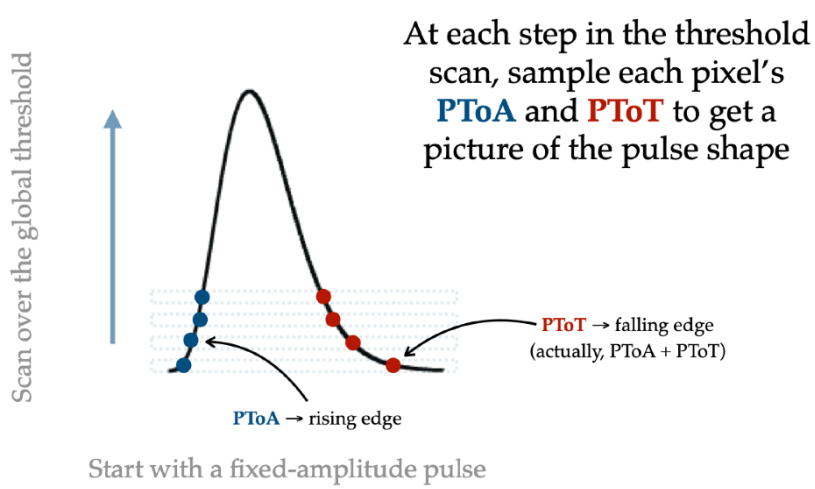


- **Digital circuity respond properly to digital signal injections**
- Signal ToA in ns precision obtained from precision ToT data
- Besides using trigger command, digital scan can also be performed with self-trigger generated from HitOr bus signal

Analog test

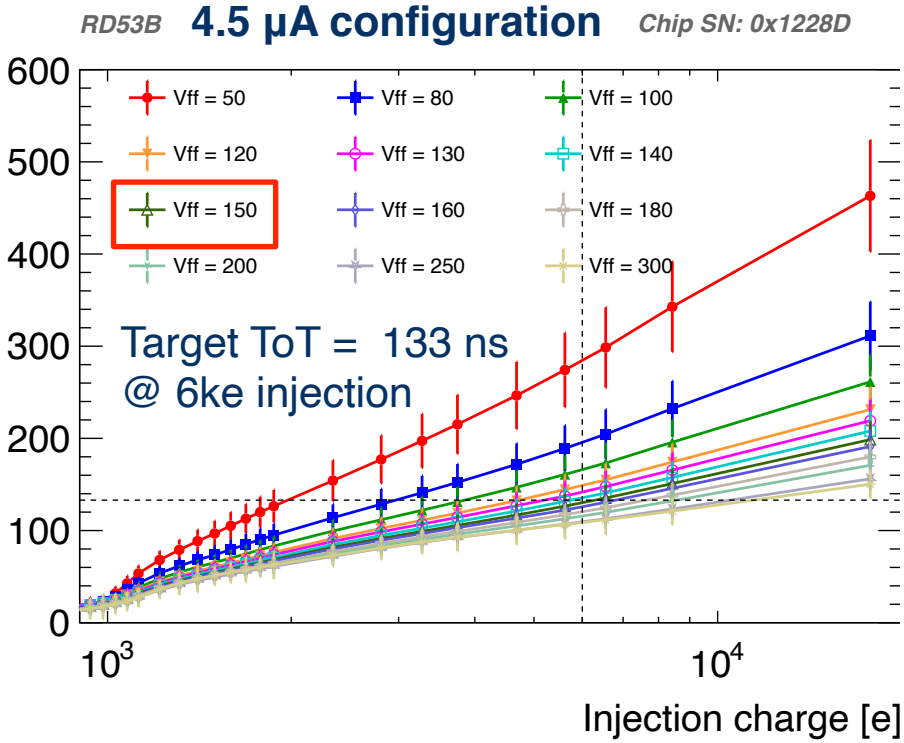


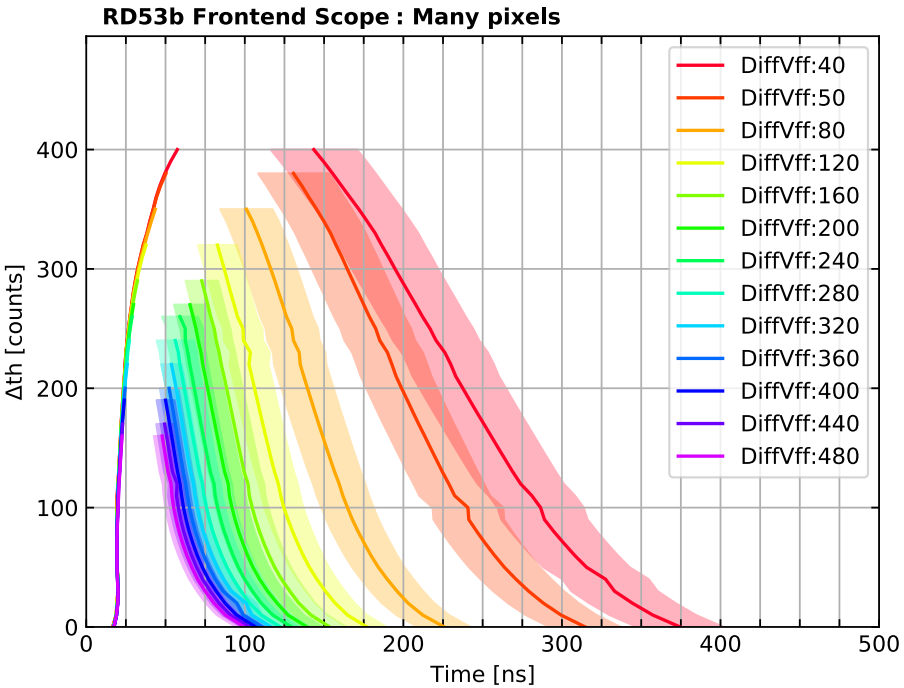




- Analog injection shows good results
- From scanning threshold, can use precision ToT and ToA to get the signal profile from analog injection!

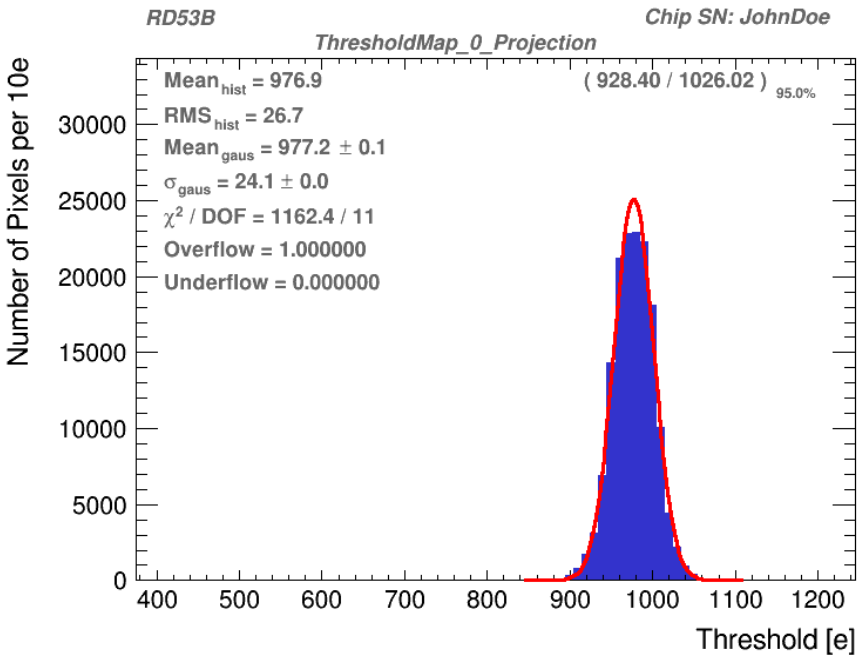
Tuning ToT

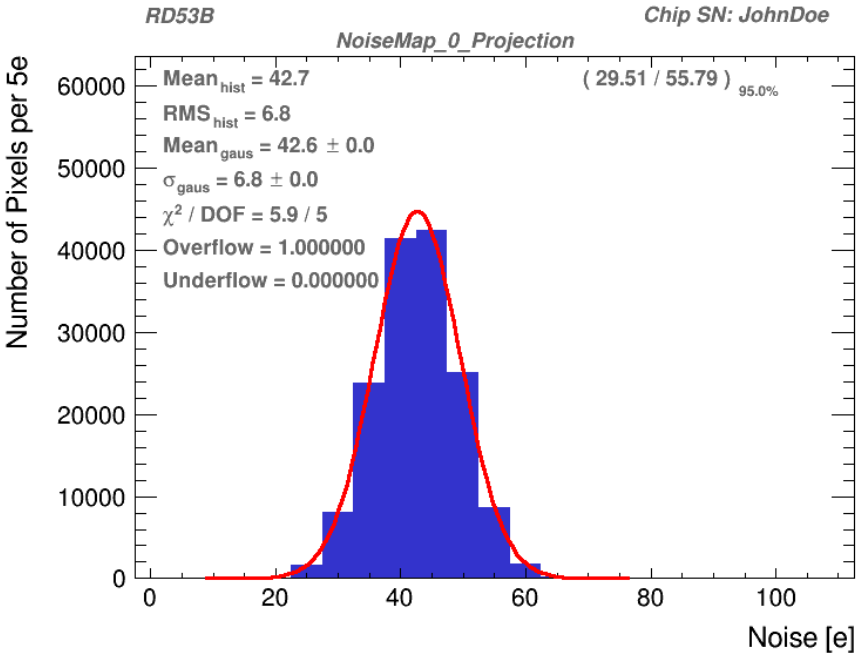




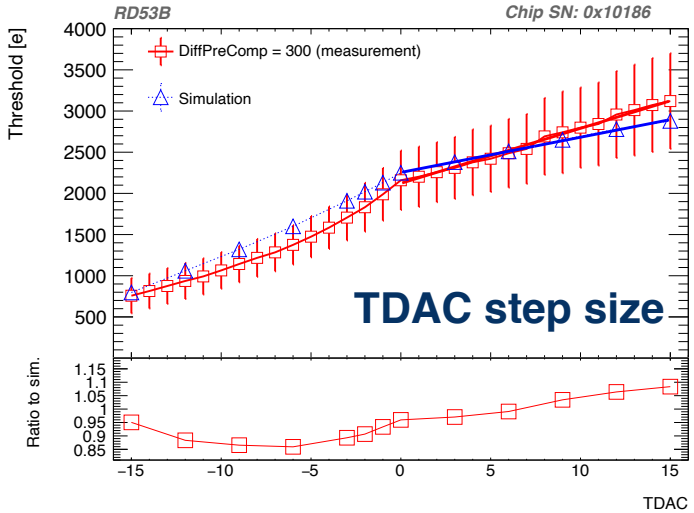
- ToT in ITkPix-V1 is controlled by the preamplifier bias and the feedback current global DACs
- Recommended DAC values available for different configurations to be used on inner/outer layers of ITk Pixel detector
  - Derived from measurement on bare chip; to be revisited with sensor attached

Threshold tuning

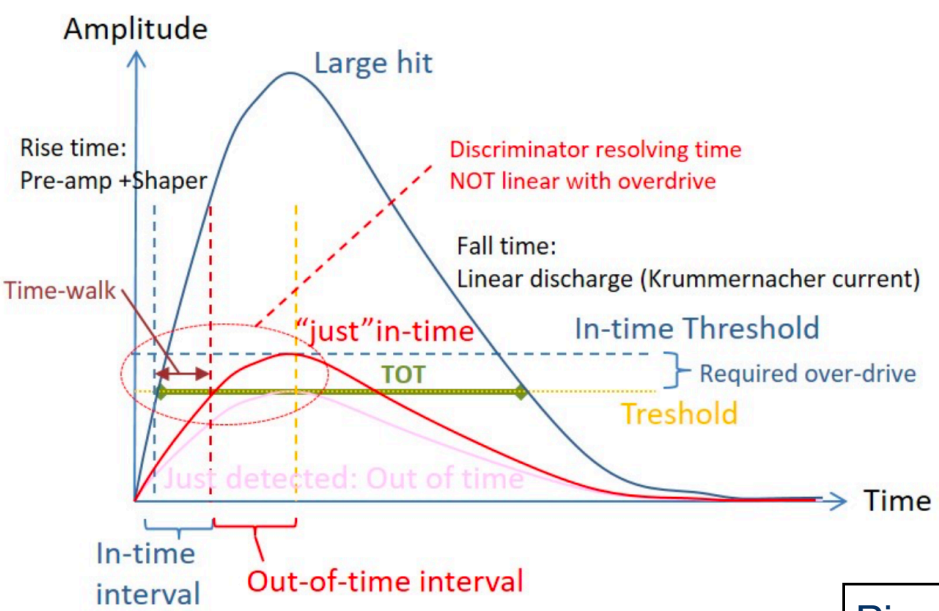


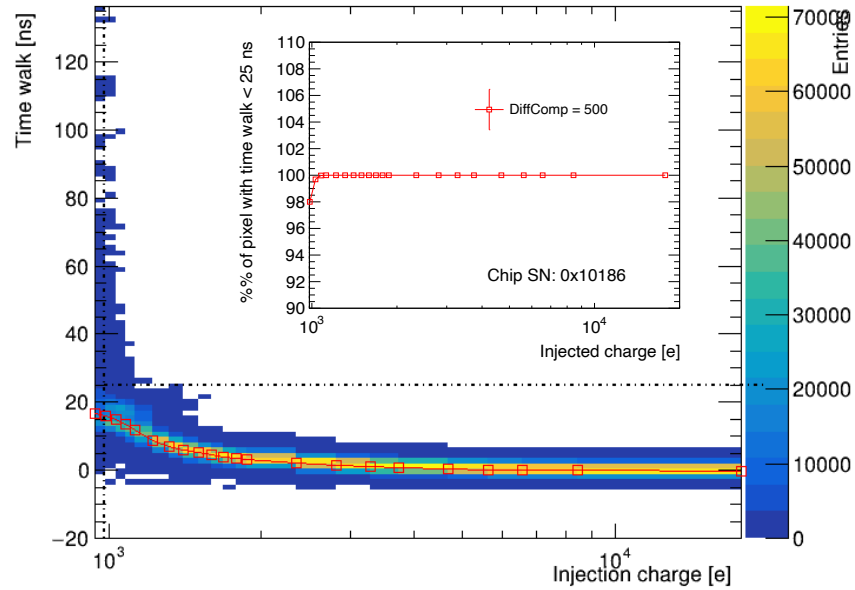


- Can reach **~25e** dispersion at 1000e threshold dispersion after tuning
- **Very low noise: ~45e**
  - This is from bare chip without sensor capacitance. Noise will slightly increase with sensor attached



Time-walk measurement

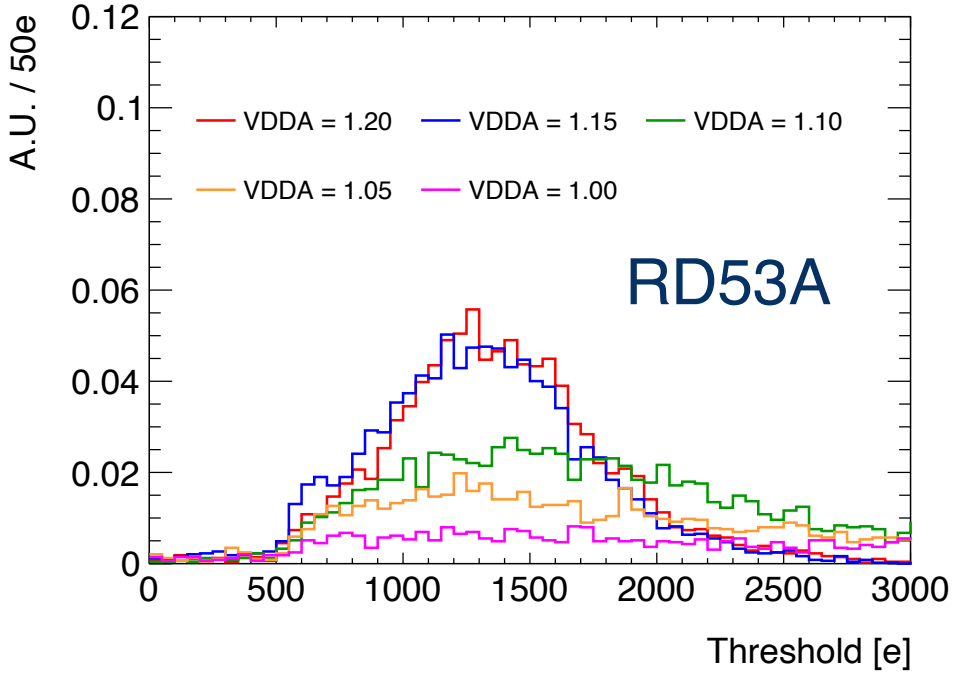


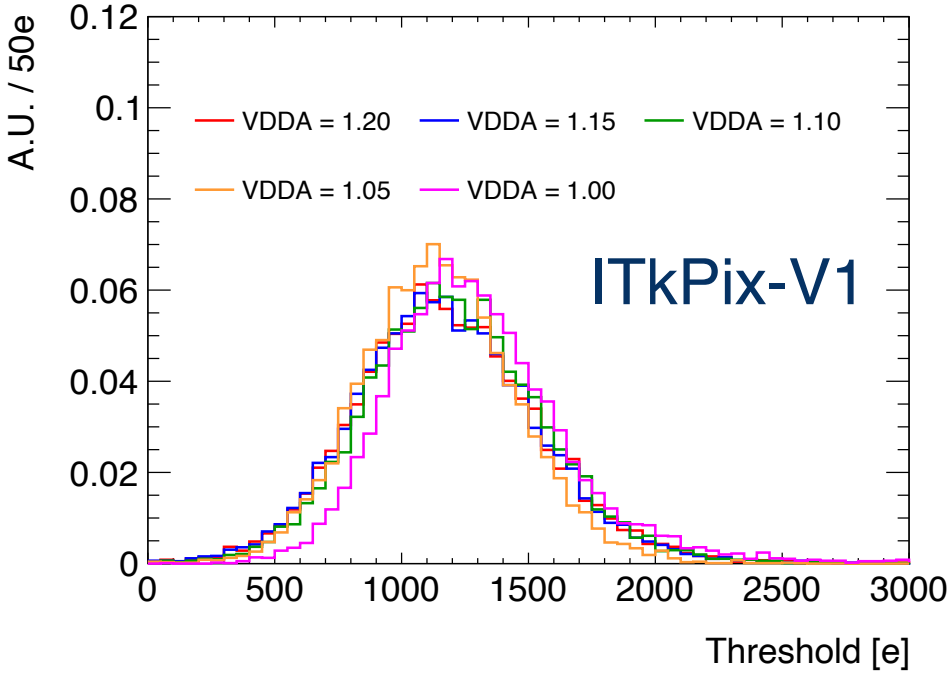


Pixel threshold tuned to 1000e, no sensor capacitance

- Time-walk: ToA difference between a small and a very large injection
  - LHC bunch crossing frequency is 40 MHz, so we have **25 ns** before the signal gets a wrong bunch crossing stamp
- **Differential analog FE time-walk is well below 25 ns** (to be revisited with sensor attached)

ITkPix-V1 vs. RD53A



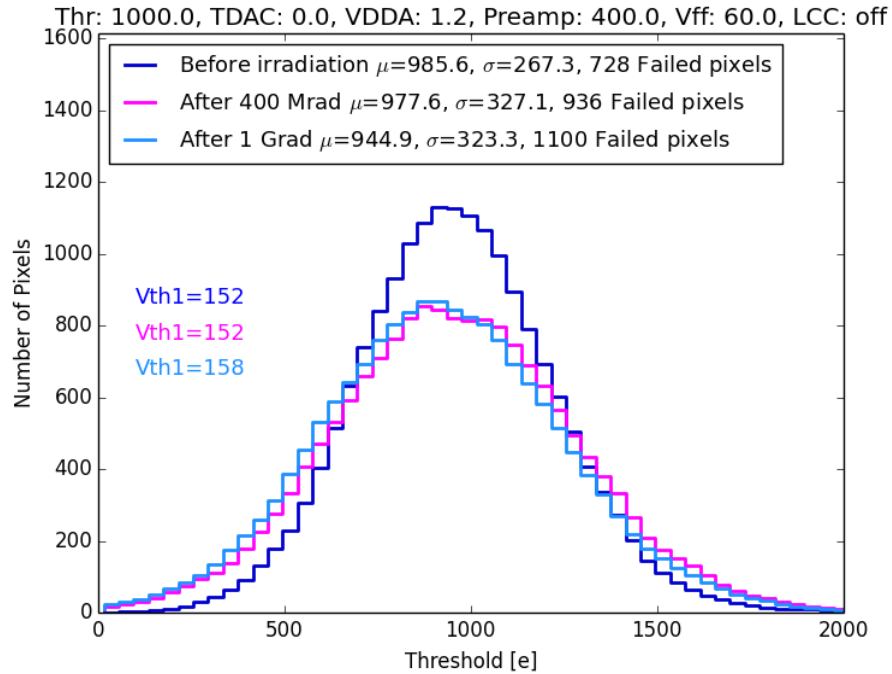


Untuned threshold distributions normalized to total number of good pixels

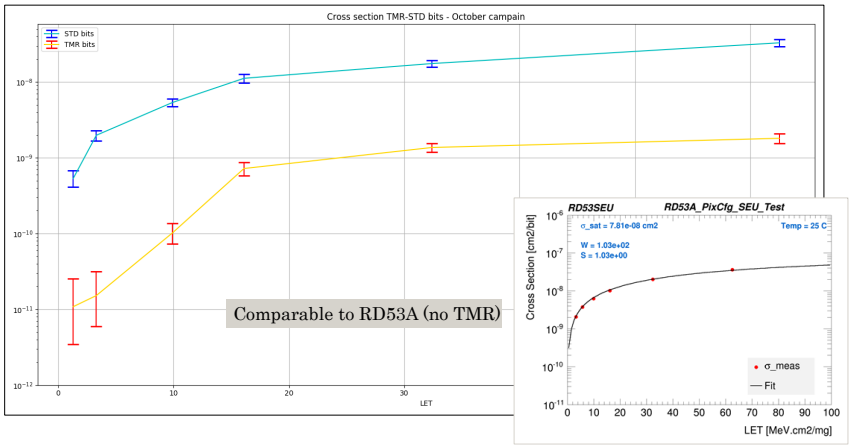
- RD53A is a demonstrator for ITkPix-V1. The differential analog FE has been significantly improved from RD53A to ITkPix-V1
- Check whether ITkPix-V1 has a stable working point after receiving high radiation
  - Use low temperate (-40°C) and low VDDA are used to emulate high radiation damage: ITkPix-V1 shows more stable operation compared with RD53A

X-ray irradiation and single-event-effect studies

- Various testing sites now have X-ray machines
  - **ITkPix-V1 appears to be radiation hard up to 1 Grad!**
- Single-event-effect (SEE) studied in test beams
  - Important registers are triplicated in ITkPix-V1 and have low SEE xs



Pixel configuration tests – cross section (ions)

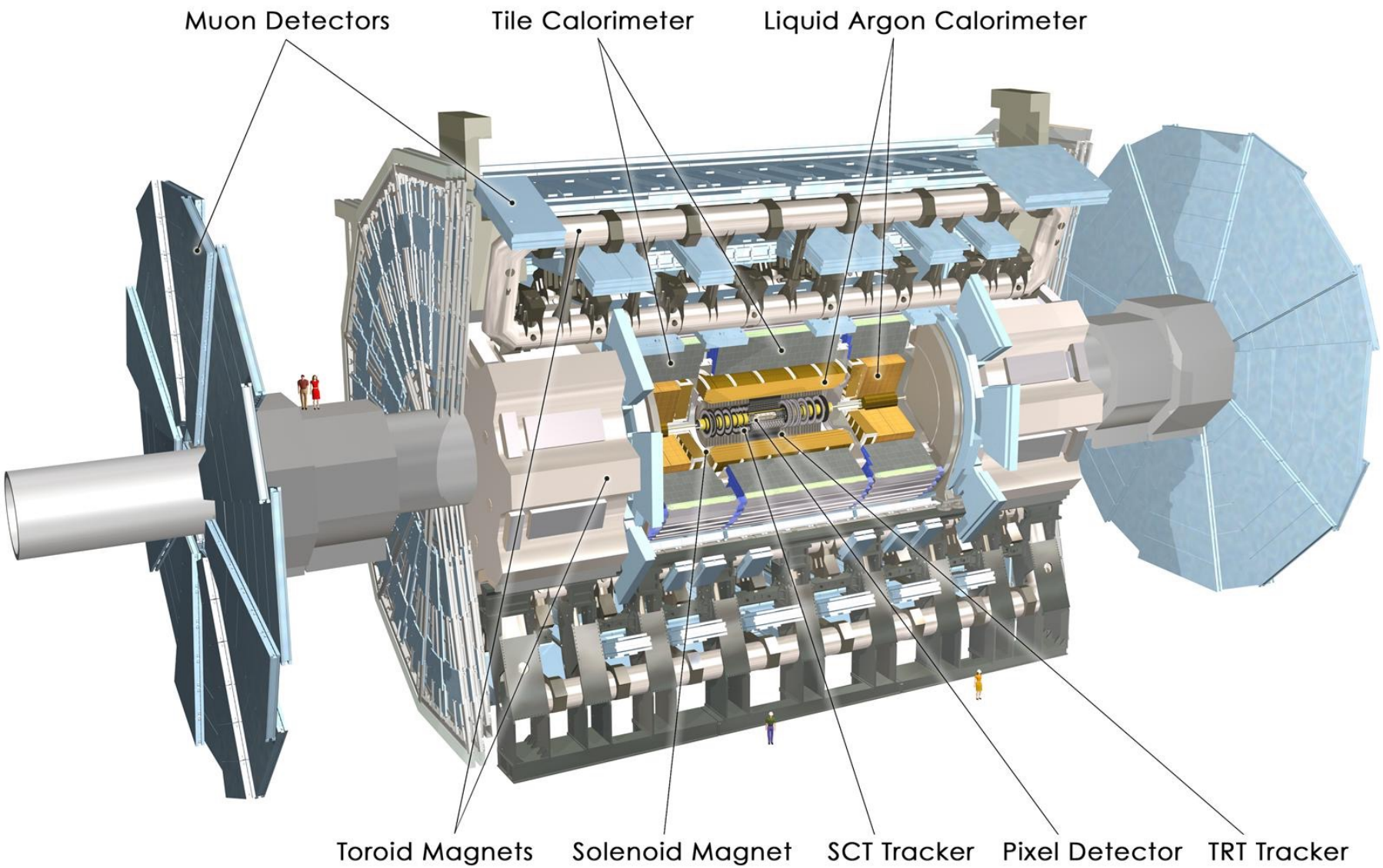


Conclusions

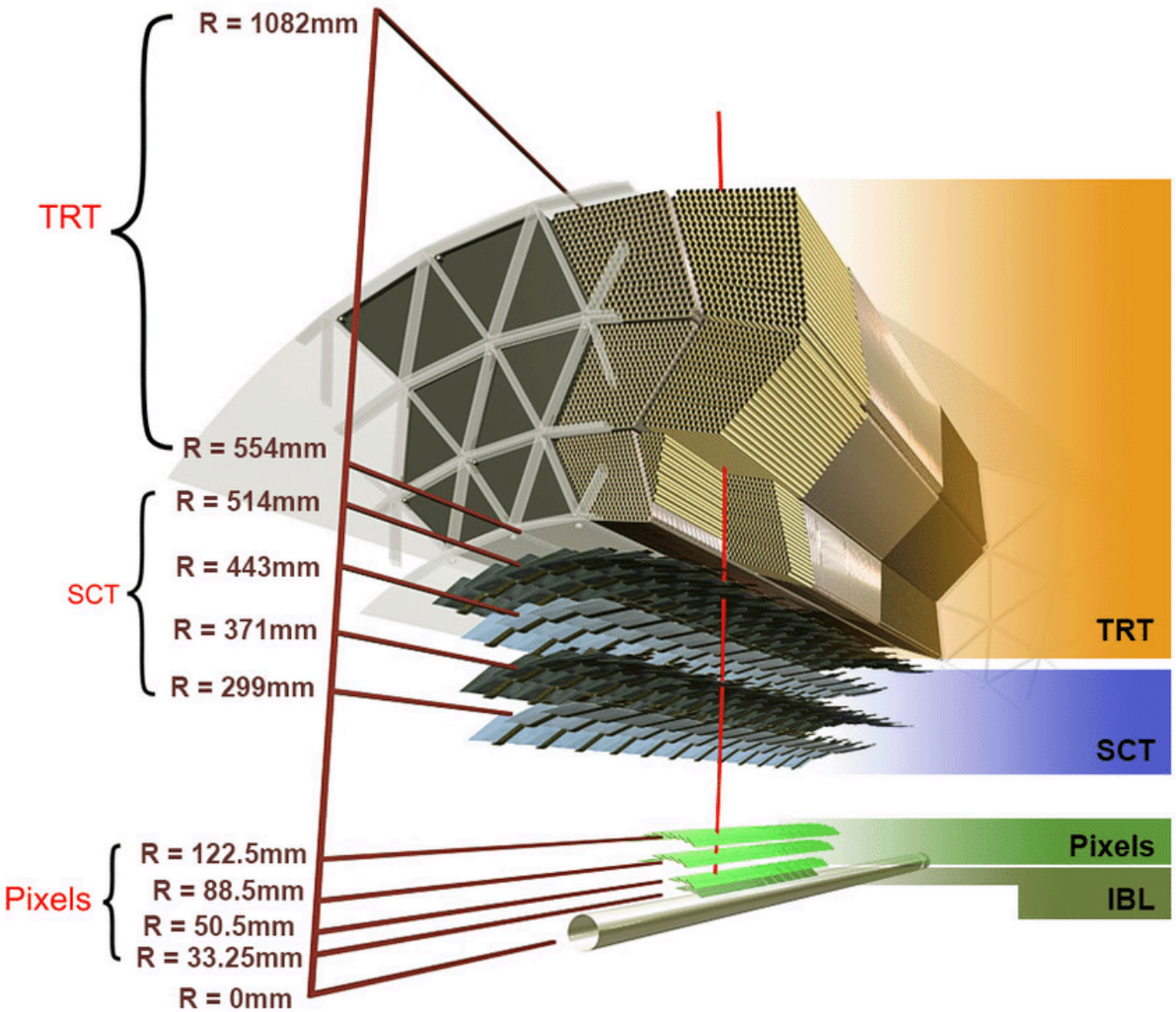
- ITkPix-V1 validation in good progress: determines readiness to submit ITkPix-V2
  - **Except for the ToT memory issue, ITkPix-V1 chip has worked wonderfully so far, with only some minor bugs identified**
  - Many important studies not covered in this talk due to limited time
- ITkPix-V1.1 with ToT memory patch will be used as pre-production chip. Expect to be used for sensor assembly and system tests. Stay tuned!

Backup

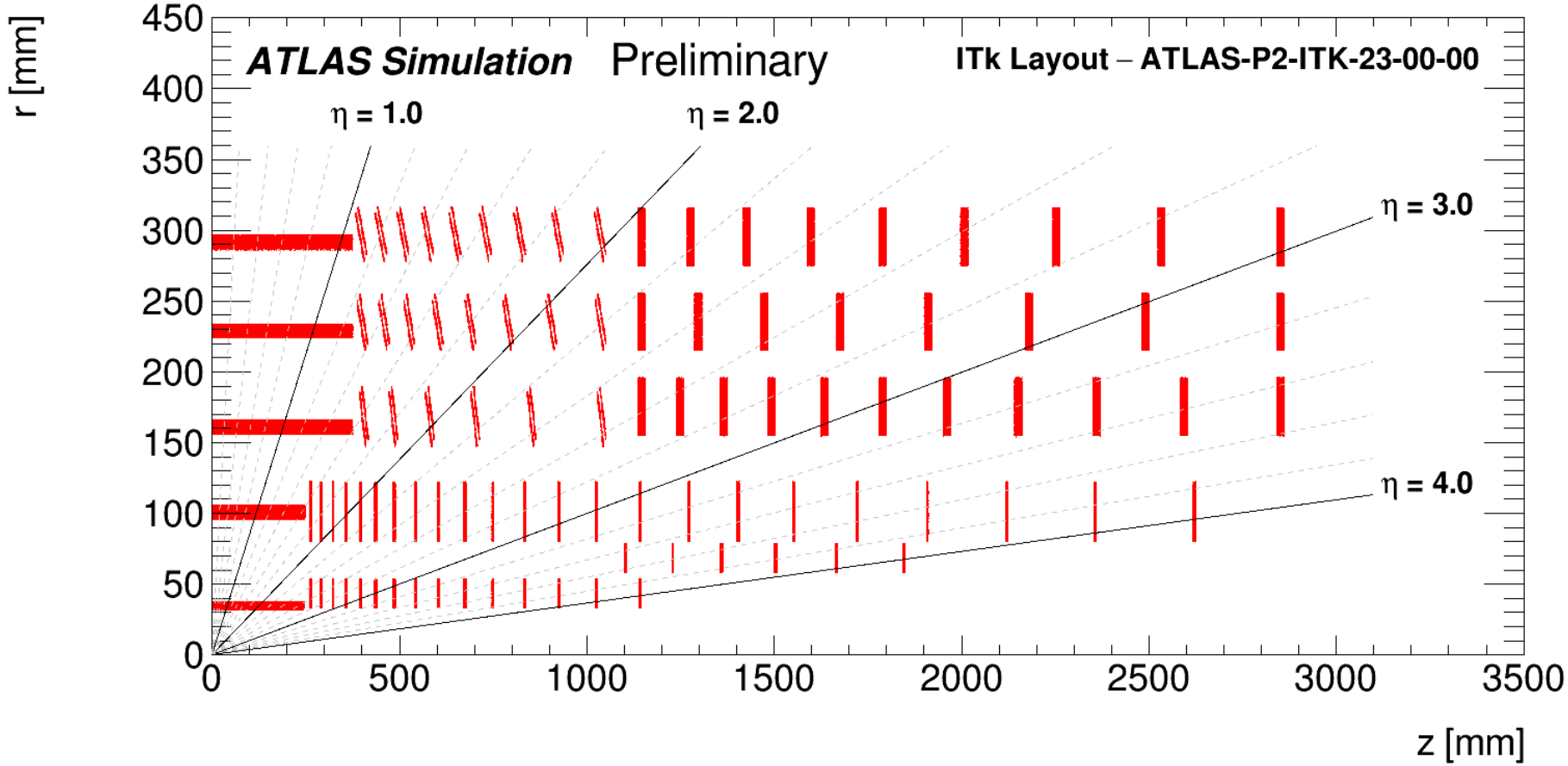
ATLAS detector



Current ATLAS Inner Detector

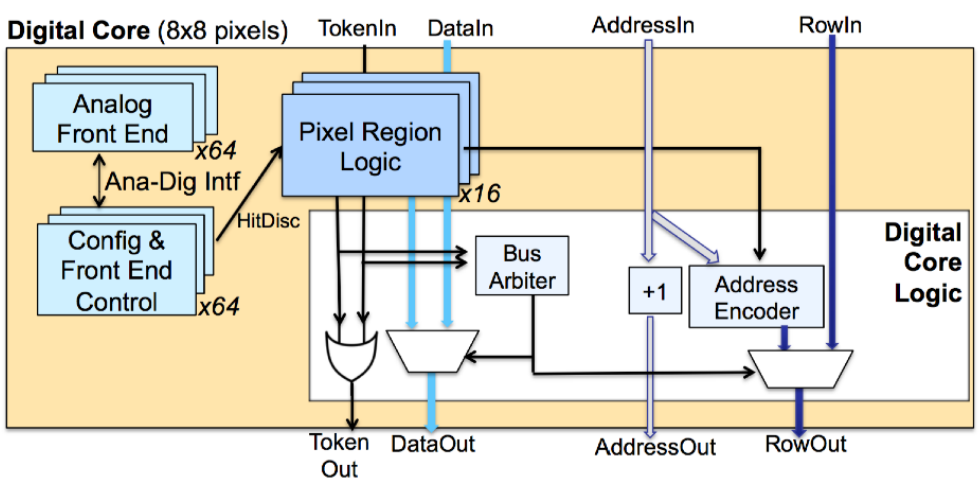


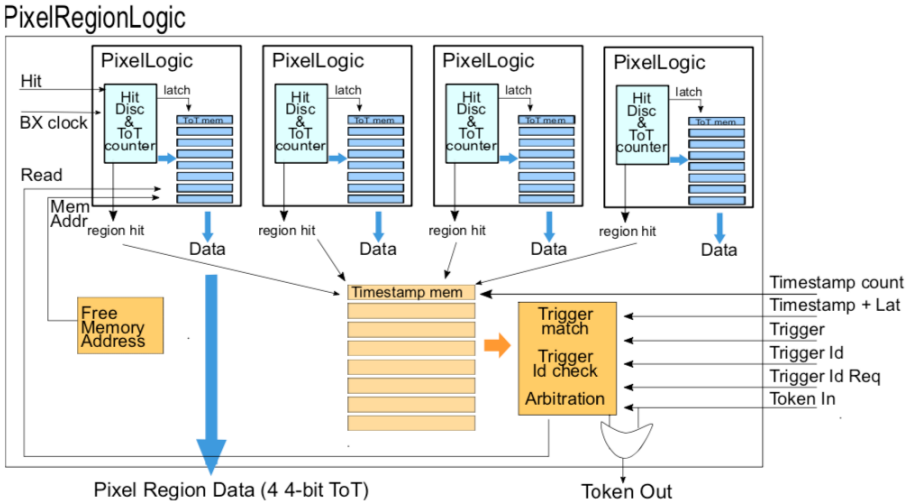
ITk Pixel Detector layout



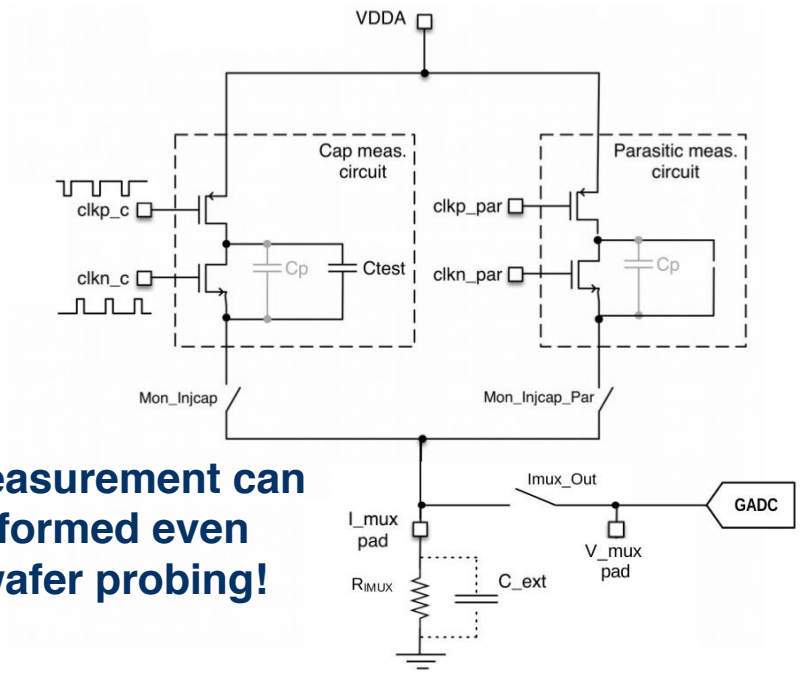
ITkPix-V1 digital block

- Organized in digital cores (8×8 pixels)
  - Cores are stepped & repeated to create pixel matrix
  - Each digital core contains 16 1×4 Pixel Region logics
- Each pixel has 4-bit time-over-threshold (ToT) memory. Hits saved as ToT associated with time stamp (bunch crossing)

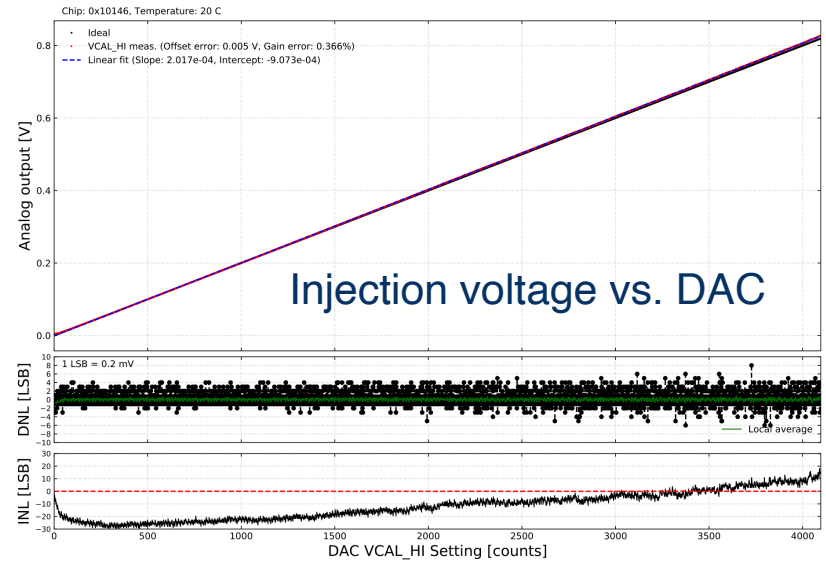


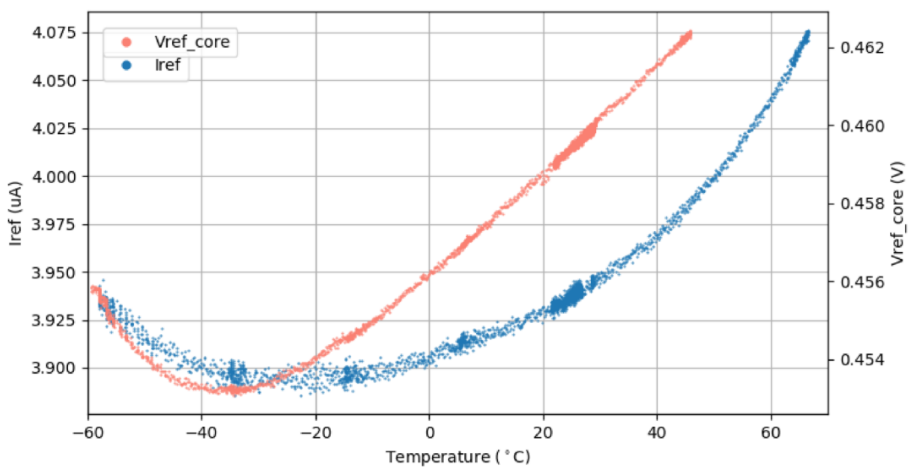


Characterization of analog circuits



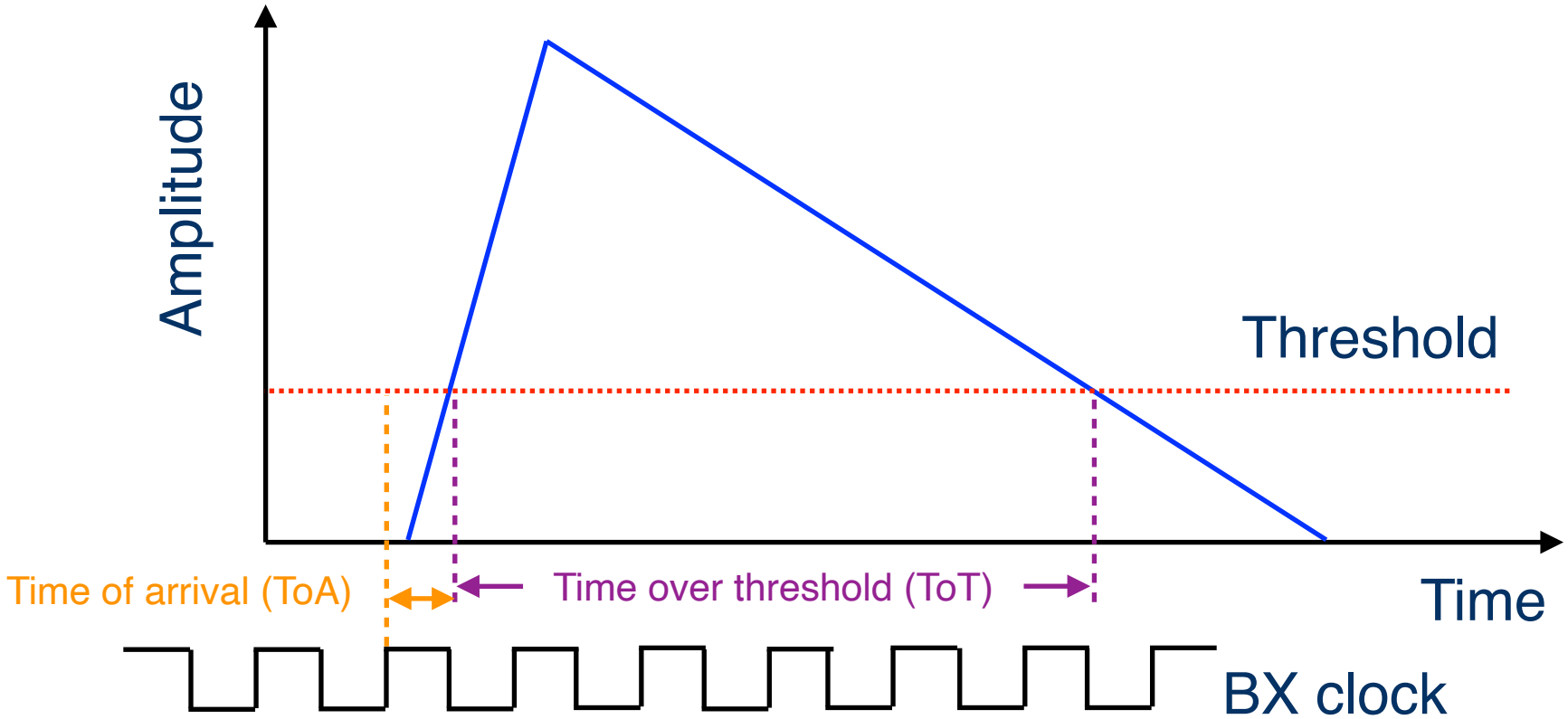
C_{inj} measurement can be performed even after wafer probing!





- Injection capacitor measured to be 7.5 fF using internal circuit
- Injection voltage vs. DAC shows good linearity
- Reference voltage vary by 4% within 120°C range

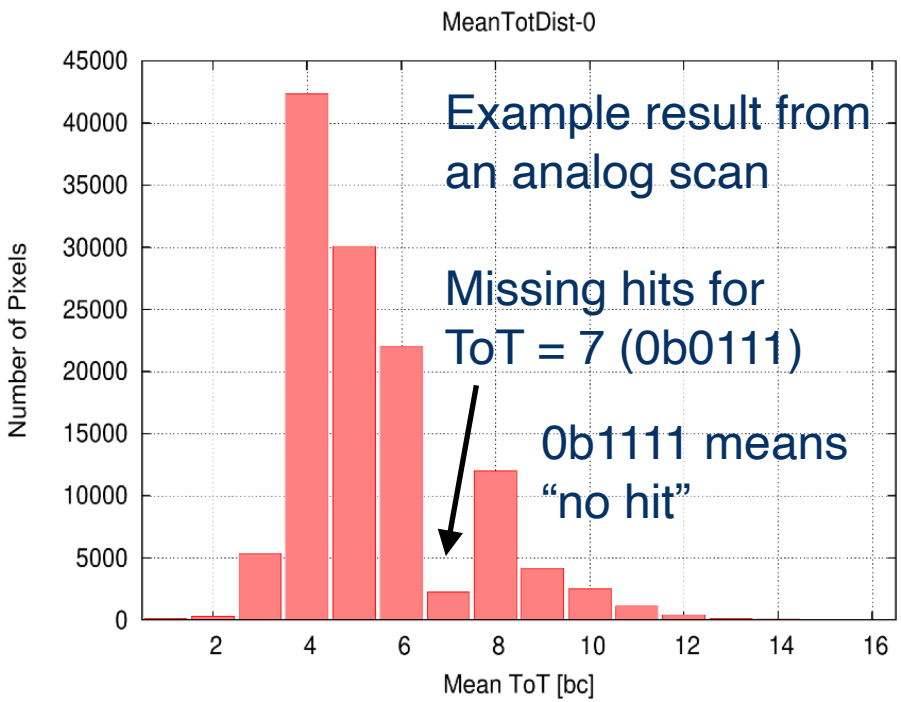
Data from ITkPix-V1



- Standard ToT data: pixel address (column, row) + ToT in unit of **40 MHz** BX clock
- **Precision ToT data**: record precision ToT/ToA counted in **640 MHz** clock on each hit bus. Require reverse-engineering of pixel address according to the pixel enable mask

Issue in ToT memory

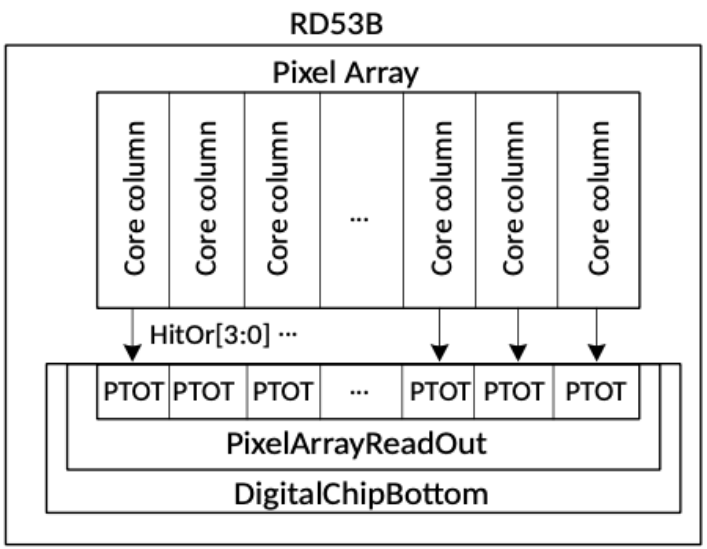
- Notice large digital current and loss of hits when ToT value contains more than one bit set to “1”
  - Traced back to a bug in the multi-latch ToT memory that allows a direct path from VDDD to ground under specific circumstances, and leads to some internal nodes not being on a well defined potential

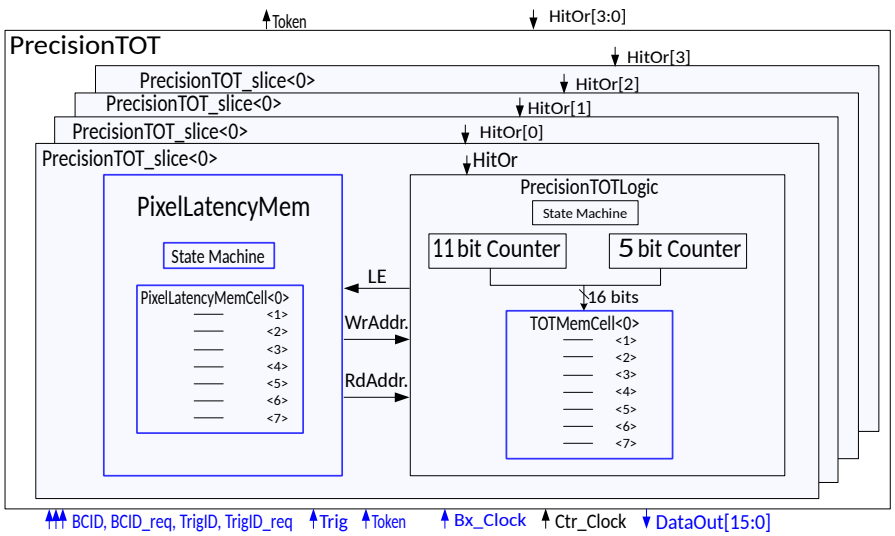


- Patch applied in ITkPix-V1.1, which is becoming available at various testing sites
- ToT memory redesigned to use single latch in CMS chip (CROC) and ITkPix-V2 to provide fully clean solution

Mitigate ToT memory issue

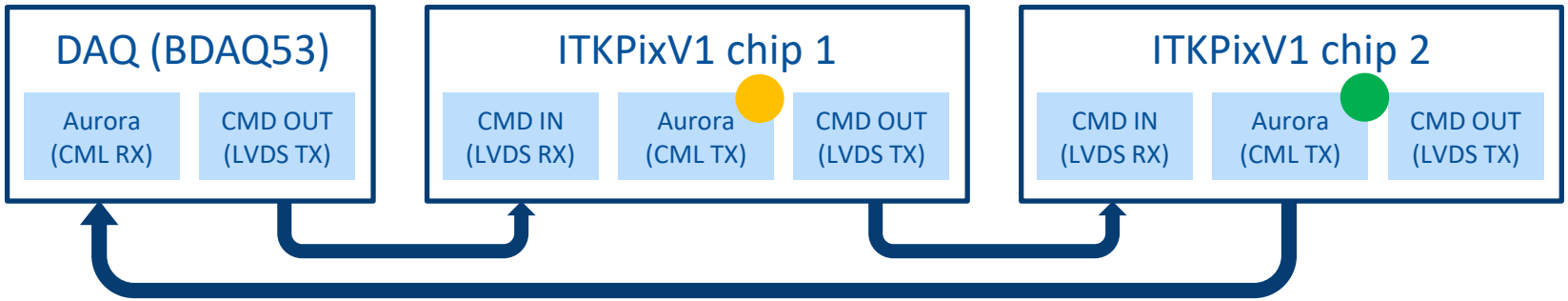
- **Large digital current:** mitigated by constantly resetting ToT memory to 0b0000 after calibration injection
  - Can reduce digital current to normal value around 0.65A
- **Lost hits:** recovered from precision ToT data provided for each HitOr bus at chip bottom
  - Can only enable one pixel on each HitOR per injection
- **ITkPix-V1 chip with above mitigations can be used for most tests that are not affected by large current or require taking random hits**

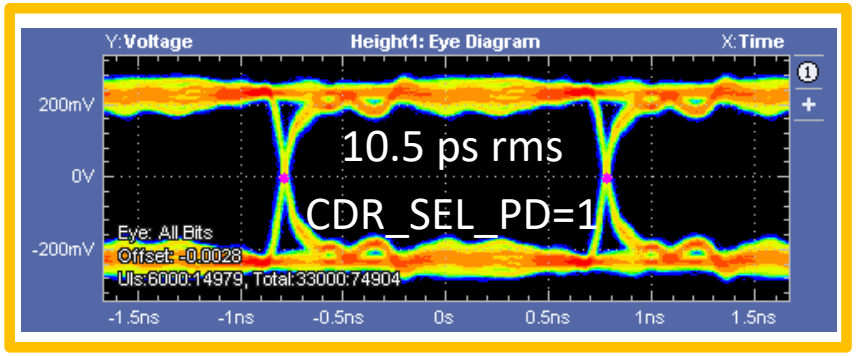


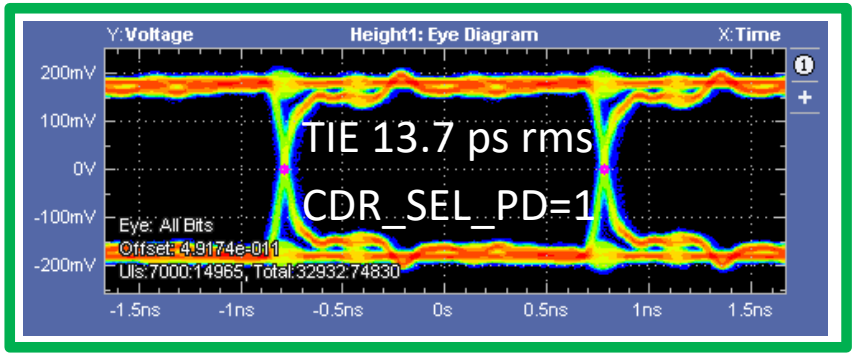


CMD forwarding

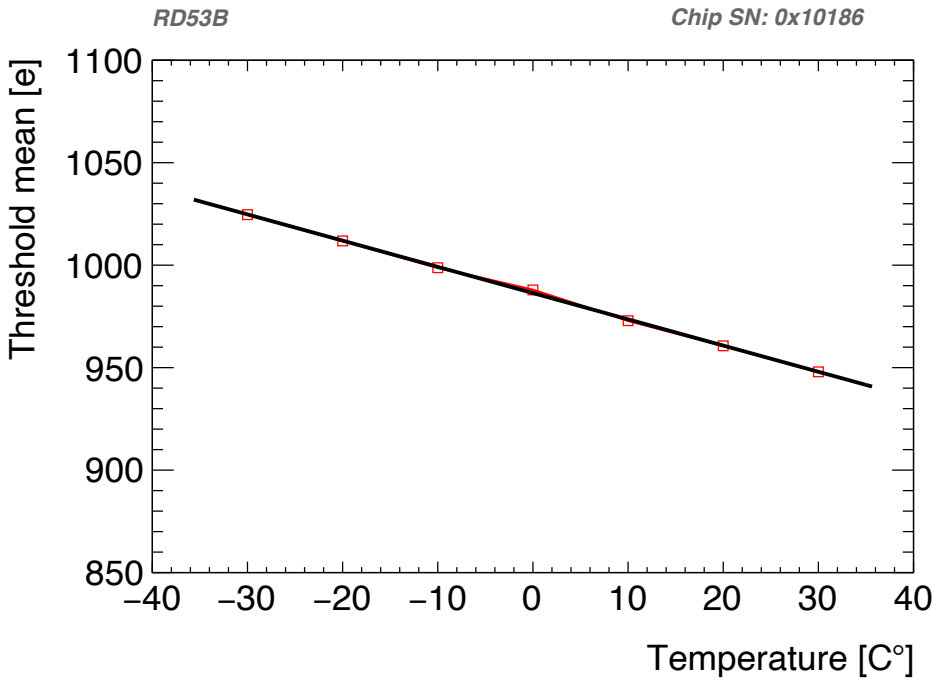
- In ITk Pixel detector, CMD will be forwarded from one module to next on the same stave
- ITkPix-V1 can forward CMD using GPO_LVDS, both with and without re-sampling (improvement over RD53A)
- **First test using two SCCs show good link quality. Both chip configured**

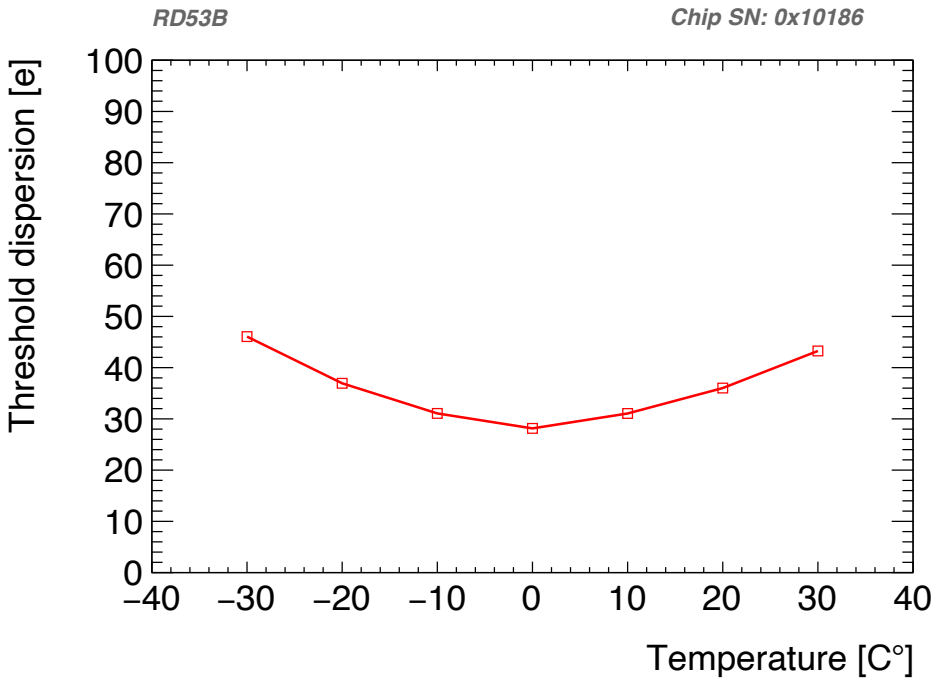
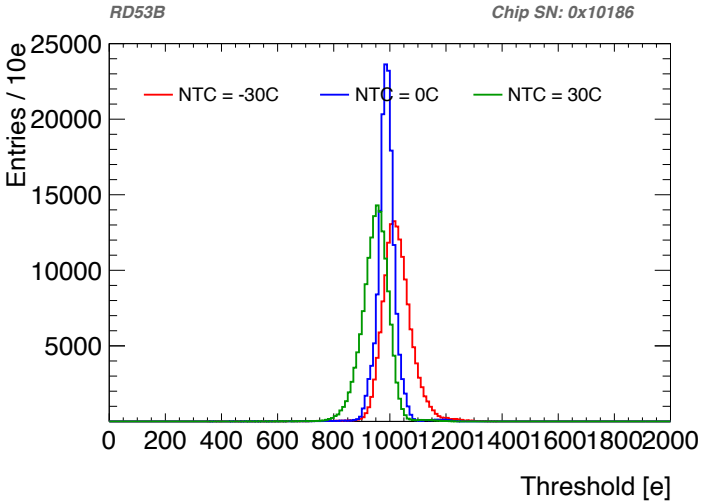






Threshold vs. temperature





- Tune threshold to 1000e at 0°C, then measure threshold at different temp.
  - Threshold mean changes by **-1.3e/°C**
  - Threshold dispersion minimal at 0°C, then increase when temp. deviates