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LArPix-v2: a commercially scalable large-format 3D charge-readout scheme for LArTPCs

Brooke Russell on behalf of the LArPix Team

CPAD 2021

March 22, 2021

Archetypal single-phase LArTPC for accelerator ν oscillation physics

+ Massive, homogenous, dense target for appreciable neutrino interaction rate

+ Fine grained 3D tracking with local dE/dx information

– Ambiguities associated with spatial projections

➔ Realize a true 4π charged particle detector with *pixel readout*

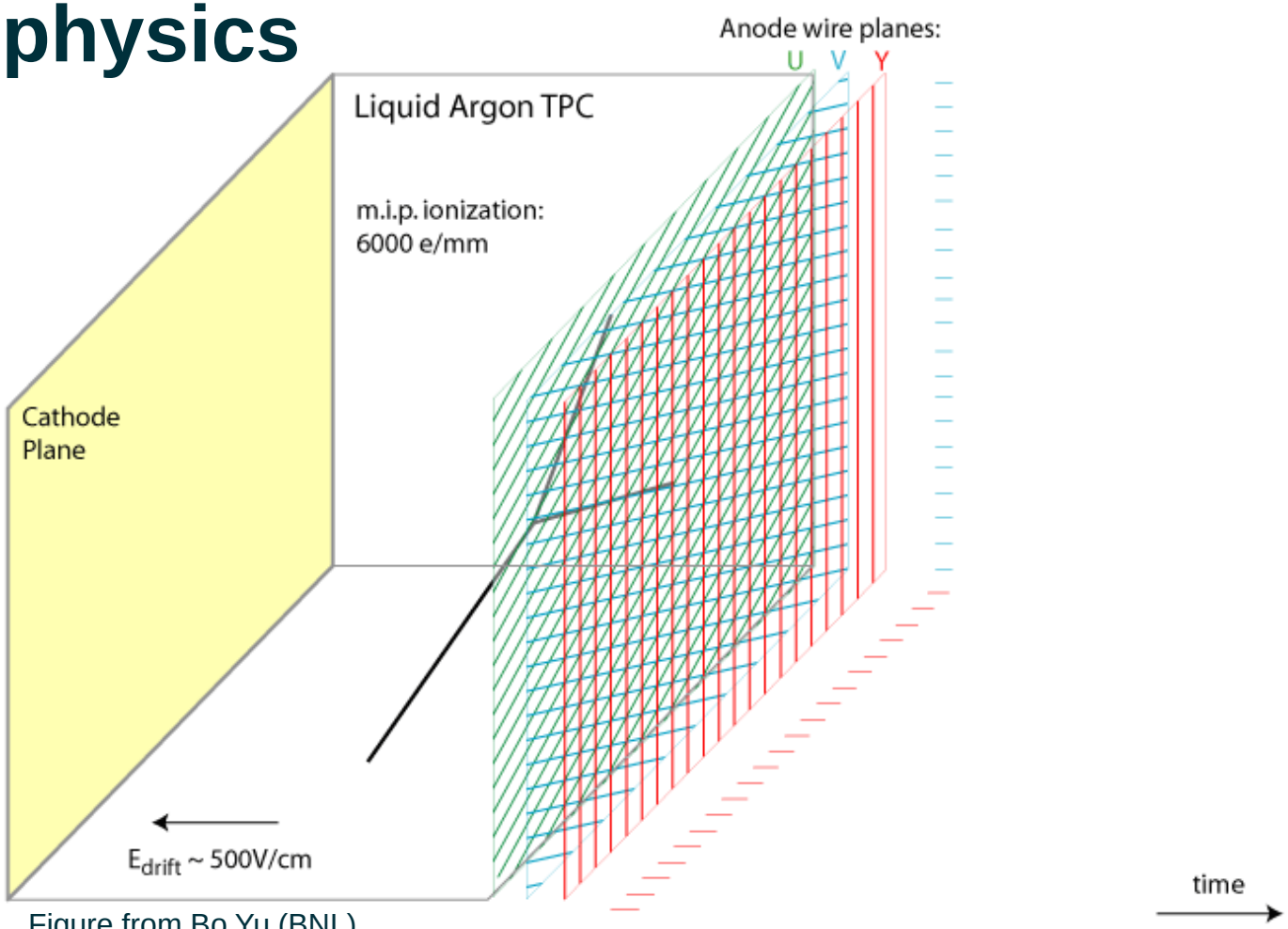
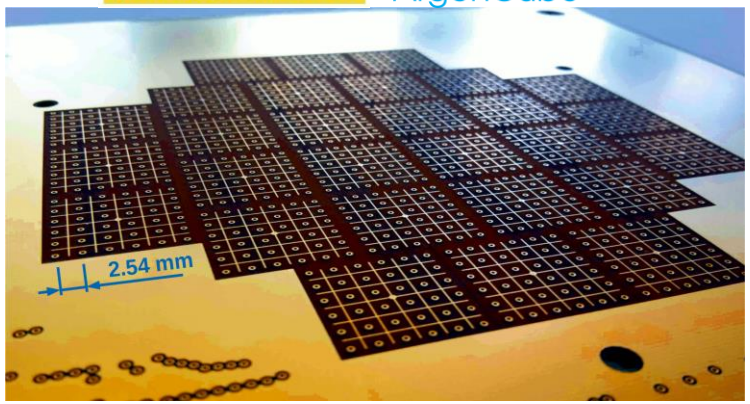


Figure from Bo Yu (BNL)

Pixel Readout R&D for LArTPCs

Key challenges:

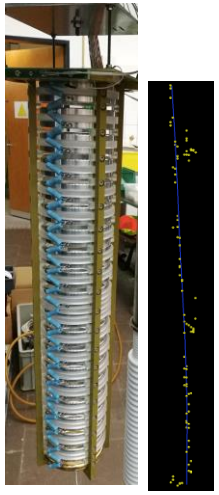
- Power
- Channel density
- Cost

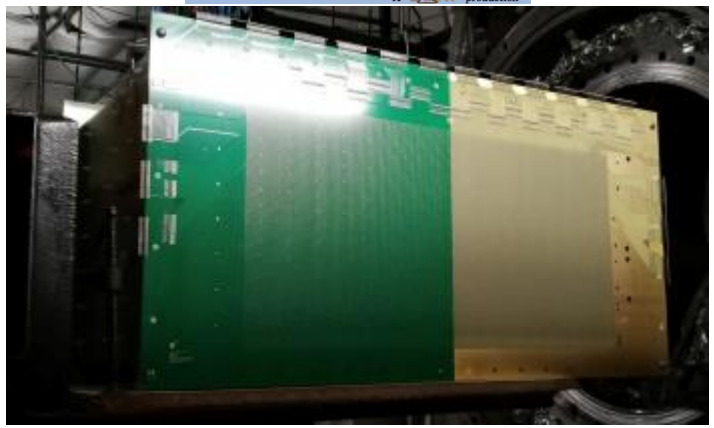


Demonstrated pixel readout in LAr (Summer ‘16)

Combined pixel signals to dramatically reduce channel count

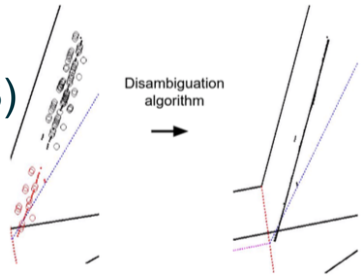
J. Asaadi *et al.* Instruments 4 (2020) 1,9



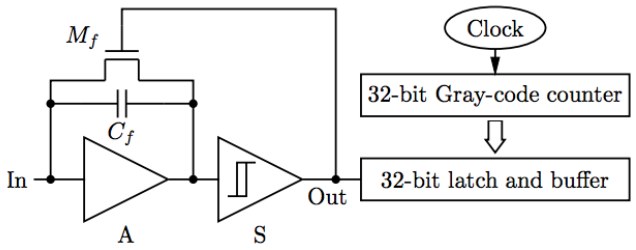


Large-area pixel sensor in LArIAT (Dec. ’17 – Jan. ‘18)

28,800 pixels merged into 480 channels



Q-Pix



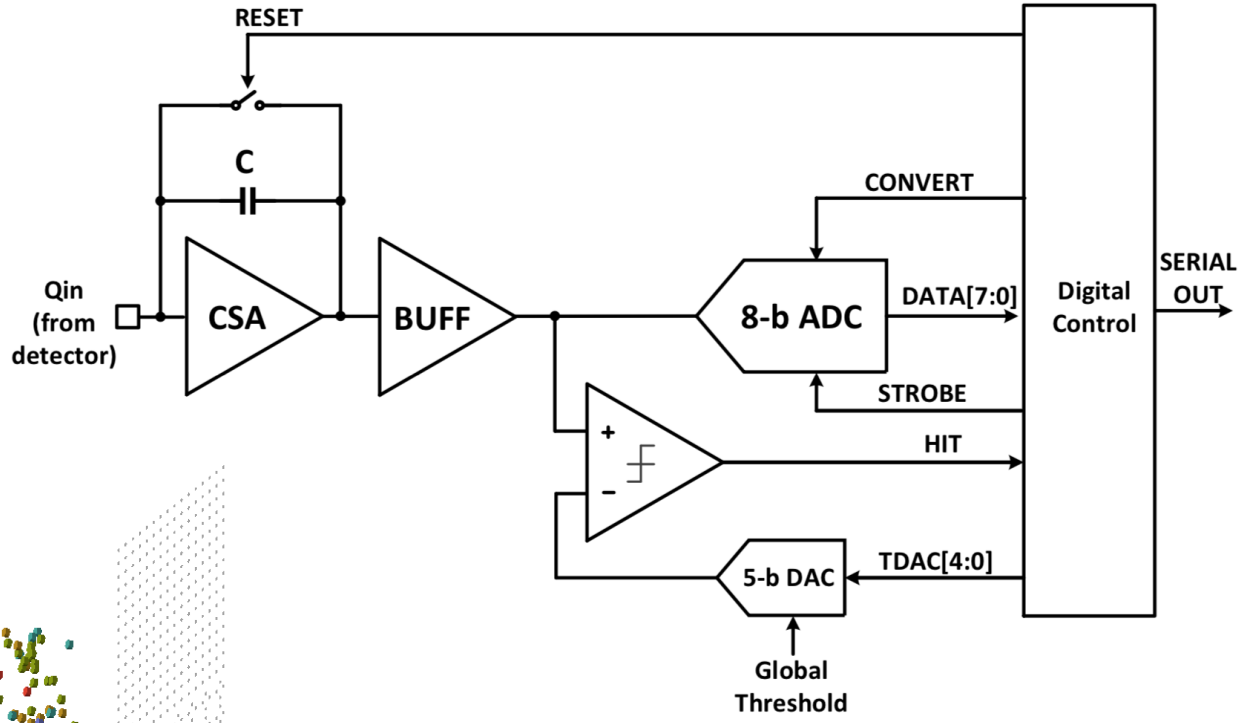
Novel concept using a unique CSA, Schmitt trigger for each pixel

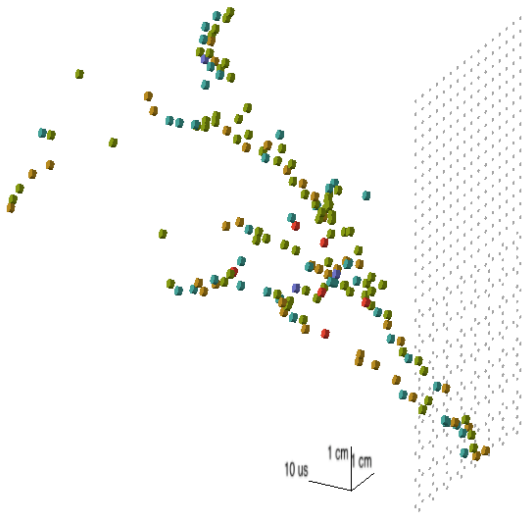
Given a Scmitt threshold *dQ*, current arriving at pixel in interval *dt* between triggers is *dQ/dt*

Based on conceptual design from D. Nygren & Y. Mei arXiv:1809.10213

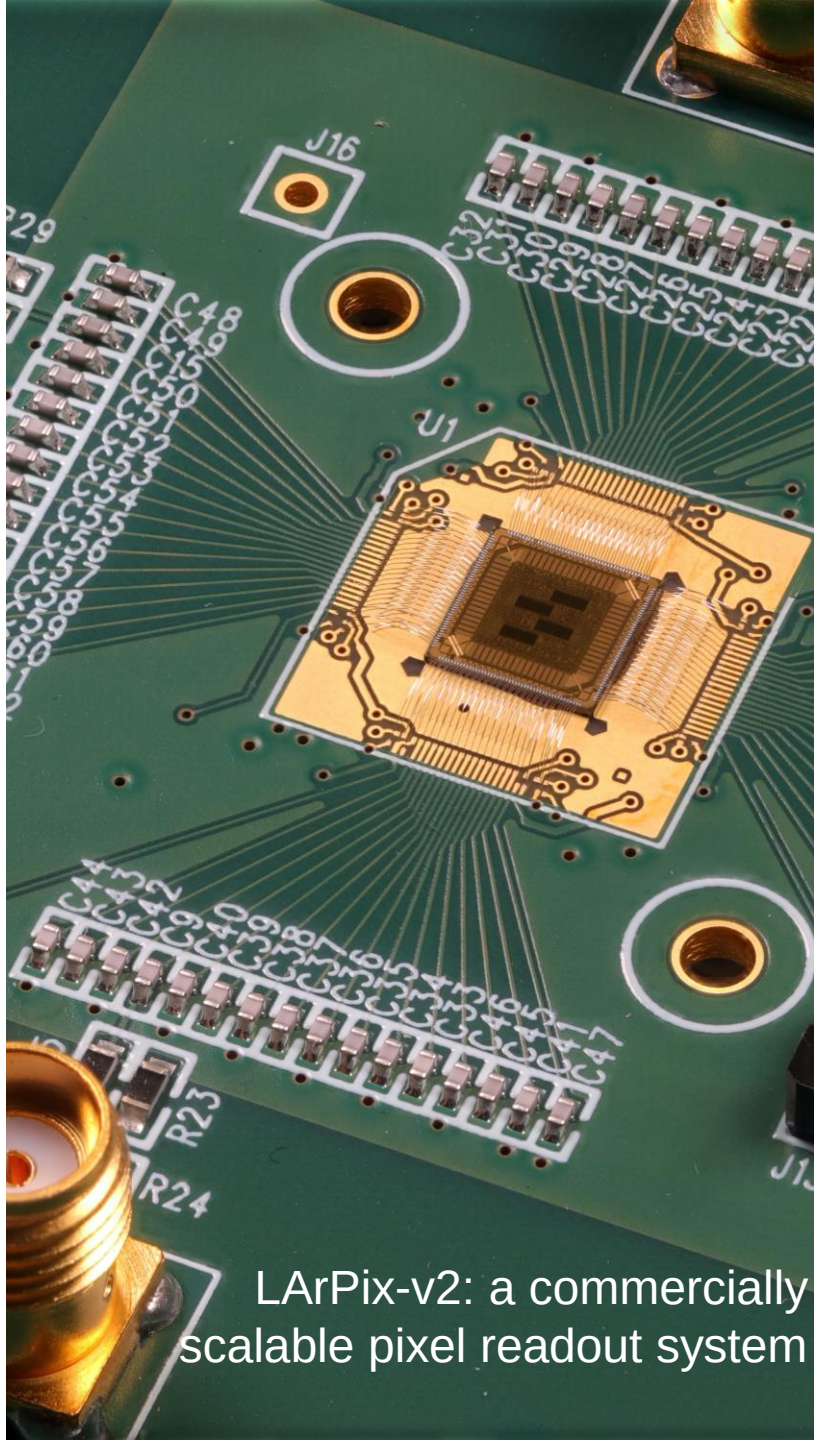
See talks from:
Gang Liu
Austin McDonald
Elena Gramellini

Low-power, integrating amplifier with self-triggered digitization and readout





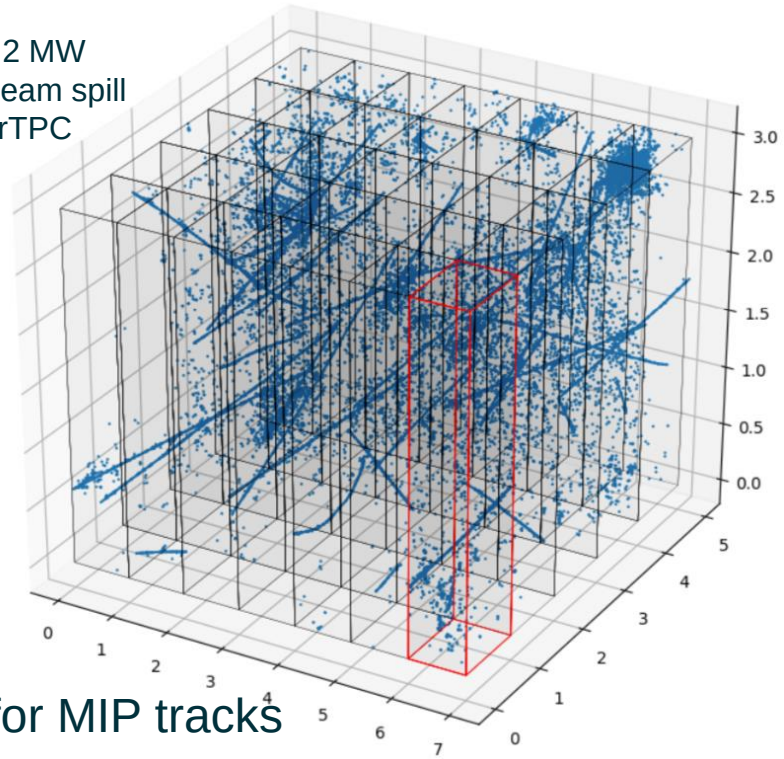
LArPix-v1: first proof of principle demonstration by Dan Dwyer *et al. JINST 13 (2018) P10007*



LArPix-v2: a commercially scalable pixel readout system

LArPix System Requirements

Example FHC 1.2 MW
LBNF neutrino beam spill
at DUNE ND LArTPC



Provide true 3D imaging of TPC ionization

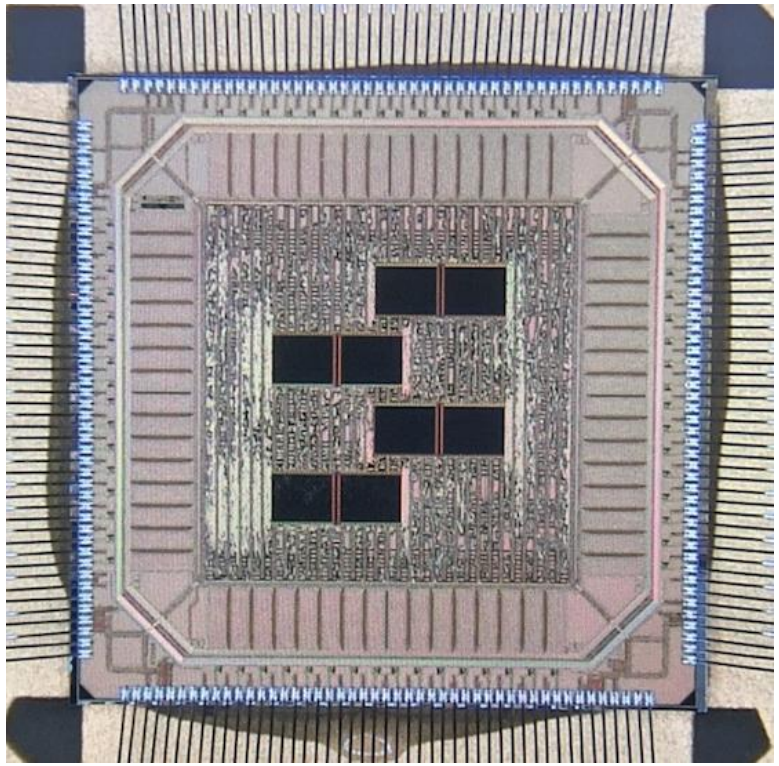
- Overcome beam neutrino pileup in high rate environments
- High fidelity imaging of large multiplicity neutrino topologies

Noise	< 1000 e- ENC	S/N ratio of >20:1 for MIP tracks
Channel Density	64 channels / die	Unique front-end channel for pixels at ~4 mm pitch
Power	< 200 uW / channel	Low-power to avoid boiling LAr
Digital Multiplexing	> O(1k) pixels / I/O channel	Viable cable plant & cryostat feedthroughs
Robustness	< 0.1% tile failures	Minimize single-point failures in cryogenic environment Anode tile robust to failed ASICs
Scalability	> 200 m^2 anode @ < \$10k/m^2	Design compatible with standard large-scale commercial electronics production techniques

LArPix-v2 ASIC

Custom ASIC with amplifier, digitizer, multiplexer

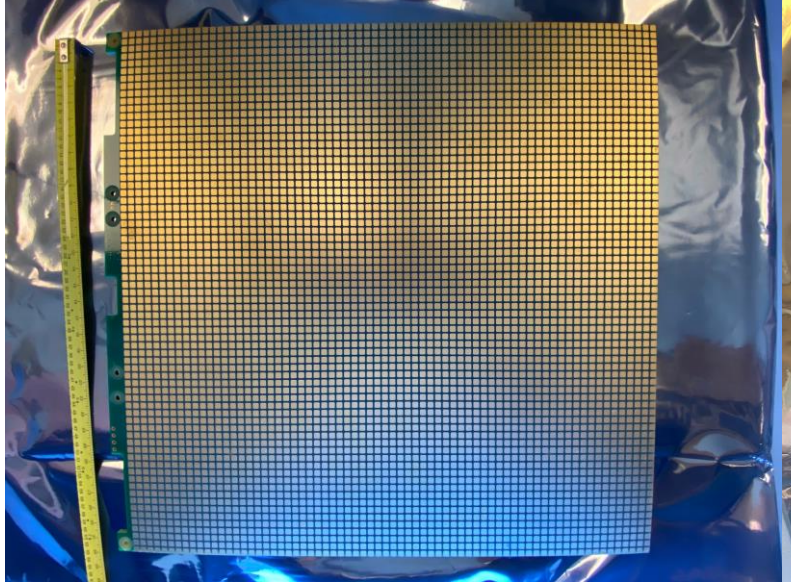
- Low-power, low-noise cryogenic-compatible ASIC
  - S/N ratio of ~30:1 for MIP tracks
- No resistive feedback or shaping
  - Charge stays on pixel until you do something with it
  - Self-, external-, cross-, and periodic-trigger reset modes
    - Optional “burst” modes to process N hit cycles
- Pixels are continuously active
  - Serial data packets stream out of system as channels self-trigger
  - Serial I/O data rate is slow (~ 5Mb/s per digital I/O channel) to limit digital power in cryogenic environment
  - Modest data volumes: ~1 MB/s per square meter of anode in surface cosmic flux
- **Main issue:** digital I/O has excessive capacitive coupling to analog signal inputs
  - Increases pixel noise during data transmission
  - Biases pixel self-trigger threshold during data transmission

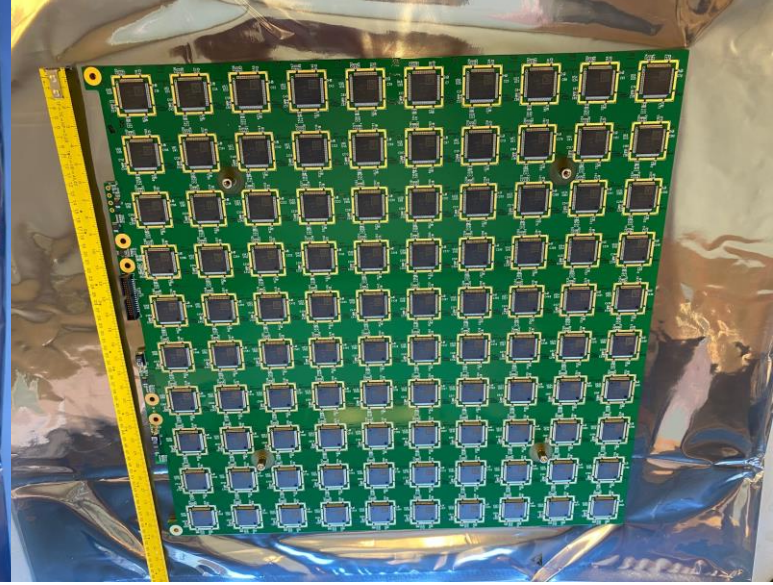


64 channels on 25 mm^2 die

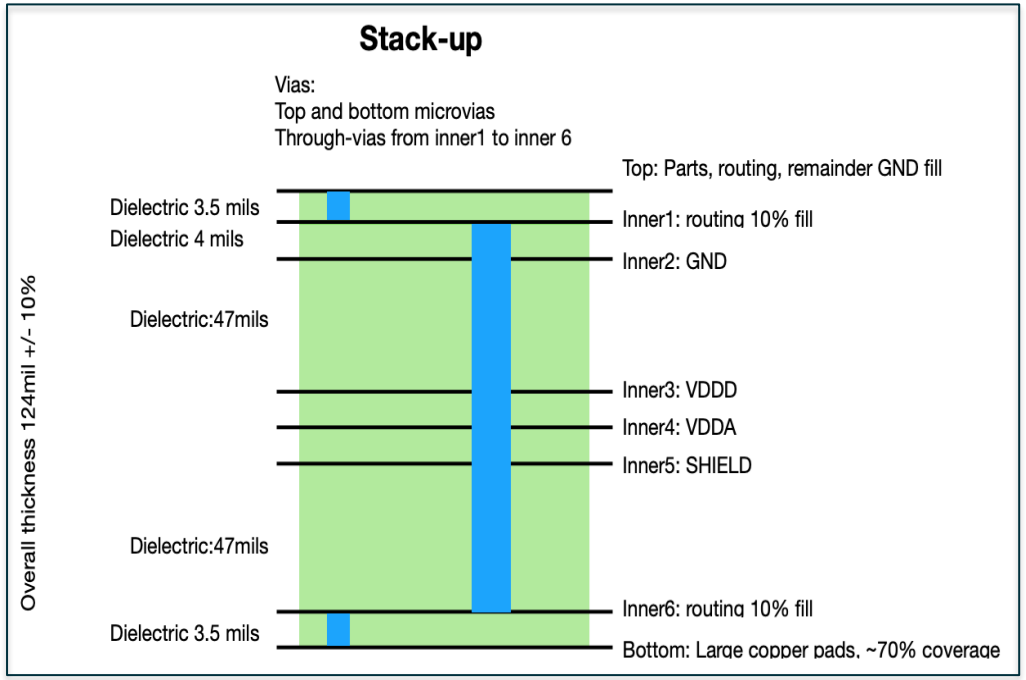
LArPix-v2 Anode Tile

Composed of 2D grid of charge-sensitive conductive pixels or pads





- High channel density
  - 10x10 array of ASICs instrument pixel PCB-based anode (32 cm by 32 cm)
  - O(100k) channels per square meter of anode
- LArPix ASIC is the only active component in cryogenic active
  - Remaining components all passive: decoupling capacitors, resistors, ESD protection diodes, one cable connector
- Scalabe design compatible with standard large-scale commercial electronics mass production techniques
  - >200 m^2 anode at <$10k/$m^2$
  - 'Tileable' design to cover anodes of arbitrary scale
  - Quick-turn (~few weeks) fully-commercial production and assembly

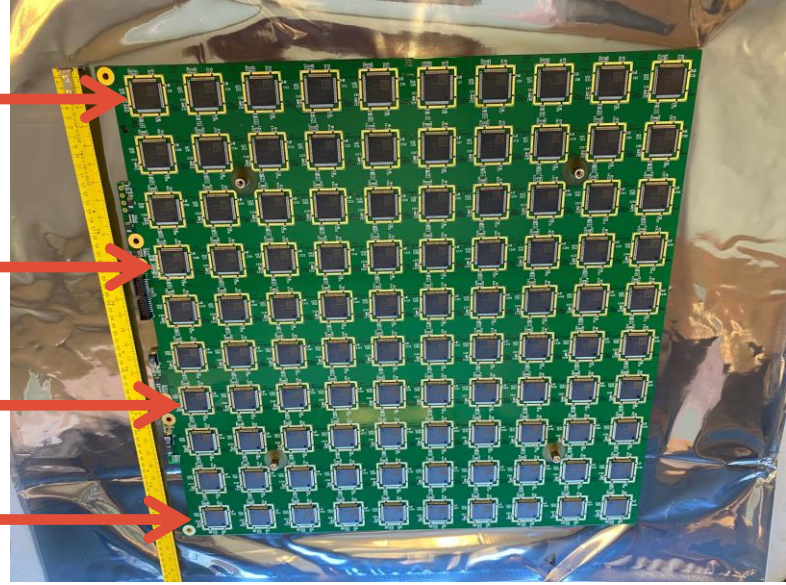


Micro-vias to enhance shielding between digital/analog traces and vias

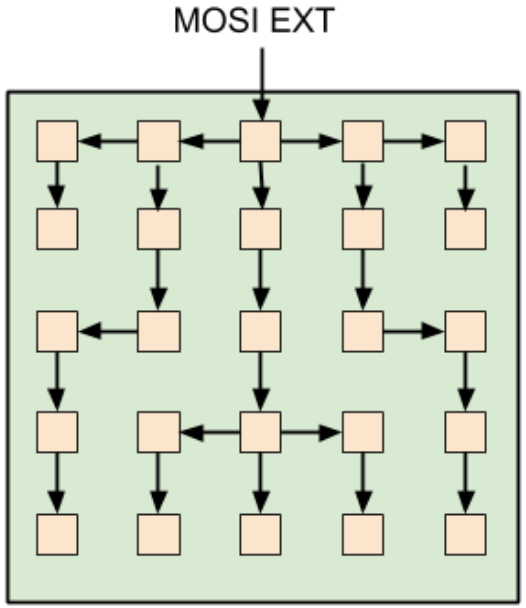
LArPix-v2 Robustness

- Minimize single-point failures in cryogenic environment
  - Tile robust to failed ASICs
- Robust to repeated cryogenic cycling

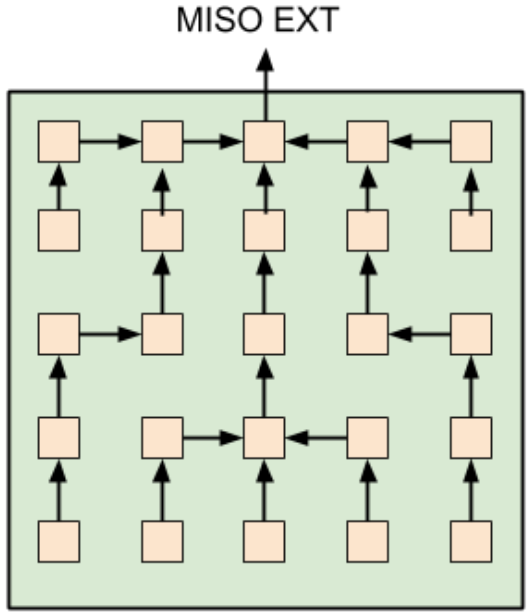
Four chips have direct off-tile I/O channels



Example: 5 x 5 Pixel Tile



Upstream configuration commands



Downstream data flow

- Each tiles has an independent cable (power and I/O) to the outside world, with fully-redundant I/O channels (x4)
- I/O can occur between any neighboring ASICs on pixel tile

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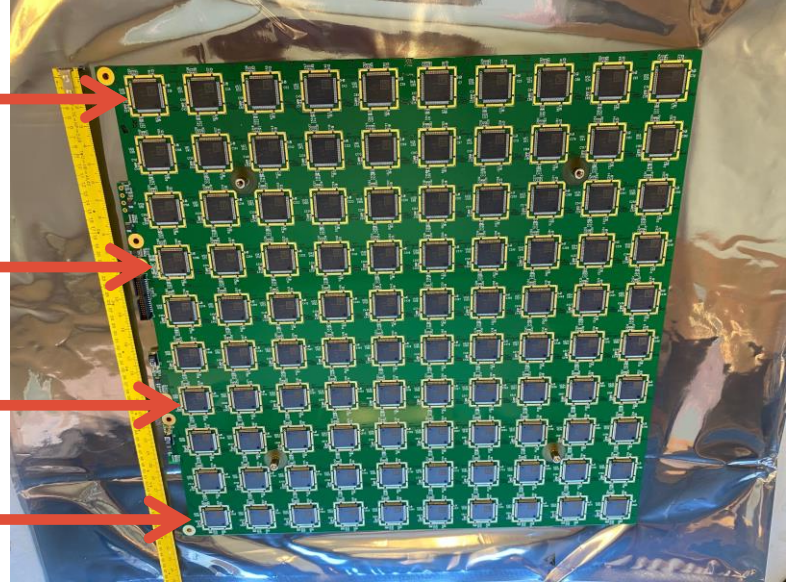

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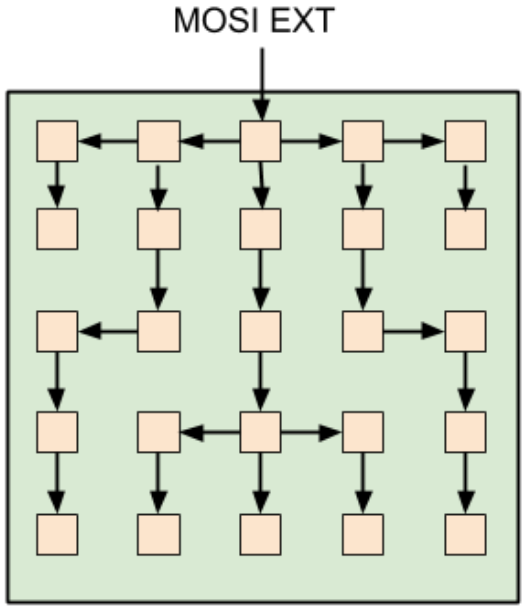

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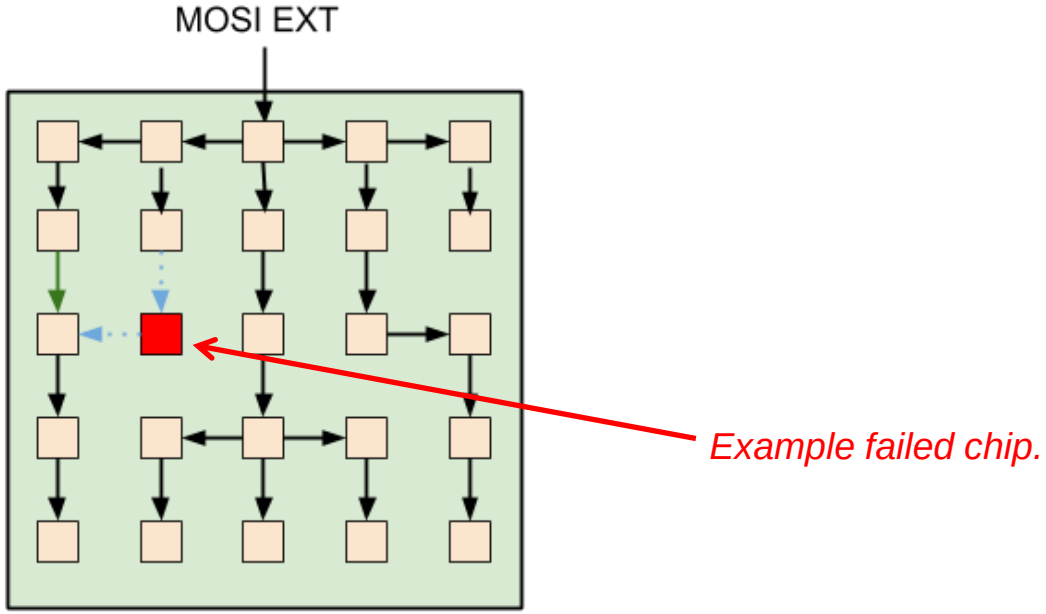
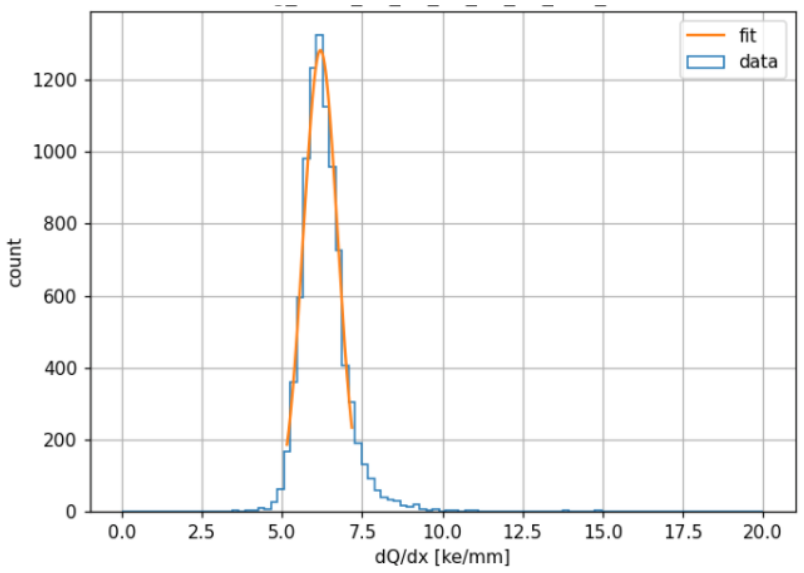


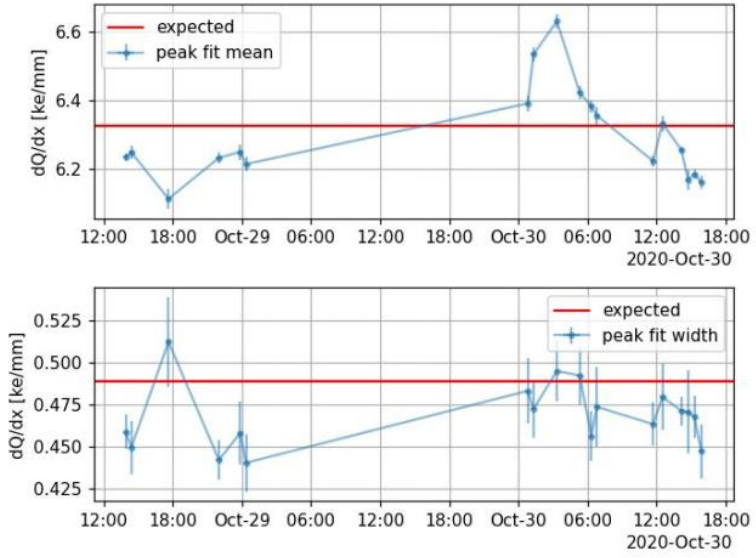
Network reconfigured to avoid failed ASIC

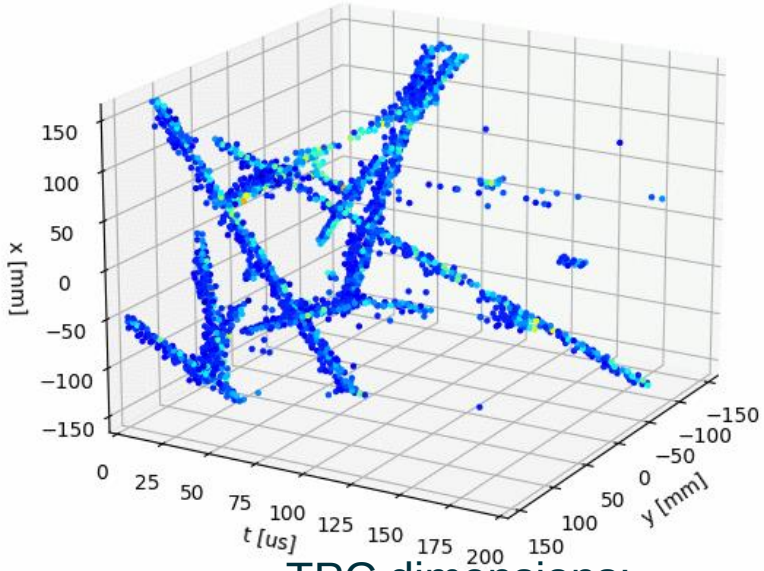
SingleCube

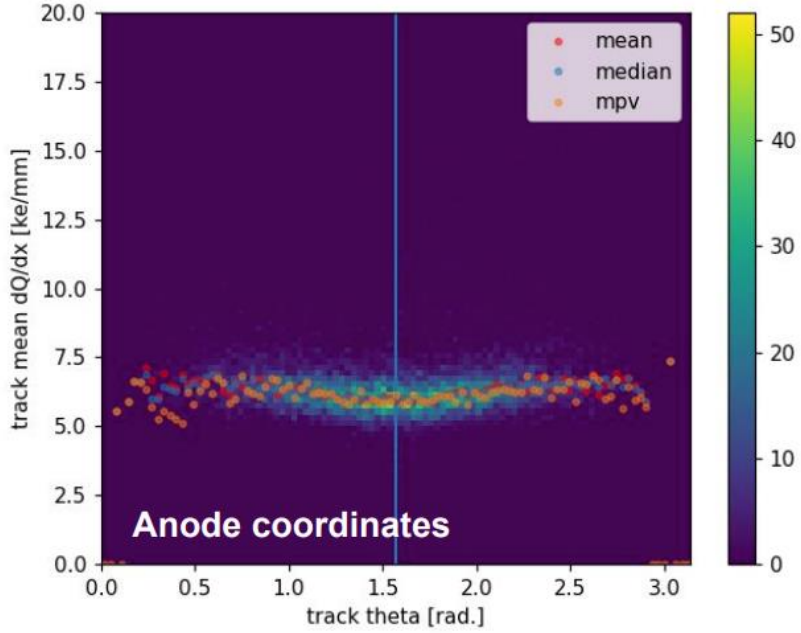
Small-scale system integration demonstrator

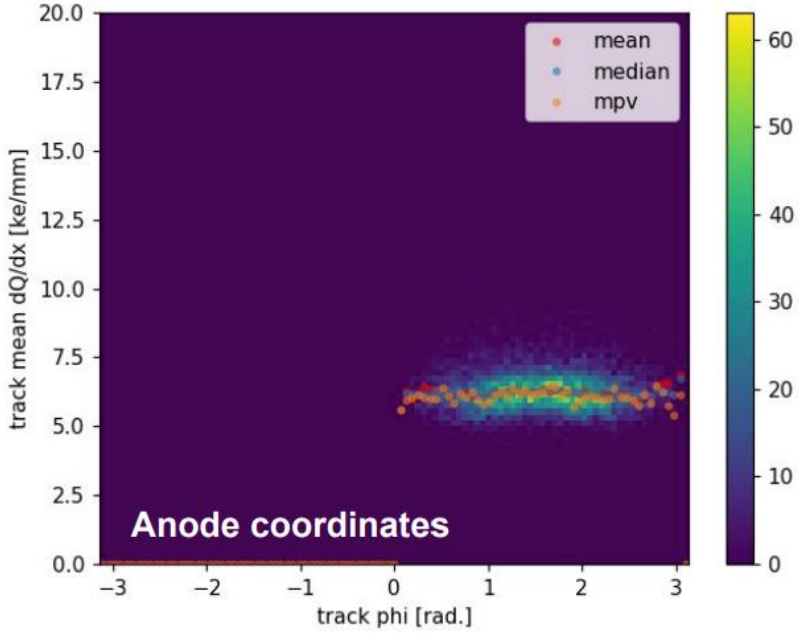
- Charge stable and consistent with expectation
- Small variation in dQ/dx based on muon track orientation to anode
- LArPix data provides independent measurement of LAr purity











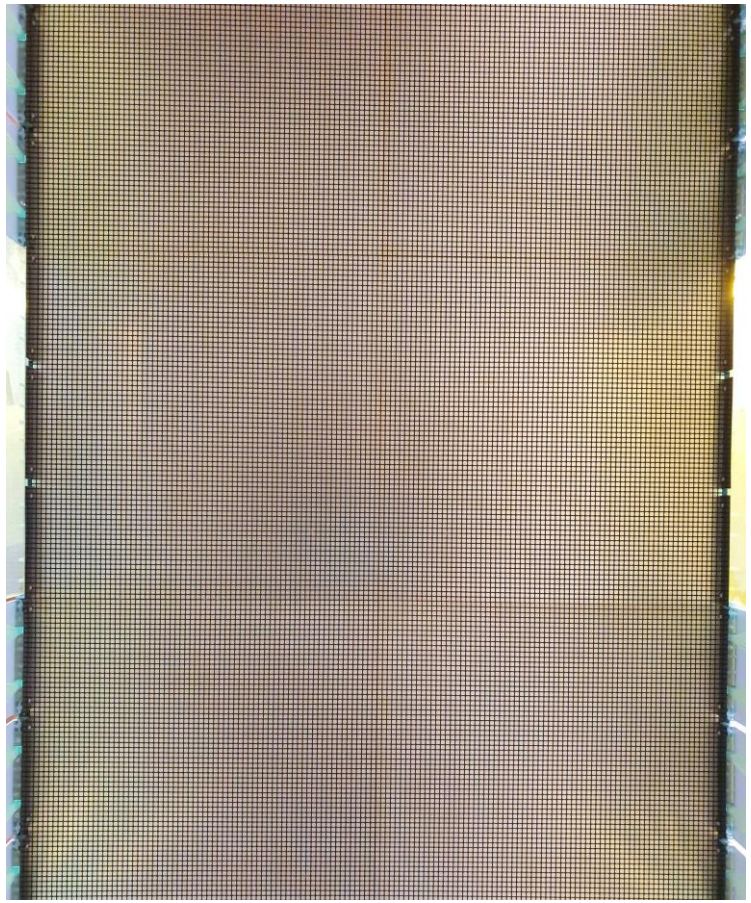
TPC dimensions:
1000 cm^2 anode area, 30 cm max drift distance

Peter Madigan (UC Berkeley)

Summary

LArPix-v2 is a robust and scalable pixel anode system for LArTPCs

- Successful cosmic ray imaging with measured charge stable and consistent with expectation
- Robust to repeated cryogenic cycling
- Scalable system: fast (~few weeks) fully-commercial production/assembly
- Looking ahead, LArPix-v2 will instrument ProtoDUNE-ND for LArTPC neutrino beam physics operation



Each anode composed of 8 tiles, 39.2k channels, 8192 cm^2 total area

Fully instrumented prototype module (70 cm x 70 cm x 140 cm)

LArPix Team

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