Multi-use advanced digital readouts using 3D stacking (Relimage)

Richard Younger

CPAD Instrumentation Frontier Workshop 2021

March 18-21, 2021
Advanced Imager Technology Group

Developing innovative imaging and sensing technology to enable impactful National Security capabilities and scientific discovery

- CCDs
- Geiger-mode APDs
- Superconducting Detectors

- Digital focal planes
- Reconfigurable imagers

- Instruments enabling new scientific discovery & DoD capabilities

Detectors

Read-Out Circuits

Imaging & Sensing Applications
Selected Current Science Programs

- **Digital CCD**
  - Sponsor: NASA
  - Partners: MIT Kavli Inst.

- **Superconducting Detectors**
  - Sponsor: NASA
  - Partners: NASA GSFC

- **Deep Space Optical Comm**
  - Sponsor: NASA
  - Partners: JPL, SSG

- **Pan-FTS**
  - Sponsor: Internal
  - Partners: JPL

- **Brain Imaging**
  - Sponsor: NIH, Line
  - Partners: MGH

- **Ge CCD Tech Maturation**
  - Sponsor: NASA
  - Partners: MIT Kavli Inst.

- **Critical-Angle X-Ray Gratings**
  - Sponsor: NASA
  - Partners: MIT Kavli Inst.

- **THAI-Spice**
  - Sponsor: NASA
  - Partners: SWRI

- **Europa Lander**
  - Sponsor: NASA
  - Partners: JPL

- **Detectors for Particle Physics, Dark Matter**
  - Sponsor: DOE
  - Partners: FNAL, BNL, LBNL
Innovation in Imagers at MITLL

- Digital CCD
- Digital Focal Plane Arrays
- Wide Area Motion Imaging
- On-chip Data Reduction
- On-FPA Computation
- 3-D Stacked Imager
- Multi-function Imagers
- Multi-mode Imager
- High Efficiency LADAR
- Photon-counting Imaging
Evolution of High Performance Imagers

**Useful Information Rate**

**OBSERVE**
- Film Cameras

**RECOGNIZE**
- Early Digital Imagers

**PERCEIVE**
- High Performance Imagers

**Thrusts**
- Higher pixel count
- Higher dynamic range
- New spectral bands
- 3D imagery
- Faster readout rates

**Requires**
- On-chip processing
- Faster communication

Microelectronics revolution
Revolution of High Performance Imagers?

Useful Information Rate

OBSEERVE

Film Cameras

Early Digital Imagers

High Performance Imagers

Adaptive Imagers

Next Gen Consumer Electronics

- Higher pixel counts
- Facial Recognition
- Vehicle LIDAR
- Machine vision

RECOGNIZE

Consumer Electronics

PERCEIVE

Imagers with intelligence to adapt measurement approach in real time

Year
ROIC Fabrication Technology Landscape

*A. Spivak, et. al. “Low-Voltage 96 dB Snapshot CMOS Image Sensor with 4.5 nW Power Dissipation per Pixel”, Sensors 2012, 12(8), 10067-10085*
ROIC Fabrication Technology Landscape

![Graph showing technology node vs. transistors per pixel and circuit density](image)

- Analog pixel CMOS imagers
- Commercial CMOS imaging

**Technology Node**
- 10µm
- 1.5µm
- 800nm
- 90nm
- 65nm
- 14nm
- 7nm

**Circuit Density (Transistors per cm²)**
- 10⁴
- 10⁵
- 10⁶
- 10⁷
- 10⁸
- 10⁹
- 10¹⁰

**Transistors per Pixel**
ROIC Fabrication Technology Landscape

Motorola 68000
Intel 8086

More Transistors
High Capability

Technology Node

Circuit Density (Transistors per cm²)

Transistors per Pixel

10µm 1.5µm 800nm 90nm 65nm 14nm 7nm

Analog pixel
CMOS imagers
Designing a Modular Reconfigurable Imager
Designing a Modular Reconfigurable Imager

General Purpose Resources

- Reconfigurable Logic
- DSP Blocks
- Memory

Detector

Custom Blocks

- Detector Interface
  - Analog to digital converter
  - Unique for different detectors

- Digital Pixel Circuitry
  - Records digital signal
  - Provides local processing

- Digital Processing Circuitry
  - Controls pixel array
  - Processes data for output

FPGA

ROIC

Digital

Analog/Mixed Signal
Designing a Modular Reconfigurable Imager

**General Purpose Resources**

- **Reconfigurable Logic**
- **DSP Blocks**
- **Memory**

**Custom Blocks**

- **Detector Interface**
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- **Digital Pixel Circuitry**
  - Records digital signal
  - Provides local processing
- **Digital Processing Circuitry**
  - Controls pixel array
  - Processes data for output

**3D Sensor Stack**

- Digital
- Analog/Mixed Signal
Reconfigurable Imager Integration Options

3D Packaging
- Die stacking (Akita Elpida)
- Ball Grid Array (Tessera)
- Multi-Chip module (Hess Mechatronics)

2.5D Interposer
- TSMC / Xilinx Vertex 7 FPGA
  - micro-bump 45µm pitch, 10µm diameter TSV 210µm pitch
- IO pitch ~100s µm
  - Course pitch routing, lower performance
- IO pitch ~10s µm
  - Fine pitch routing, but 2D arrangement

High Density 3D
- Direct Bond Interconnect (Ziptronix)
- Cu-Cu bond (Tezzeron)
- Through-oxide-vias (Lincoln Lab)
- IO pitch < 10 µm
  - Short interconnect lengths, highest performance
What Could We Do with a Reconfigurable Imager?

• Address the processing problem with sensing massive amounts of data

• Replace single-purpose sensor with multi-purpose
  – Partial re-use for multiple wavebands
  – Start-up fab cost $O(1,000)$ of a production wafer

• Rapidly prototype new capabilities
  – Avoid 2 – 5 year design cycles

• Inline updates
  – Adapt measurement approach based on measured data or new features

• Enable simultaneous multiple modes of operation

Potential Instrumentation Impact

• On-sensor L1 triggering
  – Relax trigger BW limitations

• Bring advanced capabilities to smaller experiments

• What else?
Outline

• Introduction
• Motivation
  • Relimage Chips
    – Griffin
    – Manticore
• Challenges & Path Forward
MIT LL Reconfigurable Circuit Development for ReImagine

DARPA Reconfigurable Imaging (ReImagine) Program 3D Sensor Architecture

MIT LL Field Programmable Imaging Array (FPIA)

The Griffin chip is an imaging FPGA

<table>
<thead>
<tr>
<th>Tier 3</th>
<th>Waveband Specific Detector Array</th>
<th>Industry</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tier 2</td>
<td>Detector Specific Analog Interface</td>
<td>Industry</td>
</tr>
<tr>
<td>Tier 1</td>
<td>Reconfigurable Digital Circuit with Integrated FPGA Processing</td>
<td>MIT LL</td>
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</table>
# Griffin FPIA Summary

<table>
<thead>
<tr>
<th>Resource Type</th>
<th># Resources on Griffin FPIA</th>
<th>Resources/Pixel</th>
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</thead>
<tbody>
<tr>
<td>Macropixel Tiles</td>
<td>20,480</td>
<td>1 per 8x8 sub array</td>
</tr>
<tr>
<td>Lookup Tables</td>
<td>275,032</td>
<td>N/A</td>
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<tr>
<td>Deserializer Tiles</td>
<td>576</td>
<td>1 per perimeter 8x8 sub array</td>
</tr>
<tr>
<td>DSP Tiles</td>
<td>1736</td>
<td>N/A</td>
</tr>
<tr>
<td>Memory Tiles (8K 16-bit words)</td>
<td>820</td>
<td>N/A</td>
</tr>
<tr>
<td>Perimeter GPIO</td>
<td>275</td>
<td>N/A</td>
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<td>1,310,720</td>
<td>1 per pixel</td>
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<td>18</td>
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</tr>
<tr>
<td>LVDS Tx Pairs, 77K</td>
<td>9</td>
<td>N/A</td>
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</table>

### Griffin FPIA 14 nm Design

Largest IC ever developed within the DoD
- 320 mm² area in a 14 nm FinFET process
- Greater than 6.6 billion transistors
- Greater than 9 km of internal wiring
ReImagine: Proving the Reconfigurable Concept
January 2021

Device Testing

- Gen-1 IC functionality verified
  - All digital blocks operational and first full application demonstrated
  - Basic cryogenic operation verified

Technology Transfer

- Two industry partners with Griffin tier-2 chips
- Griffin T1-only hardware development kit shipped January 2021
Outline

• Introduction
• Motivation
• Relimage Chips
  – Griffin
  – Manticore
• Challenges & Path Forward
Manticore Tier 1 Architecture

- Digital Pixel Array
  - In-pixel memory and SIMD computation pipeline
  - Data collect controllable for mode (intensity, timing), and configuration (rate, bit depth)

- SIMD vector processor
  - Enables parallel and nonlocal computation

- FPGA
  - Enables arbitrary processing logic and control of pixel modes

- Reduced Instruction Set Computer (RISC-V) core
Redefining the Digital Pixel

Manticore SoC Architecture
- 1280 x 1024 Digital Pixel Array
- Column vector processors
- Field Programmable Gate Array (FPGA)

Manticore Macropixel
- Sensor counters, sensor timer
- 7 frames local storage
- Embedded 250MHz math core
  - Fixed-point processing comparable to original Pentium in each core

Resource Type | Manticore
--- | ---
Macropixels | 5,120
Pixel Addressing | Random access w/ wildcards
Pixel Pitch | 12 µm
DSPs | 5120 + 160 + 150
Memory | 7 frames in-pixel
| 2 frames vector
| 4.5 frames in FPGA
Data Flow | 80 column busses
FPGA Lookup Tables | 44,628
3D GPIO | 163,240 + 1920
Perimeter GPIO | 60
LVDS Tx Pairs, 300K / 77K | 18 / 18
3D Pixel Inputs | 1280 x 1024

*SoC = System on a Chip
Manticore Testing Status
February 2021

- Critical functionality passes tests on smallest chip
- Large chip in test in progress; all tests successful to-date
- Projected to complete initial test & characterization Spring 2021

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<td>• Multiple internal and external partners in process of tier 2 design</td>
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<tr>
<td>• Anticipate at least one bonded assembly to begin late 2021</td>
</tr>
<tr>
<td>• Demo camera in 2022</td>
</tr>
</tbody>
</table>
Using Manticore: a few examples

Simulated Capabilities

In-pixel Gain & Offset

- 16 bit, (32 bit math)
- 100k+ FPS

Filter + Exceedance

- 16 bit, 3×3 Convolutional filter
- Per-pixel threshold
- ~100k FPS on-chip

In-array 2D FFT

- 16 bit, 1024×1024 spatial transform
- ~10 FPS

*FFT = Fast Fourier Transform

Max design clock speed of 250 MHz
Rates do not include off-chip readout
Subarray processing can be faster
More sophisticated adaptive processing possible in-pixel and in-array
Using Reconfigurable Imagers

Conventional Processing
- In-pixel NUC
- In-array 2D FFT
- Exceedance

Machine Learning
- Simulated in-pixel NUC & exceedance rates in excess of 100,000 FPS
- More sophisticated adaptive processing possible in-pixel and in-array
- Conducted feasibility study for split learning model on Griffin

Multimodal Sensing
- High timing resolution collection enabled by on-chip trigger
Outline

• Introduction
• Motivation
• ReImagine Chips
  – Griffin
  – Manticore

• Challenges & Path Forward
Extreme Environments

- Commercial advanced node FinFETs show comparable leakage to 90nm
  - Potential to improve 14nm process leakage in RHBP (radiation hardening by process)

- Foundries do not generally characterize processes for cryogenic temperatures
  - Analog IP such as PLLs and high-speed IO blocks for room temperature will not work at low temperature
    - Cryo-interested communities need to develop (and publish) their own analog IP

- Digital design challenges at extreme low temperatures are analog-y: timing violations, etc.

- Griffin & Manticore will be tested at cryogenic temperatures
  - Initial results are good
What Next?

Limitations

• Cost
  – 14nm fabrication is extremely expensive
  – Multi-purpose device may be the only way to pay for the fab
  – Design mistakes become extremely expensive

• Large area sensors – existing reconfigurable designs are not abuttable

• Power
  – Any multi-purpose device will sacrifice efficiency relative to a single purpose device

Path Forward

• Design refinement

• Deeper stacking?
  – Computation tier, Memory tier, ML tier, Comms tier, etc.
  – Increase modularity
  – Path to abuttability?

• Extreme environments
  – Radiation hardening
    ▪ RH by Process
    ▪ RH by Design
  – Cryogenic qualified IP
Summary

• Lincoln Laboratory has a decades-long experience making unique focal planes in support of national security and science

• Emerging 3D stacking technology enables integration of new technology into imaging sensors

• A reconfigurable imager has the potential to help address data quantity problems and bring advanced sensing to more science and physics experiments

• MIT Lincoln Laboratory has prototyped two new reconfigurable sensor back ends, incorporating unprecedentedly flexible and adaptable image processing
### MIT/LL ReImagine Team

<table>
<thead>
<tr>
<th>Rich Younger</th>
<th>Maria Blood</th>
<th>Renee Lambert</th>
<th>Tim Gagnon</th>
</tr>
</thead>
<tbody>
<tr>
<td>Valerie Finnemeyer</td>
<td>Glenn Garvey</td>
<td>Donna Yost</td>
<td>Erik Duerr</td>
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<tr>
<td>Jon Frechette</td>
<td>Kate Gillis</td>
<td>Sandra Lee</td>
<td>Eric Dauler</td>
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<tr>
<td>Sue Burzyk</td>
<td>Philemon Chose</td>
<td>Hannah Whisnant</td>
<td>Dan Ripin</td>
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<tr>
<td>Brian Tyrrell</td>
<td>Kate Thurmer</td>
<td>Praneeth Vepakomma (MIT)</td>
<td>Kaitlyn Dixon</td>
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<tr>
<td>Matt Stamplis</td>
<td>Jordan Lahanas</td>
<td>Tom Karolyshyn</td>
<td>Stephan Chase</td>
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<td>Jonathan Leu</td>
<td>Tom Ross</td>
<td>Greg Rowe</td>
<td>Kenny Sims</td>
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<tr>
<td>Peter Grossmann</td>
<td>Ian Brown</td>
<td></td>
<td>Elaine Swenson</td>
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<tr>
<td>Matt Gregory</td>
<td>Tony Kryzak</td>
<td>Farhan Adil</td>
<td>Chris Leitz</td>
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<td>George Jordy</td>
<td>Austin Holloway</td>
<td>Phillip Bailey</td>
<td>Kevin Ryu</td>
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<td>Tom Cheng</td>
<td>Tony Soares</td>
<td>Hernan Castro</td>
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<td>Jim Wey</td>
<td>David Volson</td>
<td>Dan Santiago</td>
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<tr>
<td>Alice Lee</td>
<td>Jerry Lipson</td>
<td>Domenic Terranova</td>
<td></td>
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<tr>
<td>Ana-Maria Mandrila Vacca</td>
<td>Mike Cooper</td>
<td>Tim Smith</td>
<td></td>
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<tr>
<td>Brian Yu</td>
<td></td>
<td>Dmitriy Kaplan</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bob D'Ambra</td>
<td></td>
</tr>
</tbody>
</table>

Designing and producing these chips is the product of a large team of professionals.
Questions?
Supplemental
Machine Learning on Griffin
Example Application – Passive Camera

- Like an FPGA, imager logic is written in Verilog
- Control logic might (e.g.) be designed as a FSM
- Processing logic reads pixel data, post-processes, and transfers off chip
Example Application #2 – Smart Camera

- Logic generates signal on sensed exceedance
- Only triggered data read out
  - Reduced bandwidth
- Very low latency possible

Can add feedback to change sensing modality
Example Application #3 – ML Camera

- Add CNN layers for processing gated events

Diagram:
- Passive Input Control
- Pixel Array Model (MITLL supplied)
- Event Sensing
- CNN Layers
- Output

Event Sensing

CNN

Output
Machine Learning Feasibility

• Character recognition example using client/server split learning architecture
  – Split learning separates input data from full body of inference network

• Used hls4ml to translate character recognition split learning model in Keras to Vivado HLS

• Results: This model should, with further optimizations, fit on Griffin
  – Need to investigate network compression (pruning) & DSP re-use
  – 2D convolutional layers were a challenge for hls4ml (as of v0.1.6)

<table>
<thead>
<tr>
<th>Resource</th>
<th>Split Learning Model</th>
<th>Kintex UltraScale 115</th>
<th>Griffin FPIA</th>
</tr>
</thead>
<tbody>
<tr>
<td>LUTs</td>
<td>92,395</td>
<td>663,390</td>
<td>275,032</td>
</tr>
<tr>
<td>I/O</td>
<td>634*</td>
<td>702</td>
<td>275</td>
</tr>
<tr>
<td>DSP tiles</td>
<td>3,286</td>
<td>5,530</td>
<td>1,736</td>
</tr>
<tr>
<td>BRAM</td>
<td>60.5</td>
<td>2,160</td>
<td>820</td>
</tr>
</tbody>
</table>

* Includes image

Compare / Contrast Griffin & Manticore
# Two Tier-1 Chips

<table>
<thead>
<tr>
<th>Griffin</th>
<th>Manticore</th>
</tr>
</thead>
<tbody>
<tr>
<td>• 1280 × 1024, 12μm pitch</td>
<td>• 1280 × 1024, 12μm pitch</td>
</tr>
<tr>
<td>• Reconfigurable</td>
<td>• Reconfigurable</td>
</tr>
<tr>
<td>• FPGA-based architecture</td>
<td>• SoC-based architecture</td>
</tr>
<tr>
<td>– Pixel blocks are connected by custom FPGA interconnect &amp; neighbor shift bus</td>
<td>– Pixel blocks &amp; edge processor pipelined in SIMD GPU-style interconnect</td>
</tr>
<tr>
<td>▪ Data routing is entirely user-controlled</td>
<td>▪ Data routing follows hard column busses</td>
</tr>
<tr>
<td>▪ Reconfigurable processing &amp; memory at periphery</td>
<td>▪ Programmable processing &amp; memory integrated in pipeline</td>
</tr>
<tr>
<td>– Enormous flexibility for data flow, detector configuration</td>
<td>– Good flexibility for data flow, pixel population</td>
</tr>
<tr>
<td>– Enormous flexibility to implement custom processing (AI, other)</td>
<td>– Efficient implementation of common algorithms</td>
</tr>
<tr>
<td></td>
<td>– Includes FPGA block for custom processing</td>
</tr>
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</table>
## Manticore / Griffin Summary

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<th>Manticore Resources</th>
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<tr>
<td>Macropixels</td>
<td>20,480</td>
<td>5,120</td>
</tr>
<tr>
<td>Pixel Addressing</td>
<td>User defined (FPGA)</td>
<td>Random access w/ wildcards</td>
</tr>
<tr>
<td>Data Deserializers</td>
<td>1 Deserializer per perimeter 8x8</td>
<td>1 bus/column</td>
</tr>
<tr>
<td>DSPs</td>
<td>1736 FPGA</td>
<td>5120 + 160 + 150</td>
</tr>
<tr>
<td>Memory</td>
<td>1 frame in-pixel 5.1 frames in FPGA</td>
<td>7 frames in-pixel 2 frames vector 4.5 frames in FPGA</td>
</tr>
<tr>
<td>Lookup Tables</td>
<td>275,032</td>
<td>44,628</td>
</tr>
<tr>
<td>3D GPIO</td>
<td>163,240 (8 per 8x8)</td>
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<td>275</td>
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<td>LVDS Tx Pairs, 300K / 77K</td>
<td>18 / 9</td>
<td>18 / 18</td>
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<td>3D Pixel Inputs</td>
<td>1,310,720</td>
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Using Reconfigurable Imagers

### Conventional Processing
- In-pixel NUC
- In-array 2D FFT

### Machine Learning
- Simulated in-pixel NUC & exceedance rates in excess of 100,000 FPS
- More sophisticated adaptive processing possible in-pixel and in-array
- Conducted feasibility study for split learning model on Griffin

### Multimodal Sensing
- High timing resolution collection enabled by on-chip trigger
Manticore Slides
Redefining the Digital Pixel

- 1280 x 1024 Digital Pixel Array
- Column vector processors
- Field Programmable Gate Array (FPGA)

Digital Pixel Array

Vector Processor

FPGA

192 μm

18.75 mm

Manticore SoC Architecture

Manticore Macropixel

- Sensor counters, sensor timer
- 7 frames local storage
- Embedded 250MHz math core
  - Fixed-point processing comparable to original Pentium in each core

- 5,120 Macropixels per array

<table>
<thead>
<tr>
<th></th>
<th>Manticore Macropixel</th>
<th>1st Generation Intel Pentium</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die Size (mm square)</td>
<td>0.192</td>
<td>16.7 x 17.6</td>
</tr>
<tr>
<td># transistors</td>
<td>0.82 Million</td>
<td>3.1 Million</td>
</tr>
<tr>
<td>Process</td>
<td>14 nm</td>
<td>800 nm</td>
</tr>
<tr>
<td>Local memory</td>
<td>3kB</td>
<td>16kB</td>
</tr>
<tr>
<td>Max Clock rate (MHz)</td>
<td>250 (design)</td>
<td>100 MHz</td>
</tr>
<tr>
<td>Million Ops per second</td>
<td>250 MOPS</td>
<td>188 MIPS</td>
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<tr>
<td>Architecture size</td>
<td>32 bits</td>
<td>32 bits</td>
</tr>
<tr>
<td>Operand size</td>
<td>16 bits</td>
<td>32 bits</td>
</tr>
</tbody>
</table>

*SoC = System on a Chip
Example Application

- Pixel and vector commands issued by FPGA (Verilog) or RISC peripheral processor
- Rich set of commands allow extensive in-pixel or edge processing
- For supported operations, processing is more power and time efficient
Macropixel Facts

### Manticore Macropixel Fun Facts

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<td>32 bits</td>
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</table>

There are 5,120 macropixels in the largest Manticore array
### Tier 1 Overview

- **We’ve designed 4 imagers:**
  - 64 x 64: XSmallTall (XST)
  - 256 x 256: MediumGrande (MG)
  - 640 x 512: LargeTall (LT)
  - 1280 x 1024: XLarge Tall (XLT)

<table>
<thead>
<tr>
<th>Variant Name</th>
<th>Array Size</th>
<th>Die X (mm)</th>
<th>Die Y (mm)</th>
<th>Pixel SRAM</th>
<th>Vector SRAM</th>
<th>FPGA SRAM</th>
<th>LUTs</th>
<th>DSP</th>
<th>GPIO</th>
<th>3D</th>
<th>LVDS</th>
</tr>
</thead>
<tbody>
<tr>
<td>XSmallTall</td>
<td>64x64</td>
<td>3.6</td>
<td>6.3</td>
<td>56KiB</td>
<td>256KiB</td>
<td>768KiB</td>
<td>2460</td>
<td>10</td>
<td>8</td>
<td>128</td>
<td>18</td>
</tr>
<tr>
<td>MediumGrande</td>
<td>256x256</td>
<td>5.9</td>
<td>9.6</td>
<td>896KiB</td>
<td>1.0MiB</td>
<td>3.0MiB</td>
<td>11460</td>
<td>42</td>
<td>24</td>
<td>384</td>
<td>18</td>
</tr>
<tr>
<td>LargeTall</td>
<td>640x512</td>
<td>10.5</td>
<td>11.66</td>
<td>4.4MiB</td>
<td>2.0MiB</td>
<td>5.6MiB</td>
<td>21900</td>
<td>75</td>
<td>48</td>
<td>768</td>
<td>18</td>
</tr>
<tr>
<td>XLarge Tall</td>
<td>1280x1024</td>
<td>18.75</td>
<td>18.35</td>
<td>17.5MiB</td>
<td>5.0MiB</td>
<td>11.2MiB</td>
<td>44628</td>
<td>150</td>
<td>60</td>
<td>1920</td>
<td>18</td>
</tr>
</tbody>
</table>

*Current as of 11 February 2020*
Torch
Automatic Generation of Application Specific FPGAs

The top level module instantiates each tile in the fabric.

HDL models of routing resources and configuration bit storage come from internal libraries.

HDL models of logic blocks come from standard or custom IP libraries.
SUMMARY OF FPIA Use Model – GRIFFIN PROGRAMMING PACK

• Model application using hardware description languages

• Run synthesis, optimization, place and route, bitstream generation

• Load bitstream onto FPGA chip for use in field
MITLL VTR Enhancements

- Added syntax support for synthesis
- Command-line API unification of three VTR tools
- Bitstream generation
Putting the Griffin Programming Pack to Work

• Programming pack end use:
  • Consult documentation
  • Review example applications
  • Integrate hard IP models
  • Configure Griffin with Torch
Background on other MIT/LL work
MIT-LL Microelectronics Laboratory
An Enabling Resource for Advanced CCD Fabrication

- 70k ft², 8100 ft² Class-10, 10,000 ft² Class-100
- Production-class sub-90-nm toolset on 200-mm-diameter wafers
- Lithography capabilities ranging from i-line to e-beam
- Process capabilities include CCDs, APDs, low power FDSOI CMOS, 3D integration
High Density 3D Integration Development at MIT-LL

- **MOSAIC I**
  - **ARMY**
    - APS - CMOS
  - 2000

- **VISA**
  - Three tier
    - 1.5V CMOS
    - 3.3V CMOS
    - APD
  - 2005

- **MOSAIC II**
  - Three tier
    - 180 nm CMOS
  - 2010

- **SWIR**
  - InGaAs detector - CMOS
  - 2015

- **Advanced Imagers**
  - 200 mm

### 3D Integration Technology Demonstrations

- **3DL1**
  - Three tier
    - 180 nm CMOS
  - Two tier
    - Foundry
    - JAZZ

- **3DM2**
  - Three tier
    - 150 nm CMOS
  - RF third tier

- **3DM3**
  - CMOS - MEMS

- **NIRD**
  - Photonic - CMOS

- **EPHI**
  - 200 mm

- **GaN – CMOS**
  - 200 mm
Principal Driver for 3D Development at MIT-LL

- Advanced Imaging Array Goals
  - 100% fill factor
  - On-Chip processing
  - Fast read out rate, entire array in <1msec
  - Scalable to large-area focal plane

- Achieved with Heterogeneous 3D integration

Demonstrated 1024 x 1024 pixel array imager with more than 1 million 3D vias on 8 µm pitch with >99.999% via yield

Wafer-Scale 3D Integration Demonstrations of Advanced Focal Plane Imagers

- 100% fill factor detector
- Heterogeneous optimized tier function
- Local image processing
- Fast read out rate – entire array in <1 msec
- Scalable to large-area focal plane

Image from 3D Chip

Chip Photomicrograph

Four Side Abuttable Imager

Tiled Focal Plane

SEM cross section of bonded Imager to CMOS

Demonstrated 1024 x 1024 pixel array imager with more than 1 million 3D vias on 8 µm pitch with >99.999% via yield

“ A Four-Side Tilable Back Illuminated Three-Dimensionally Integrated Megapixel CMOS Image Sensor”
Suntharalingam et. al ( ISSCC 2005 & 2009)
High Density Wafer-Scale Integration Offers Highest Density Interconnect

Dense unrestricted 3D via interconnect of three CMOS tiers with CMOS electrical connections between tiers

High-Density 3D Integration for Micro-Systems Yost et al. (GOMAC Tech 2013)
Prototype Germanium CCDs

32 × 32 Pixel Array

Device under Test

First Light Imagery

Prototypes show expected performance, now scaling to megapixel-class imagers
Roadmap for Next-Generation CCD Capabilities

Low-Voltage CCDs

- New process to enable operation at CMOS-compatible clock voltages

Novel Low-Noise Amplifiers

- New amplifier under development for single-photon sensitivity

High-Speed Focal Planes

- Chip stacking to enable high-speed imaging, on-chip processing

Future devices will combine best features of CMOS and CCD imagers, supporting low-noise, high-speed imaging
Geiger-Mode Avalanche Photodiode (GmAPD) Detector Technology

Photodiode Modes of Operation for MIT/LL Digital Pixel FPAs

Gain

100
10
1
DC bias
breakdown voltage
Reverse Bias

Ordinary photodiode
Linear mode APD
Geiger mode APD
overbias

A single photon absorbed by the overbiased APD generates a fast rush of current

Geiger-mode APDs provide:

- Single-photon sensitivity
- Lots of current → easy digitization
- Fast breakdown → excellent (sub-ns) time resolution
- TEC accessible temperatures → low SWAP
- Large format arrays

Device Cross-section

Lenslet array
Gm APD array
Digital readout circuit
Lincoln Superconducting Technology in Microcalorimeters

Increase Pixel Count

TES arrays with 49,100 pixels

Lincoln fabrication process helps NASA overcome the wiring challenge for large TES arrays

Sensitivity

Use high-Q aluminum process to reduce noise

Ease of Use

Use single flux quantum circuits to digitize TES signals on-chip